CHRONTEL

# CH9089

*Preliminary*

# PCI Clock Generator

## Features

- Generates preset CPU and PCI frequencies, 1 peripheral clock, and buffers the input reference frequency
- Supports mix 3.3V Pentium™ with 5V chipset designs
- Two 3.3V CPU clock outputs and one 3.3V buffered reference frequency output
- Three CPU output buffers and one Early CPU buffer for 5V chip set
- Supports both synchronous and asynchronous PCI clocks with 6 PCI output buffers at 5V
- Low skew output buffers
- Power down, slow down, or stop clock feature supporting "Green PC" applications
- External loop filter provides exceptionally smooth, glitch-free frequency transitions
- Low, short-term and long-term jitter
- Supports Pentium™ and all x86-based designs
- Supports ISA, VESA, and PCI-based designs
- CMOS technology in 36-pin SSOP (300 mil)
- Mixed voltage (5V and 3.3V) supply

Pentium is a trademark of Intel Corporation

## Description

CH9089 is a triple PLL clock generator designed for mixing 5V system logic chipsets with 3.3V Pentium™ designs on the same motherboard. CH9089 buffers the 14.318 MHz reference frequency into two outputs, generates multiple CPU and PCI clocks from a preset ROM table, and provides a 24 MHz peripheral clock.

CH9089 provides two CPUQ and one XOUTQ outputs supporting up to two Pentium™ chips at 3.3V. CH9089 also provides three CPUs, one Early CPU, one XOUT, one 24MHz , and six PCI clock outputs to support system logic chipsets operating at 5V.

CPU output frequencies are selected by the frequency select inputs, FS[1:0]. Early CPU output typically precedes the CPU and CPUQ outputs by 2 to 5 ns.

Both synchronous and asynchronous PCI clocks are supported using the PSYNC* select pin. When PSYNC* is high, PCI clocks are set at 33.3 MHz. Otherwise, PCI clock outputs are synchronous with the CPU clock and runs at half the CPU clock.

CH9089 is available with power down (PD*), slow down (SD*), or stop clock (CPUEN) options, which are ideal for low power "Green PC" applications. All input pins, including FS [1:0], are TTL compatible with internal pull-ups, and can be driven from either a 3.3V or 5V signal.

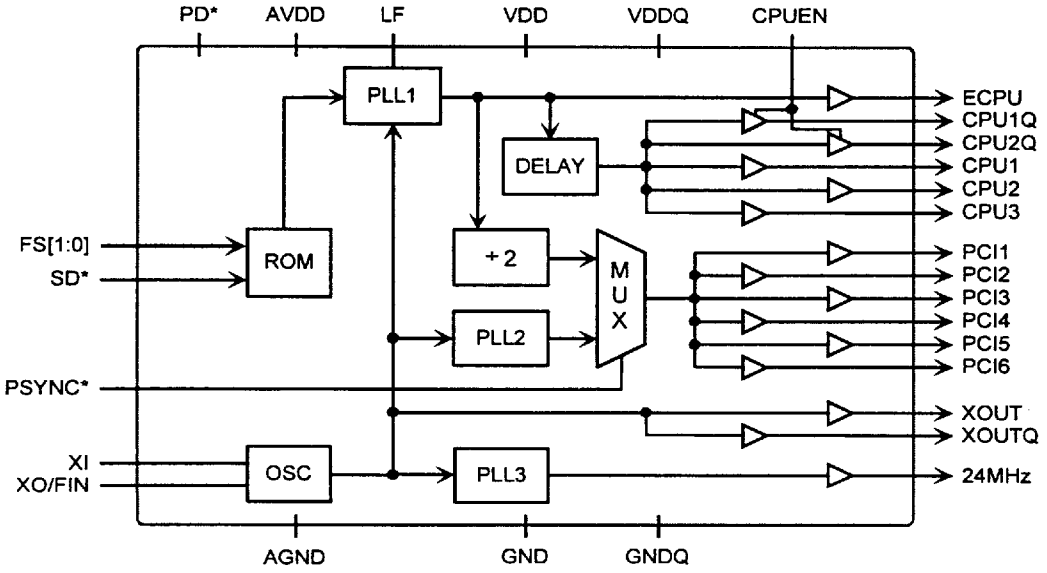


**Figure 1: Block Diagram**

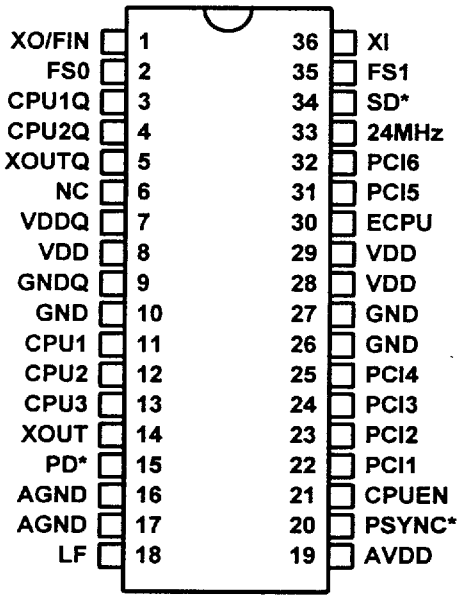


**Figure 2: CH9089A Pinout Diagram**

**Table 1 • Pin Description CH9089A**

| Pin | Type | Symbol | Description |
|---|---|---|---|
| 1 | Out / In | XO / FIN | Crystal output or external FREF input |
| 2, 35 | In | FS0, FS1 | CPU clock select inputs (internal pull-up) |
| 3, 4 | Out | CPU1Q, CPU2Q | 3.3V CPU clock outputs |
| 5 | Out | XOUTQ | 3.3V buffered reference (14.318 MHz) clock output |
| 6 | – | NC | No connect |
| 7 | Power | VDDQ | 3.3V power supply for CPU1Q, CPU2Q, and XOUTQ |
| 8, 28, 29 | Power | VDD | 5V power supply |
| 9 | Power | GNDQ | Reference ground for CPU1Q, CPU2Q, and XOUTQ |
| 10, 26, 27 | Power | GND | Ground |
| 11, 12, 13 | Power | CPU1 – CPU3 | 5V CPU clock outputs |
| 14 | Out | XOUT | 5V buffered reference (14.318 MHz) clock output |
| 15 | In | PD* | Power down input (active low, internal pull-up) |
| 16, 17 | Power | AGND | Analog ground |
| 18 | Out | LF | External loop filter |
| 19 | Power | AVDD | Analog 5V supply |
| 20 | In | PSYNC* | Synchronous or asynchronous PCI clock select input (active low, internal pull-up) |
| 21 | In | CPUEN | CPU1Q and CPU2Q clock enable pin (active high, internal pull-up). When CPUEN is low, both CPU1Q and CPU2Q are disabled and held at a low state. |
| 22 – 25, 31 – 32 | Out | PCI1 – PCI4, PCI5 – PCI6 | PCI clock outputs (5V) |
| 30 | Out | ECPU | Early CPU clock output (5V) |
| 33 | Out | 24MHz | 24 MHz clock output (5V) |
| 34 | In | SD* | Slow down input (active low, internal pull-up) |
| 36 | In | XI | Crystal input |

### Table 2 • CPU Clock Output Frequency (in MHz)

| CPU Clock Select Inputs | | ECPU, CPU, and CPUQ Outputs | |
|---|---|---|---|
| FS1 | FS0 | SD* = 1 | SD* = 0 |
| 0 | 0 | 60.0 | 30.0 |
| 0 | 1 | 50.0 | 25.0 |
| 1 | 0 | 60.0 | 33.3 |
| 1 | 1 | 66.6 | 33.3 |

**Note:** ECPU typically precedes CPU and CPUQ outputs by 2 – 5 ns

### Table 3 • PCI Clock Output Frequency (in MHz)

| PSYNC* | PCI Output |
|---|---|
| 0 | CPU ÷ 2 |
| 1 | 33.3 |

### Table 4 • Absolute Maximum Ratings

| Symbol | Description | Value | Unit |
|---|---|---|---|
| VDD | Power supply voltage with respect to GND | –0.5 TO +7.0 | V |
| VIN | Input voltage on any pin with respect to GND | –0.5 TO VDD+0.5 | V |
| TSTOR | Storage temperature | –55 TO +150 | °C |

**Note:** Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Table 5 • DC Specifications (Operating Conditions: $T_A$ = 0°C – 70°C, $V_{DD}$ = 5V ±5%)

| Symbol | Description | Test Condition @TA = 25°C | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOH | Output high voltage | VDD = 4.75V, IOH = 12mA | 2.4 | | | V |
| VOL | Output low voltage | VDD = 4.75V, IOL = 12mA | | | 0.4 | V |
| VIH | Input high voltage | | 2.0 | | | V |
| VIL | Input low voltage | | | | 0.8 | V |
| IPU | Input pull-up current | | | 5 | 20 | µA |
| ILK | Input leakage current | | –10 | | 10 | µA |
| CI | Input capacitance | Except XO / FIN, XI | | | 10 | pF |
| CI | Input capacitance | Pins XO / FIN, XI | | 20 | | pF |
| IDD | Operating current | VDD = 5V CPU = 40 MHz, No load<br>CPU = 80 MHz, No load | | 35<br>45 | | mA |

### Table 6 • AC Specifications (Operating Conditions: $T_A$ = 0°C – 70°C, $V_{DD}$ = 5V ±5%)

| Symbol | Description | Test Condition @TA = 25°C | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FXTAL | Crystal frequency | | | 14.318 | | MHz |
| FIN | Input frequency (crystal pin) | | 1 | 14.318 | 32 | MHz |
| TR | Output clock rise time | 30 pF load, VOUT = 0.8V to 2.0V | | | 2 | ns |
| TF | Output clock fall time | 30 pF load, VOUT = 0.8V to 2.0V | | | 2 | ns |
| TDC | Duty cycle | | 45 | 50 | 55 | % |
| TJCC | Jitter, cycle to cycle | CPU = 50 MHz | | TBD | | ps |
| TFT | Frequency transition time | 8 – 80 MHz with 0.1 µF LF capacitor | | 10 | | ms |
| TPU | Power up time | From OFF to 100 MHz with 0.1 µF LF capacitor | | 15 | | ms |
| TPLH, TPHL | Propagation delay (ECPU to CPU) | | | 3.2 | | ns |
| TSKEW1 | Buffer out skew (same buffer group) | | | | 0.7 | ns |
| TSKEW2 | PCI to CPU (synchronous PCI) | | | | 1.5 | ns |

**Table 7 • DC Specifications for CPUQ and XOUTQ (Operating Conditions: $T_A$ = 0°C – 70°C, $V_{DDQ}$ = 3.3V ± 0.3V)**

| Symbol | Description | Test Condition @$T_A$ = 25°C | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage | $V_{DD}$ = 3.0V, $I_{OH}$ = 6mA | $V_{DD}$ – 0.5 | | | V |
| $V_{OL}$ | Output low voltage | $V_{DD}$ = 3.0V, $I_{OL}$ = 8mA | | | 0.5 | V |

**Table 8 • AC Specifications for CPUQ and XOUTQ (Operating Conditions: $T_A$ = 0°C – 70°C, $V_{DD}$ = 3.3V ± 0.3V)**

| Symbol | Description | Test Condition @$T_A$ = 25°C | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_R$ | Output clock rise time | 30 pF load, $V_{OUT}$ = 0.8V to 2.0V | | | 5 | ns |
| $T_F$ | Output clock fall time | 30 pF load, $V_{OUT}$ = 0.8V to 2.0V | | | 5 | ns |
| $T_{DC}$ | Duty cycle | | 45 | 50 | 55 | % |
| $T_{JCC}$ | Jitter, cycle to cycle | CPU = 50 MHz | | TBD | | ps |
| $T_{FT}$ | Frequency transition time | 8 – 80 MHz with 0.1 µF LF capacitor | | 10 | | ms |
| $T_{PU}$ | Power up time | From OFF to 100 MHz with 0.1 µF LF capacitor | | 15 | | ms |
| $T_{PLH}$, $T_{PHL}$ | Propagation delay (ECPU to CPUQ) | | | 3.2 | | ns |
| $T_{SKEW1}$ | Buffer out skew (same buffer group) | | | | 0.7 | ns |
| $T_{SKEW2}$ | PCI to CPUQ | | | | 1.5 | ns |
| $T_{SKEW3}$ | CPU (5V) to CPUQ (3.3V) | | | | 1.0 | ns |

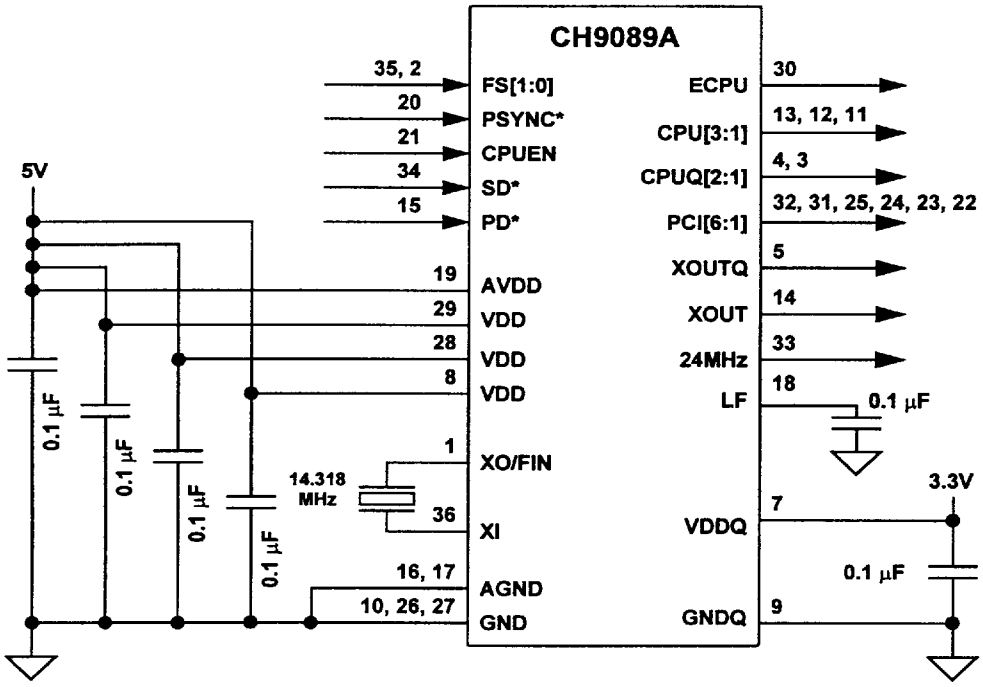


**Figure 3: Application Schematic**

| ORDERING INFORMATION | | | |
|---|---|---|---|
| Part number | Package type | Number of pins | Voltage supply |
| CH9089A-M-D | 300 mil SSOP | 36 | 5V and 3.3V |


# Chrontel

**2210 O'Toole Avenue**
**San Jose, CA 95131-1326**
**Tel: (408) 383-9328**
**Fax: (408) 383-9338**




47011