Graphics Clock Generator

Features

- Synthesizes 32 preset frequencies and buffers the optional reference frequency
- Requires only three external components: one 14.318 MHz crystal and two 0.1 µF capacitors
- Supports MDA, CGA, VGA, Super-VGA, and 8514 graphics standards
- Supports output frequencies up to 110 MHz
- Provision for an external frequency input
- Advanced PLL design with low-phase jitter
- Internal PLL remains locked while external frequency is selected
- Pin compatible to ICS1394 / 1494
- CMOS technology in 20-pin PDIP and SOIC
- 5V or 3.3V supply. For specific details on the 3.3V version, please consult Chrontel.

Description

CH9201 is a high performance PLL clock generator designed for graphics systems and applications where selection of multiple frequencies is desired. The output frequency is selected from a set of 32 frequencies by setting the FSx pins to VDD or GND. CH9201 uses a standard 14.318 MHz reference frequency. Other input frequencies can be used to obtain different output frequencies. In addition to supporting the most common graphics controller frequency tables, CH9201 provides the option of defining the frequency table by mask programming the internal ROM.

CH9201 reduces system costs by replacing multiple external clock oscillators, reducing board layout space, eliminating external components, and lowering inventory costs.

CH9201 has the capability to multiplex externally generated signal sources into the signal path. This feature allows the device to overlay text or graphics with an external VCR or frame grabber so real time images can be superimposed for multimedia applications.

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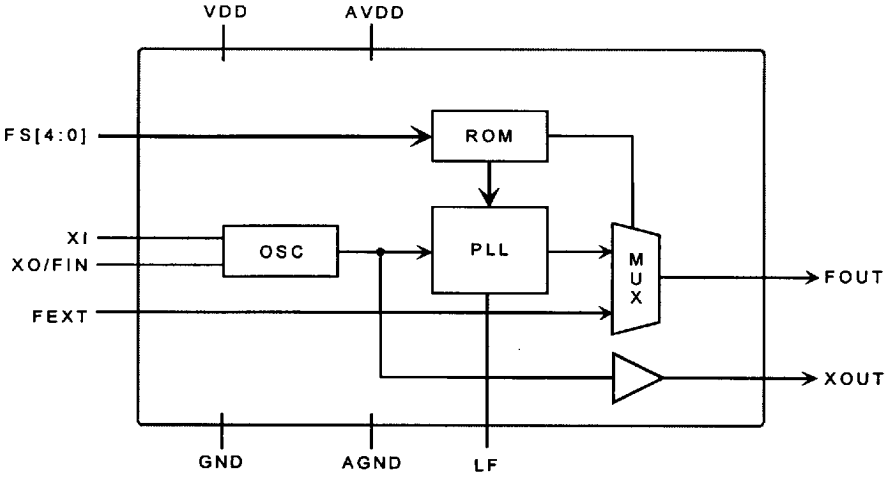

Figure 1: Block Diagram

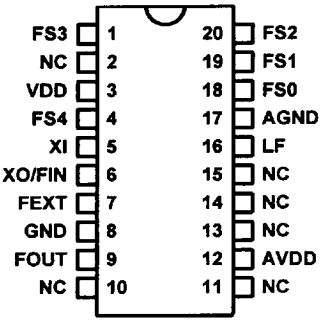

Figure 2: CH9201AA

Table 1 • Pin Description

Pin	Type	Symbol	Description
1, 4, 18, 19, 20	In	FS3, FS4, FS0, FS1, FS2	Frequency select inputs (internal pull-up)
2, 10, 11, 13, 15	—	NC	No connection
3	Power	VDD	5V supply
5	In	XI	Crystal input
6	Out / In	XO / FIN	Crystal output or external FREF input
7	In	FEXT	External frequency input (internal pull-down)
8	Power	GND	Ground
9	Out	FOUT	Synthesized frequency output
12	Power	AVDD	Analog 5V supply
14	—	NC	No connection, **MUST BE LEFT OPEN**
16	In	LF	External loop filter
17	Power	AGND	Analog ground

Table 2 • Frequencies for CH9201AA (in MHz)

FS4	FS3	FS2	FS1	FS0	FOUT
0	0	0	0	0	25.175
0	0	0	0	1	28.322
0	0	0	1	0	40.0
0	0	0	1	1	32.514
0	0	1	0	0	50.35
0	0	1	0	1	65.0
0	0	1	1	0	38.0
0	0	1	1	1	44.9
0	1	0	0	0	25.175
0	1	0	0	1	44.9
0	1	0	1	0	50.35
0	1	0	1	1	65.0
0	1	1	0	0	40.0
0	1	1	0	1	FEXT **
0	1	1	1	0	50.35
0	1	1	1	1	80.0

FS4	FS3	FS2	FS1	FS0	FOUT
1	0	0	0	0	25.175
1	0	0	0	1	28.322
1	0	0	1	0	32.514
1	0	0	1	1	36.0
1	0	1	0	0	40.0
1	0	1	0	1	44.9
1	0	1	1	0	50.35
1	0	1	1	1	65.0
1	1	0	0	0	25.175
1	1	0	0	1	28.322
1	1	0	1	0	32.514
1	1	0	1	1	36.0
1	1	1	0	0	40.0
1	1	1	0	1	44.9
1	1	1	1	0	50.35
1	1	1	1	1	62.0

Note: ** PLL remains locked at specified frequency

Custom Frequency Option

Customers can specify up to 32 custom frequencies by mask programming the ROM. Although the frequency range of CH9201 spans from 5 MHz to 110 MHz, the output stage is only able to maintain TTL levels up to 90 MHz. At frequencies above 90 MHz, the following options are recommended:

- in most cases, an AC coupling circuit
- an ECL differential line receiver used to buffer the output to ECL levels.

Layout Considerations

For the best phase-noise performance, the following layout rules are recommended:

- Place all power supply bypass capacitors in close proximity to their respective power pins.
- Use a ground plane to connect GND, AGND and all external component grounds. Isolate this ground plane from other circuits by connecting it to ground at the card edge.
- Use a low inductance trace to connect AVDD, the loop filter capacitor, and the decoupling capacitor.
- Place the loop filter capacitor and the reference crystal close to the CH9201 device.
- Do not run any signal lines through the synthesizer section of the board, especially node LF.

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Table 3 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	−0.5 to +7.0	V
VIN	Input voltage on any pins with respect to GND	−0.5 to VDD+0.5	V
TSTOR	Storage temperature	−55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4 • DC Specifications (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 4mA	2.4			V
VOL	Output low voltage	VDD = 4.75V, IOL = 8mA			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			5	20	µA
ILK	Input leakage current		−10		10	µA
IDD	Operating current	VDD = 5V FOUT = 50MHz, No load		20		mA

Table 5 • AC Specifications (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FIN	Crystal / FREF input		10	14.318	20	MHz
FOUT	Output frequency		5		110	MHz *
TR	Output clock rise time	CL = 25pF, VOL – VOH		2		ns
TF	Output clock fall time	CL = 25pF, VOL – VOH		2		ns
TDC	Output clock duty cycle	VDD = 5V @VDD / 2	40	50	60	%

Note: * Output levels are guaranteed up to 90 MHz. Please consult Chrontel for suggested circuit implementations for frequencies higher than 90 MHz.

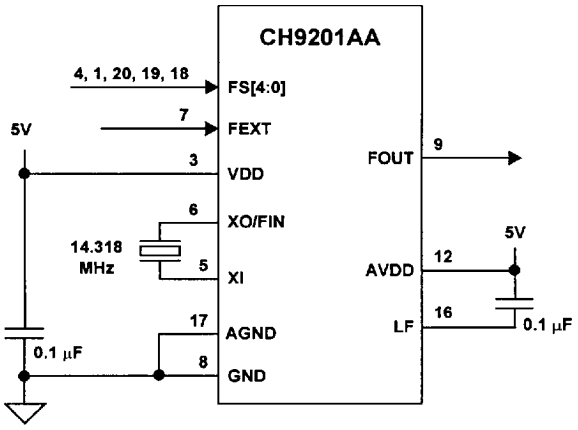

Figure 3: Application Schematic

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9201AA-NC	300 mil PDIP	20	5V
CH9201AA-SC	300 mil SOIC	20	5V