Dual Graphics Clock Generator

Features

- Generates 16 preset video clock frequencies, including one external frequency input, and 8 preset memory clock frequencies
- Built-in power supply conditioning circuitry provides excellent jitter performance and eliminates the need for external VDD dropping resistor
- Requires only one external 0.1 µF decoupling capacitor
- Supports VGA, Super-VGA, XGA™, and 8514 graphic standards
- Supports output frequencies up to 135 MHz
- CMOS technology in 20-pin PDIP and SOIC
- 5V or 3.3V supply. For specific details on the 3.3V version, please consult Chrontel.

Description

CH92C64 is a dual PLL clock generator designed for high performance applications, such as graphics systems based on VGA, Super-VGA, XGA™, and 8514 formats. CH92C64 also supports any application requiring multiple clocks, including, but not limited to, disk drives, CD-ROM systems, and modems.

The CH92C64 provides separate memory clock (MCLK) and video clock (VCLK) outputs. The reference frequency (14.318 MHz) is driven from an external frequency source such as the AT system bus clock.

CH92C64 has built-in power supply conditioning circuitry, which shields the internal circuitry from external power supply variations and maintains low-phase jitter in a noisy environment.

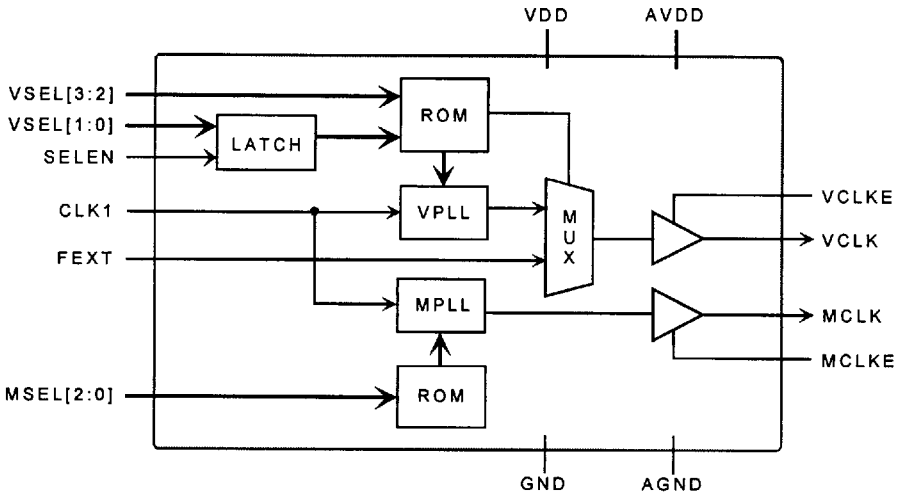

Figure 1: Block Diagram

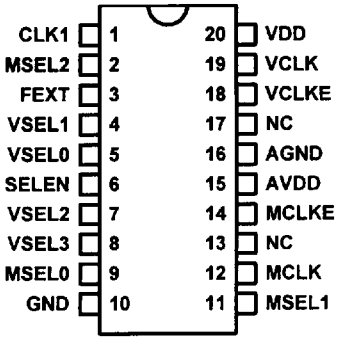

Figure 2: CH92C64

Table 1 • Pin Description

Pin	Type	Symbol	Description
1	In	CLK1	Reference (14.318 MHz) frequency input
2, 9, 11	In	MSEL2, MSEL0, MSEL1	Memory clock select inputs (internal pull-up)
3	In	FEXT	External frequency input (internal pull-down)
4, 5, 7, 8	In	VSEL1, VSEL0, VSEL2, VSEL3	Video clock select inputs (internal pull-up)
6	In	SELEN	VSEL0 and VSEL1 strobe input (rising edge)
10	Power	GND	Ground
12	Out	MCLK	Memory clock output
13, 17	—	NC	No connect, **MUST BE LEFT OPEN**
14	In	MCLKE	Memory clock output enable (internal pull-up)
15	Power	AVDD	Analog 5V supply
16	Power	AGND	Analog ground
18	In	VCLKE	Video clock output enable (internal pull-up)
19	Out	VCLK	Video clock output
20	Power	VDD	5V supply

Table 2 • Frequencies for CH92C64 (in MHz)

Video Clock

Video Select (VSEL)				VCLK
3	2	1	0	
0	0	0	0	30.0
0	0	0	1	77.25
0	0	1	0	FEXT **
0	0	1	1	80.0
0	1	0	0	31.5
0	1	0	1	36.0
0	1	1	0	75.0
0	1	1	1	50.0
1	0	0	0	40.0
1	0	0	1	50.0
1	0	1	0	32.0
1	0	1	1	44.9
1	1	0	0	25.18
1	1	0	1	28.322
1	1	1	0	65.0
1	1	1	1	36.0

Note: ** PLL remains locked at specified frequency

Memory Clock

Memory Select (MSEL)			MCLK
2	1	0	
0	0	0	33.0
0	0	1	49.218
0	1	0	60.0
0	1	1	30.5
1	0	0	41.612
1	0	1	37.5
1	1	0	36.0
1	1	1	44.296

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Table 3 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	–0.5 to +7.0	V
VIN	Input voltage on any pins with respect to GND	–0.5 to VDD +0.5	V
TSTOR	Storage temperature	–55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4 • DC Specifications (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 4mA	VDD – 0.4			V
VOH	Output high voltage	VDD = 4.75V, IOH = 8mA	2.4			V
VOL	Output low voltage	VDD = 4.75V, IOL = 8mA			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			5	20	µA
ILK	Input leakage current		–10		10	µA
IDD	Operating current	VDD = 5V VCLK = 28MHz, No load MCLK = 44MHz, No load		38	45	mA
IDD	Operating current	VDD = 5V VCLK = 80MHz, No load MCLK = 44MHz, No load		46	53	mA
CIN	Input pin capacitance	Fc = 1MHz			8	pF
COUT	Output pin capacitance	Fc = 1MHz			12	pF

Table 5 • AC Specifications (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ±5%, CL = 15pF)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FIN	Reference frequency input			14.318		MHz
TSU	Setup time, data to select enable		20			ns
THOLD	Hold time, select enable to data		10			ns
TSELEN	Select enable pulse width		20			ns
TDELAY	Prop delay for FEXT to VCLK				20	ns
VCLK	Video clock frequency		8		80	MHz
MCLK	Memory clock frequency		8		80	MHz
TRI, TFI	FIN rise / fall time	Duty Cycle: 42.5% to 57.5%			10	ns
TR	VCLK and MCLK rise time	0.8V – 2.0V 0.3VDD – 0.7VDD		1.0 1.6	1.4 2.5	ns ns
TF	VCLK and MCLK fall time	0.8V – 2.0V 0.3VDD – 0.7VDD		1.0 1.6	1.4 2.5	ns ns
TDC	Output clock duty cycle	@1.4V switch point @VDD / 2 switch point, CL = 15pF	50 45		60 55	% %

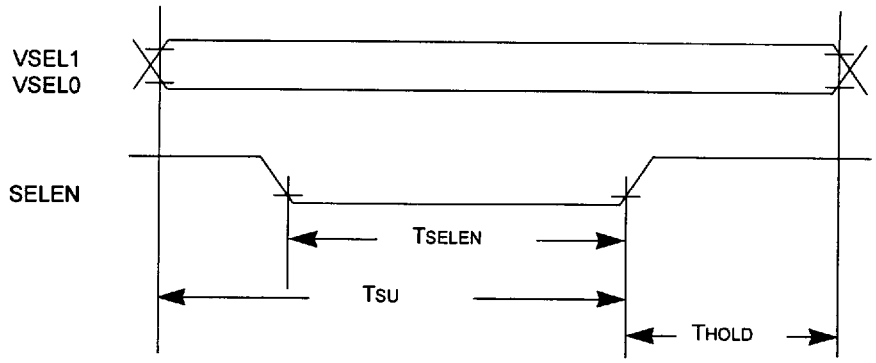

Figure 3: Select Enable Timing Diagram

Layout Considerations

To minimize phase noise and maximize performance, the following layout guidelines are recommended:

- Place all power supply bypass capacitors in close proximity to their respective power pins
- Use a ground plane to connect GND, AGND, and all external component grounds
- Avoid running any signal lines through the synthesizer section of the board

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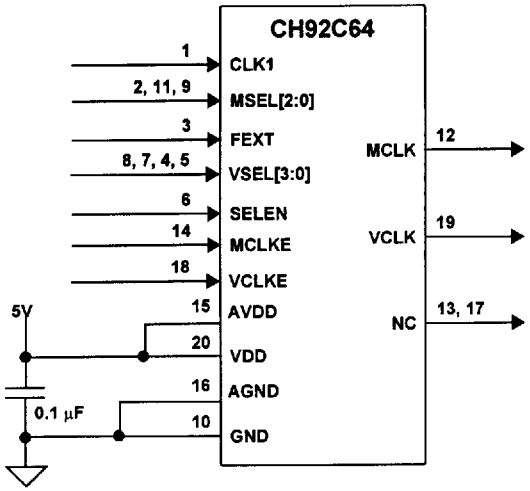

Figure 4: Application Schematic

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH92C64-N	300 mil PDIP	20	5V
CH92C64-S	300 mil SOIC	20	5V