

9388929 V T C INC

99D 01134 D

T-52-31

V54AC645

V74AC645

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

FEATURES

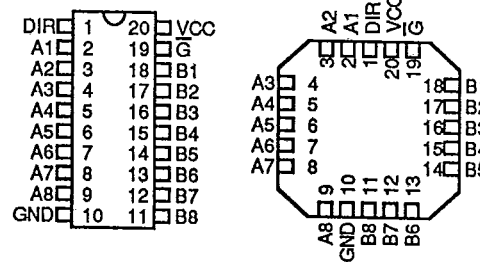
- High Speed, 4ns Typical
- I_{OL}/I_{OH} =24mA Commercial,
24mA Military
- Low Input Current, 1 μ A Max
- Fully Specified: 5V $\pm$ 10% Power Supply, Min and Max over Temperature

FUNCTIONAL DESCRIPTION

These 8-bit bus transceivers allow asynchronous two way communication between data buses A and B. The DIR signal controls the direction of data flow. When DIR is high, data flows from A to B. When DIR is low, data flows from B to A. The $\bar{G}$ signal enables the transceiver.

These parts are designed to interface with 3-state buses and I/O ports.

CONNECTION DIAGRAMS

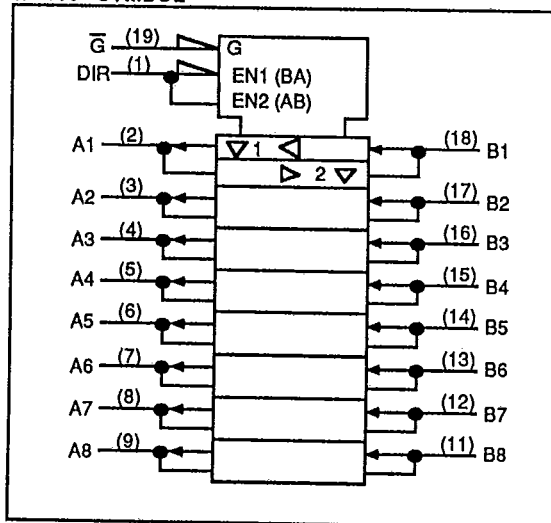


DIP and SOIC

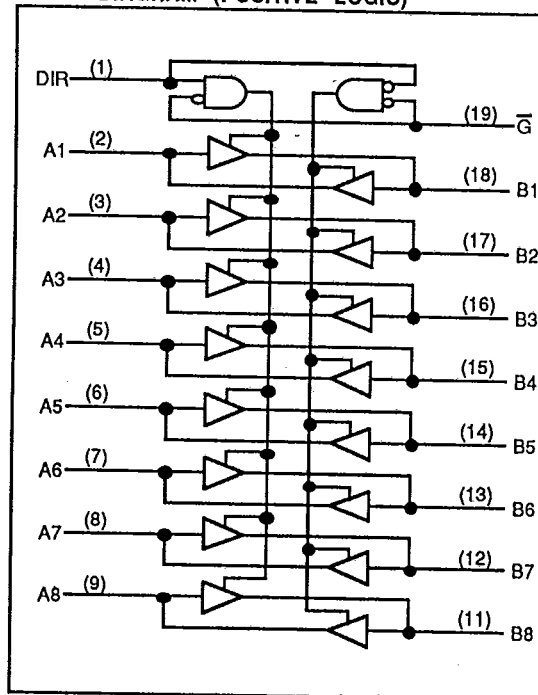
LCC

Top View

LOGIC SYMBOL



LOGIC DIAGRAM (POSITIVE LOGIC)



FUNCTION TABLE

ENABLE	DIRECTION CONTROL	OPERATION
$\bar{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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T-52-3/

AC CHARACTERISTICS

 $V_{CC} = 5V \pm 10\%$; $C_L = 50pF$; Input $t_r, t_f \leq 3nsec$

SYMBOL	PARAMETER	Min	25°C Typ	25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay	1	4	6	7	8	ns	3
t_{PHL}	A to B or B to A	1	4	6	7	8	ns	3
t_{PZH}	Prop. Delay	1	6	8	9.5	10.5	ns	2
t_{PZL}	Output Enable to B or A	1	6	8	9	10	ns	2
t_{PHZ}	Prop. Delay	1	6	8	9	10	ns	2
t_{PLZ}	Output Disable to B or A	1	7	9	10	11	ns	2

AC CHARACTERISTICS

 $V_{CC} = 3.3V \pm 0.3V$; $C_L = 50pF$; Input $t_r, t_f \leq 3nsec$

SYMBOL	PARAMETER	Min	25°C Typ	25°C Max	85°C Max	125°C Max	UNITS	
t_{PLH}	Prop. Delay						ns	
t_{PHL}	A to B or B to A						ns	
t_{PZH}	Prop. Delay						ns	
t_{PZL}	Output Enable to B or A						ns	
t_{PHZ}	Prop. Delay						ns	
t_{PLZ}	Output Disable to B or A						ns	

C_{IN}	Input Capacitance	4					pF	
C_{OUT}	Output Capacitance (Outputs Off)	10					pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)	35					pF	

* $P_T = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation when $n = \#$ of buffersAC FAMILY
DATA SHEETS