T-52-31

V54AC862
V74AC862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES

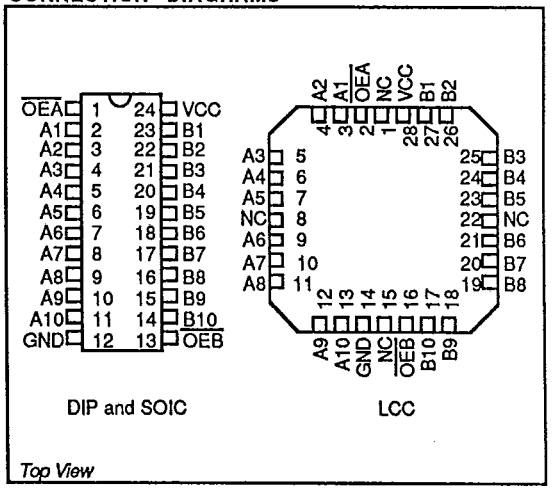
- High Speed, 4.5ns Typical
- I_{OL}/I_{OH} = 24mA Commercial, 24mA Military
- Low Input Current, 1μA Max
- Fully Specified: 5V ± 10% Power Supply, Min and Max over Temperature

FUNCTIONAL DESCRIPTION

These are 10-bit inverting transceivers with control enables $\overline{OEA}$ and $\overline{OEB}$. When $\overline{OEA}$ is low, the inverse of the data on bus B is transmitted to bus A. When $\overline{OEB}$ is low, the inverse of the data on bus A is transmitted to bus B. The ten bits provide extra bits for parity, clock, or control signals on the bus by just using a simple component.

These parts are designed to interface with 3-state buses and I/O ports. They are ideal for interfacing with high capacitance, low impedance loads on both buses A and B.

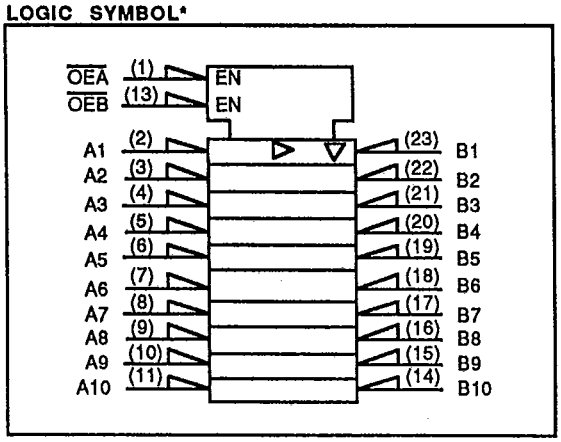
CONNECTION DIAGRAMS



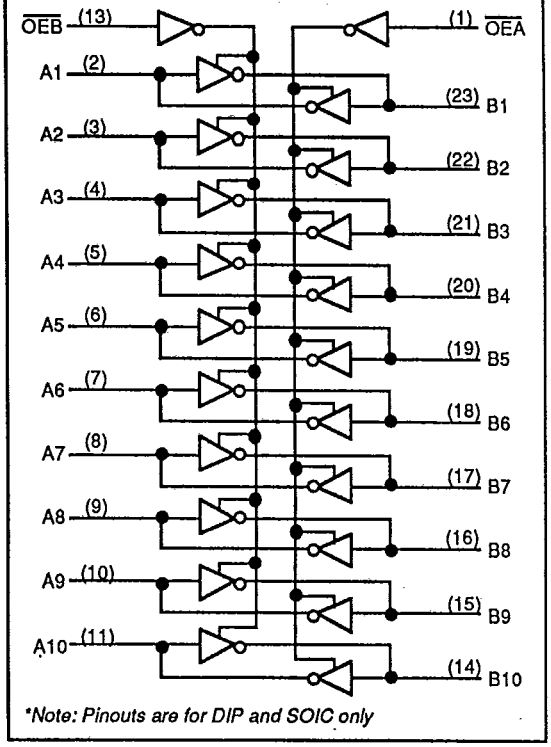
DIP and SOIC LCC

Top View

LOGIC SYMBOL*



LOGIC DIAGRAM (POSITIVE LOGIC)*



*Note: Pinouts are for DIP and SOIC only

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{OEB}$	$\overline{OEA}$	
H	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	H	Isolation
L	L	Latch

AC FAMILY DATA SHEETS

AC CHARACTERISTICS V_{CC} = 5V ±10%; C_L = 50pF; Input t_r, $t_f \leq$ 3nsec

SYMBOL	PARAMETER	Min	25°C Typ	25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	1	4.5	6.5	7.5	8.5	ns	3
t_{PHL}		1	4.5	6.5	7.5	8.5	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	1	7	11	13	14	ns	2
t_{PZL}		1	7	11	13	14	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	1	7	10	12	13	ns	2
t_{PLZ}		1	7	10	12	13	ns	2

AC CHARACTERISTICS V_{CC} = 3.3V ± 0.3V; C_L = 50pF; Input t_r, $t_f \leq$ 3nsec

SYMBOL	PARAMETER	Min	25°C Typ	25°C Max	85°C Max	125°C Max	UNITS	
t_{PLH}	Prop. Delay A to B or B to A						ns	
t_{PHL}							ns	
t_{PZH}	Prop. Delay Output Enable to A or B						ns	
t_{PZL}							ns	
t_{PHZ}	Prop. Delay Output Disable to A or B						ns	
t_{PLZ}							ns	

C_{IN}	Input Capacitance	4				pF	
C_{OUT}	Output Capacitance (Outputs Off)	10				pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)	35				pF	

*$P_T = (C_{PD}+C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation when n = # of buffers

AC FAMILY DATA SHEETS