T-52-31

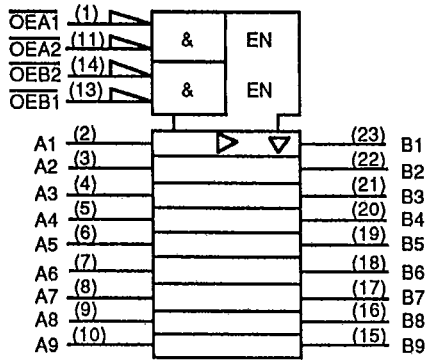
V54AC863
V74AC863
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

FEATURES
- High Speed, 5ns Typical
- I_{OL}/I_{OH} = 24mA Commercial, 24mA Military
- Low Input Current, 1µA Max
- Fully Specified: 5V ± 10% Power Supply, Min and Max over Temperature

FUNCTIONAL DESCRIPTION
These are 9-bit transceivers with dual-control enables $\overline{OEA1}$, $\overline{OEA2}$ and $\overline{OEB1}$, $\overline{OEB2}$. When both enables are low, the transceivers conduct from one port to the other. The nine bits provide the capability to transmit parity on the system buses among other possible uses.

These parts are designed to interface with 3-state buses and I/O ports. They are ideal for interfacing with high capacitance, low impedance loads on both buses A and B.

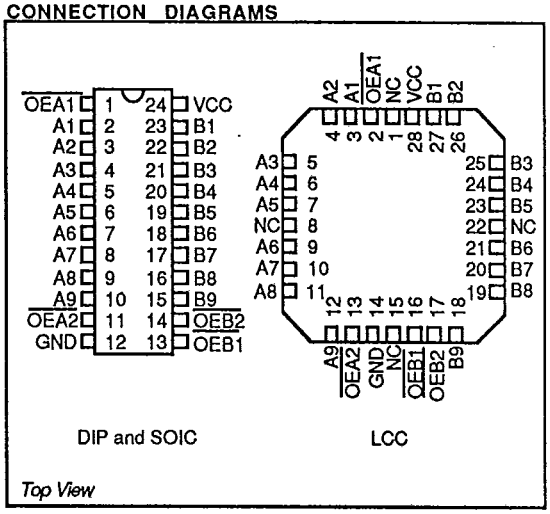
LOGIC SYMBOL*



FUNCTION TABLE

ENABLE INPUTS				OPERATION
$\overline{OEB1}$	$\overline{OEB2}$	$\overline{OEA1}$	$\overline{OEA2}$	
H	X	L	L	B data to A bus
X	H	L	L	B data to A bus
L	L	H	X	A data to B bus
L	L	X	H	A data to B bus
H	X	H	X	Isolation
X	H	X	H	Isolation
L	L	L	L	Latch

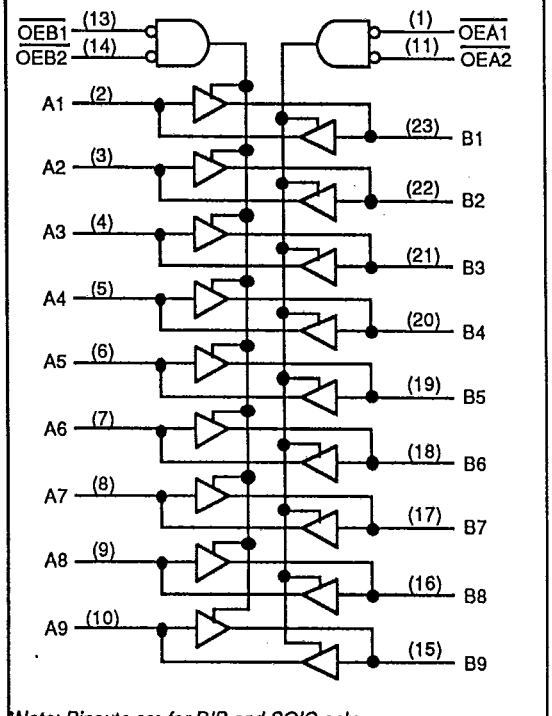
CONNECTION DIAGRAMS



DIP and SOIC LCC

Top View

LOGIC DIAGRAM (POSITIVE LOGIC)*



Note: Pinouts are for DIP and SOIC only

AC FAMILY DATA SHEETS

AC CHARACTERISTICS V_{CC} = 5V ±10%; C_L = 50pF; Input t_r, $t_f \leq$ 3nsec

SYMBOL	PARAMETER	Min	25°C Typ	25°C Max	85°C Max	125°C Max	UNITS	FIGURE
t_{PLH}	Prop. Delay A to B or B to A	1	5	7	8	9	ns	3
t_{PHL}		1	5	7	8	9	ns	3
t_{PZH}	Prop. Delay Output Enable to A or B	1	7	9.5	11	12	ns	2
t_{PZL}		1	7	9.5	11	12	ns	2
t_{PHZ}	Prop. Delay Output Disable to A or B	1	7	9	10	11	ns	2
t_{PLZ}		1	7	9	10	11	ns	2

AC CHARACTERISTICS V_{CC} = 3.3V ± 0.3V; C_L = 50pF; Input t_r, $t_f \leq$ 3nsec

SYMBOL	PARAMETER	Min	25°C Typ	25°C Max	85°C Max	125°C Max	UNITS	
t_{PLH}	Prop. Delay A to B or B to A						ns	
t_{PHL}							ns	
t_{PZH}	Prop. Delay Output Enable to A or B						ns	
t_{PZL}							ns	
t_{PHZ}	Prop. Delay Output Disable to A or B						ns	
t_{PLZ}							ns	

C_{IN}	Input Capacitance	4				pF	
C_{OUT}	Output Capacitance (Outputs Off)	10				pF	
C_{PD}	Power Dissipation Capacitance* (per buffer)	35				pF	

*$P_T = (C_{PD}+C_L) \cdot V_{CC}^2 \cdot f \cdot n + I_{CC} \cdot V_{CC}$, Total power dissipation when n = # of buffers

AC FAMILY DATA SHEETS