

**VA701****LOW-NOISE PRECISION  
OPERATIONAL AMPLIFIER****PRELIMINARY INFORMATION****FEATURES**

- Low Noise: 3.0 nV/V $\sqrt{\text{Hz}}$  at 1KHz
- High Speed: 10V/ $\mu\text{s}$  Slew Rate
- 30MHz Gain Bandwidth
- Fast Settling: 10 $\mu\text{s}$  to 0.01%
- Low Offset Voltage: 10 $\mu\text{V}$
- Large Output Current:  $\pm 50\text{mA}$
- High Gain: 5 million
- Large Output Swing:  $\pm 4\text{V}$
- Large Input Common Mode Range:  $\pm 3.5\text{V}$

**DESCRIPTION**

The VA701 is a precision operational amplifier with performance parameters similar to that of the industry-standard OP-27 but with design architecture optimized for performance with  $\pm 5\text{V}$  supplies. For example, the output voltage swing is typically  $\pm 4\text{V}$  while input common mode range is  $\pm 3.5\text{V}$ .

The low offset voltage of  $25\mu\text{V}$  and offset current of  $50\text{nA}$  maximum makes the amplifier ideal for precision instrumentation applications. In addition, the low noise of  $3\text{nV}/\sqrt{\text{Hz}}$  insures that amplification accuracy is maintained with low level input signals. The device is available in 8-pin DIP, SOIC, metal can (TO-99), and die package configuration with the industry-standard operational amplifier pinout (except SOIC).

**ABSOLUTE MAXIMUM RATINGS**

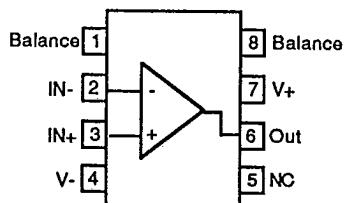
Supply Voltages .....	$\pm 6.5\text{V}$
Common Mode Input Voltage .....	$\pm 5\text{V}$
Differential Input Voltage .....	$\pm 0.7\text{V}$
Power Dissipation (Note 1, 2) .....	450mW
Operating Temperature Range:	
Commercial .....	0° to 70°C
Military .....	-55° to +125°C
Storage Temperature Range .....	-65° to +150°C
Lead Temperature (Soldering to 60 Sec) .....	300°C

Note 1: Power derating above  $T_A = 70^\circ\text{C}$  to be based on a maximum junction temperature of  $150^\circ\text{C}$  and the following thermal resistance factors:

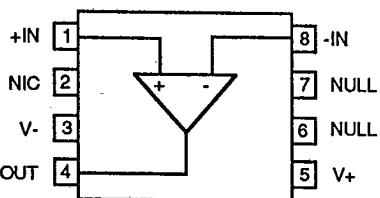
PACKAGE	$\theta_{JC}$ ( $^\circ\text{C/W}$ )	$\theta_{JA}$ ( $^\circ\text{C/W}$ )
DIP	75	180
SOIC	115	180
TO-99	115	250

Note 2: Continuous short circuit protection is allowed to the following case and ambient temperatures:

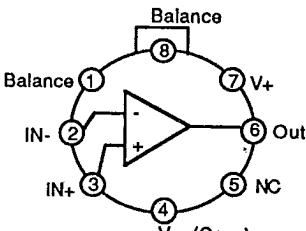
PACKAGE	$T_C$ ( $^\circ\text{C}$ )	$T_A$ ( $^\circ\text{C}$ )
DIP	110	70
SOIC	95	70
TO-99	95	30

**CONNECTION DIAGRAMS****Dual-In-Line**

Top View

**SOIC Package**

Top View

**Metal Can Package**

Top View

**PACKAGE TYPES AVAILABLE**

- 8-Pin Plastic DIP
- 8-Pin CERDIP
- 8-Pin SOIC
- 8-Pin Metal Can, TO-99

9388929 V T C INC

99D 01219 D

VA701

T-79-06-10

ELECTRICAL CHARACTERISTICS ( $V_S = \pm 15V$ ,  $T_A = 25^\circ C$  unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	VA701J			VA701K			VA701L			VA701S			UNITS
			MIN	Typ	MAX										
Input Offset Voltage	$V_{OS}$		100	400		50	100		10	25		10	25		$\mu V$
		$0^\circ \leq T_A \leq 70^\circ C$	200	600		65	140		15	40					
		$-55^\circ \leq T_A \leq +125^\circ C$		4								25	50		
Input Offset Voltage Drift		$0^\circ \leq T_A \leq 70^\circ C$	2	4		1	2			0.6					$\mu V/\text{ }^\circ C$
		$-55^\circ \leq T_A \leq +125^\circ C$													
Long Term $V_{OS}$ Stability	$V_{OS}/\text{Time}$	(Notes 1, 2)		3			3			1			1		$\mu V/\text{Mo}$
Input Offset Current	$I_{OS}$			150			100			50			50		$nA$
		$0^\circ \leq T_A \leq 70^\circ C$		200			150			100					
		$-55^\circ \leq T_A \leq +125^\circ C$											100		
Input Offset Current Drift		$0^\circ \leq T_A \leq 70^\circ C$	150			100			100						$pA/\text{ }^\circ C$
		$-55^\circ \leq T_A \leq +125^\circ C$											300		
Input Bias Current	$I_B$		50	200		25	100		10	40		10	40		$nA$
		$0^\circ \leq T_A \leq 70^\circ C$		300			150			60					
		$-55^\circ \leq T_A \leq +125^\circ C$											75		
Input Differential Resistance (Note 3)	$R_{IN}$				0.8			0.8			1.5			1.5	$M\Omega$
Input Common Mode Resistance	$R_{INCM}$			2			2			3			3		$G\Omega$
Large Signal Voltage Gain (Note 3)	$A_V$	$R_L > 2K\Omega$ $V_{OUT} = \pm 3.5V$	700	6,000		700	6,000		1,000	6,000		1,000	6,000		$V/mV$
Input Common Mode Range	$V_{CM}$		$\pm 3.5$			$\pm 3.5$			$\pm 3.5$			$\pm 3.5$			$V$
Output Voltage Swing	$V_{OUT}$	$R_L = 2K\Omega$	$\pm 3.5$	$\pm 4.0$		$V$									
		$R_L = 51\Omega$	$\pm 2.5$												
Power Supply Current	$I_S$			8	12		8	12		8	12		8	12	$mA$
Positive Current Limit	$+I_{SC}$		60		180	60		180	60		180	60		180	$mA$
Negative Current Limit	$-I_{SC}$		60		180	60		180	60		180	60		180	$mA$
Common-Mode Rejection Ratio	$CMRR$	$V_{CM} = \pm 3.5$	100			100			114			114			$dB$
Power-Supply Rejection Ratio	$PSRR$	$\Delta V_{PS} = \pm 1.0V$	94			94			100			100			$dB$

LSP FAMILY DATA SHEETS

Notes:

1. Long term input offset voltage stability refers to the average trend line of  $V_{OS}$  vs Time over extend periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 days are typically  $2.5\mu V$ .
2. Sample tested only.
3. Not tested, guaranteed by design.

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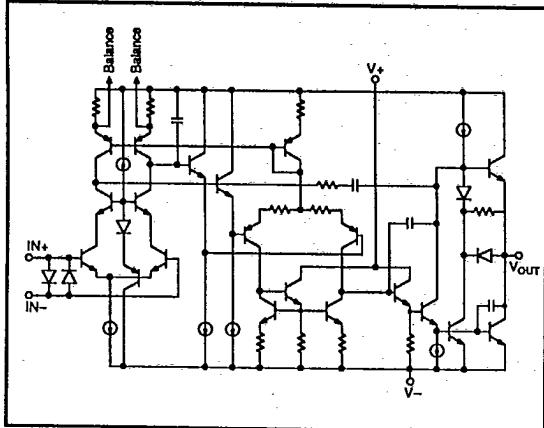
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AC and NOISE CHARACTERISTICS ( $V_S = \pm 5V$ ,  $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	VA701J			VA701K			VA701L			VA701S			UNITS
			MIN	Typ	MAX										
Input Noise Voltage	$e_{np-p}$	$f = 10\text{Hz}$ (Note 1)		0.25	0.75		0.18	0.36		0.18	0.36		0.18	0.36	$\mu\text{Vp-p}$
Input Noise Voltage Density	$e_n$	$f = 1\text{KHz}$ (Note 1)		3.8	4.5		3.0	3.8		3.0	3.8		3.0	3.8	$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current Density	$i_n$	$f = 1\text{KHz}$		1.0			1.0			1.0			1.0		$\text{pA}/\sqrt{\text{Hz}}$
Slew Rate	SR		6.0	10		6.0	10		6.0	10		6.0	10		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBW	$f = 100\text{KHz}$	30			30			30			30			MHz
Settling Time	$t_s$	$\pm 3.5\text{V Step}$	10			10			10			10			$\mu\text{s}$

Note 1: Sample tested only.

## SIMPLIFIED SCHEMATIC



T-79-06-10

WAFER ELECTRICAL CHARACTERISTICS ( $V_S = \pm 5V$ ,  $T_A = 25^\circ C$  unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	VA701X			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	$V_{os}$				25	$\mu V$
Input Offset Current	$I_{os}$				50	nA
Input Bias Current	$I_B$				40	nA
Input Common Mode Range	$V_{CM}$		$\pm 3.5$			V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 3.5V$	114			dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{ps} = \pm 1.0V$	100			dB
Large-Signal Voltage Gain	$A_V$	$R_L \geq 2K\Omega$ $V_{OUT} = \pm 3.5V$	1000	6,000		V/mV
Output Voltage Swing	$V_{OUT}$	$R_L = 2K\Omega$ $R_L = 51\Omega$	$\pm 3.5$ $\pm 2.5$			V
Power Supply Current	$I_s$				12	mA
Gain Bandwidth	GBW			30		MHz
Slew Rate	SR	$R_L \geq 2K\Omega$		10		V/ $\mu s$
Settling Time	$t_s$	$\pm 3.5V$ step		10		$\mu s$
Input Noise Voltage Density	$e_N$	$f = 1KHz$		3.0		$nV/\sqrt{Hz}$
Input Noise Current Density	$I_N$	$f = 1KHz$		1.0		$pA/\sqrt{Hz}$

## DICE POLICY

## Electrical Characteristics

Each die is electrically tested to the commercial or military grade DC parameters to guard band limits at  $25^\circ C$  to guarantee operation over the full temperature range.

## Quality Assurance

All dice are 100% visually inspected to the requirement of MIL-STD-883C, Method 2010.2, Condition 3.

All dice are glass passivated with only the bonding pads exposed to provide scratch protection.

All dice are provided with gold backing.

## DIE

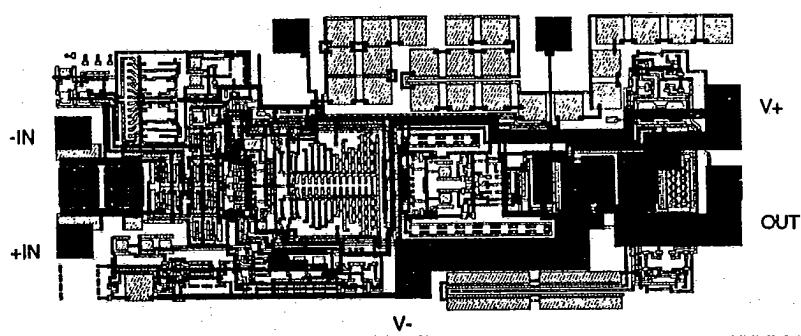
## Shipping Packages/Order Information

All dice are packaged in die crates with individual compartments which prevent damage to the die during shipping. Minimum order for dice is 100, supplied only in multiples of 100.

LSP FAMILY DATA  
SHEETS

NULL (BAL)

NULL (BAL)



Die size = 0.086 x 0.042 inch (3612 sq. mils)  
= 2.18 x 1.07 mm (2.33 sq. mm)