T-79-06-10

VTC Incorporated

VA705

HIGH-SPEED PRECISION OPERATIONAL AMPLIFIER

DISCONTINUED

FEATURES

- Fast Settling Time: ±0.1% in 250ns
- High Slew Rate: 35V/µs
- Wide Gain Bandwidth: 25MHz
- Low Offset Voltage: 1mV
- Low Offset Current: 15nA
- Ease of Use: Internally Compensated, Unity Gain Stable at C_L = 50pF, Phase Margin = 58°
- Large Output Current: ±50mA
- Wide Input Voltage Range: Within 1.5V of V+ and 0.5V of V-
- Short Circuit Protection

DESCRIPTION

The VA705 is a general purpose operational amplifier which combines the attributes of high speed with low offset voltage and current. This combination, along with a high open-loop gain of 20,000V/V, allows the amplifier to fit into video processing, as well as signal conditioning applications where accuracy is at a premium. The same processing innovations which permit the high speed/low offset combination also allow very high output currents capable of driving large capacitive loads at high speeds.

The VA705 is internally compensated for stable operation even when driving capacitive loads in excess of 50pF. The wide gain bandwidth of 25MHz and 35V/µs slew rate results in ±0.1% settling times of 250ns, which makes the amplifier ideal for fast data conversion systems.

The high output current capability of ±50mA allows the amplifier to drive terminated transmission lines of 50Ω with amplitudes of 5V peak-to-peak.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6V
Differential Input Voltage	±9V
Common Mode Input Voltage	$\|V_S\|$ -0.5V
Power Dissipation (Note 1)	450mW
Output Short Circuit Current Duration (Note 2)	Indefinite
Operating Temperature Range:	
Commercial (705 J, K, L)	0° to 70°C
Storage Temperature Range	-65° to +150°C
Lead Temperature (Soldering to 60 Sec.)	300°C

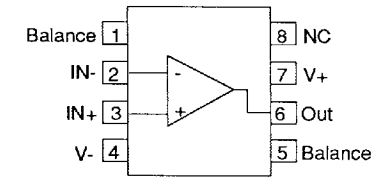
Note 1: Power derating above T_A = 70°C to be based on a maximum junction temperature of 150°C and the following thermal resistance factors:

Note 2: Continuous short circuit protection is allowed to the following case and ambient temperatures:

PKGE.	θ_{JC} (°C/W)	θ_{JA} (°C/W)	T_C (°C)	T_A (°C)
DIP	75	180	110	70
SOIC	115	180	95	70

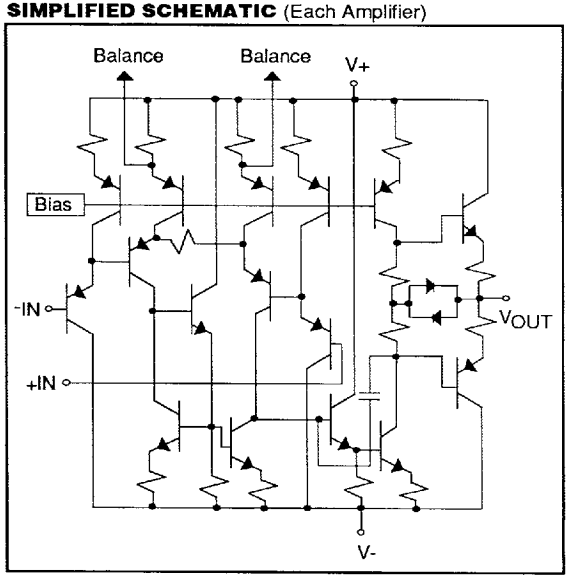
CONNECTION DIAGRAM

8-Lead Dual In-Line/SOIC Package



Top View

SIMPLIFIED SCHEMATIC (Each Amplifier)



PACKAGE TYPES AVAILABLE

- 8-Pin Plastic DIP
- 8-Pin CERDIP
- 8-Pin SOIC

4036 A-13

ELECTRICAL CHARACTERISTICS (V_S= ±5V, T_A= 25° C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	VA705J			VA705K			VA705L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			6	10		3	5		1	2	mV
T_{Min} to T_{Max}		0° ≤T_A≤70°C		9	16		5	9		2	5	
Average Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	0° ≤T_A≤70°C		±20			±20			±20		µV/°C
Input Bias Current	I_B			650	1100		650	900		650	900	nA
Input Offset Current	I_{OS}			35	120		25	50		15	25	nA
T_{Min} to T_{Max}		0° ≤T_A≤70°C		70	200		50	100		25	60	
Input Common Mode Range	V_{CM}		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		V
Differential Input Resistance	R_{IND}	(Note 1)	3	10		3	10		3	10		MΩ
Common Mode Input Resistance	R_{INC}	(Note 1)	4	8		4	8		4	8		MΩ
Differential Input Capacitance	C_{IND}	(Note 1)		2						2		pF
Common Mode Input Capacitance	C_{INC}	(Note 1)		3			3			3		pF
Input Voltage Noise	e_N	BW=10Hz to 100KHz		12			12			12		µVRMS
Open Loop Voltage Gain	A_V	V_{OUT} =±3V R_L =2kΩ	2	5		4	10		10	20		V/mV
Output Voltage Swing	V_{OUT}	R_L =2kΩ	±3.5	+4 -4.2		±3.5	+4 -4.2		±3.5	+4 -4.2		V
		R_L =51Ω	±2.0	±2.4		±2.5	±2.7		±2.5	±2.7		
Power Supply Current	I_S			7	10		7	10		7	10	mA
Common Mode Rejection Ratio	CMRR	V_{CM} =±2V	60	70		60	70		60	70		dB
Power Supply Rejection Ratio	PSRR	ΔV_{PS} =±0.5V	60	66		60	66		60	66		dB
Slew Rate	SR	10-90%of Leading Edge (Figure 1a,b)	30	35		30	35		30	35		V/µs
Settling Time	t_S	To ±0.1%(±4mV) of Final Value (Figure 1a,b) (Note 1)		250	300		250	300		250	300	ns
Gain Bandwidth Product	GBW			25			25			25		MHz
Small Signal Rise/Fall Time	t_r /t_f	e_O = ±50mV 10-90% (Figure 1c)		7			7			7		ns
Full Power Bandwidth	BW_{FP}	R_L = 2kΩ C_L = 50pF V_{OUT} = 6Vp-p		1.8			1.8			1.8		MHz

Notes: 1. Not tested, guaranteed by design

DIE INFORMATION

WAFER TEST LIMITS

V_S = ±5V, T_A = 25° C unless otherwise stated

PARAMETER	SYM	CONDITIONS	VA705XS LIMIT	UNITS
Input Offset Voltage	V_{OS}		5	mV Max
Input Bias Current	I_B		1100	nA Max
Input Offset Current	I_{OS}		25	nA Max
Input Common Mode Range	V_{CM}		+3 -4	V Min
Open Loop Voltage Gain	A_V	V_{OUT} = ±3V R_L = 2k	4	V/mV Min
Output Voltage Swing	V_{OUT}	R_L = 2KΩ	±3.5	V Min
		R_L = 51Ω	±2.5	
Power Supply Current	I_S		10	mA Max
Common Mode Rejection Ratio	CMRR	V_{CM} = ±2V	60	dB Min
Power Supply Rejection Ratio	PSRR	ΔV_{PS} = ±0.5V	60	dB Min
Slew Rate	SR	10-90% of Leading Edge (Figure 1a,b)	30	V/μs Min

TYPICAL ELECTRICAL CHARACTERISTICS

V_S = ±5V, T_A = 25° C unless otherwise stated

PARAMETER	SYM	CONDITIONS	VA705XS TYPICAL	UNITS
Input Offset Voltage T_{Min} to T_{Max}	V_{OS}		6	mV
Input Offset Current T_{Min} to T_{Max}	I_{OS}		35	nA
Settling Time	t_S	To ±0.1% of Final Value (Figure 1a,b)	250	ns
Gain Bandwidth Product	GBW		25	MHz
Small Signal Rise/Fall Time	t_r / t_f	e_O = ±50mV 10-90% (Figure 1c)	7	ns
Full Power Bandwidth	BW_{FP}	R_L = 2kΩ C_L = 50pf V_{OUT} = 6V p-p	1.8	MHz

DICE POLICY

Electrical Characteristics

Each die is electrically tested to the commercial or military grade DC parameters to guard band limits at 25°C to guarantee operation over the full temperature range.

Quality Assurance

All dice are 100% visually inspected to the requirement of MIL-STD-883C, Method 2010.2, Condition 3.

All dice are glass passivated with only the bonding pads exposed to provide scratch protection.

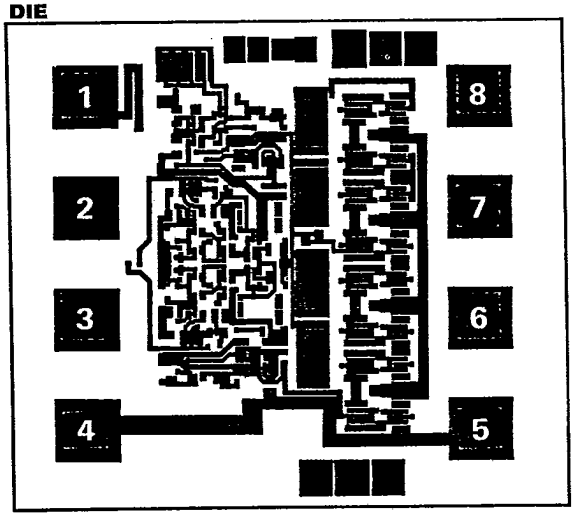
All dice are provided with gold backing.

Shipping Packages/Order Information

All dice are packaged in die crates with individual compartments which prevent damage to the die during shipping. The individual cavity size of the die crate is such that maximum rotation of the die within the cavity is < 45°.

Minimum order for dice is 100, supplied only in multiples of 100.

DIE



Die size = 0.035 x 0.035 inch (1225 sq. mils)
0.89 x 0.89 mm (0.79 sq. mm)
Shipped in die crates.

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Figure 1a: Slew Rate and Settling Time Test Circuit

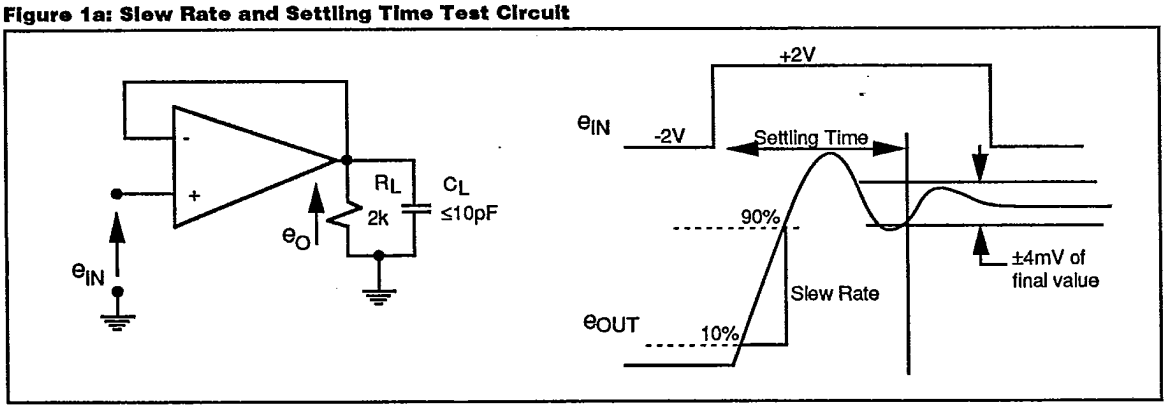


Figure 1b: Large Signal Response

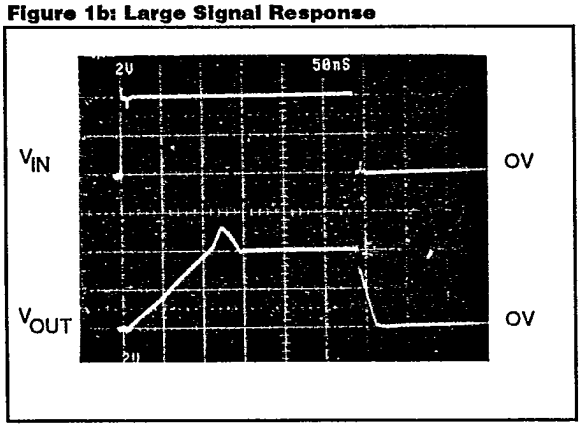
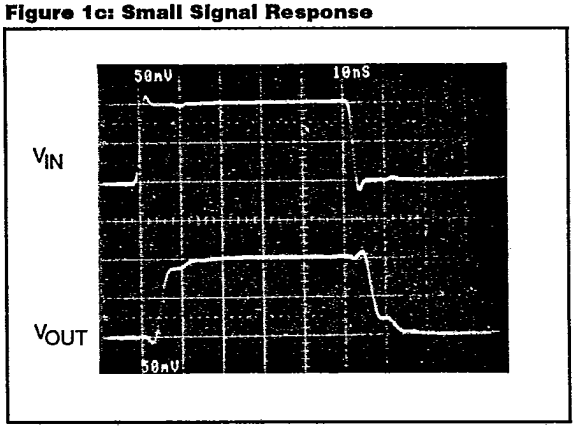
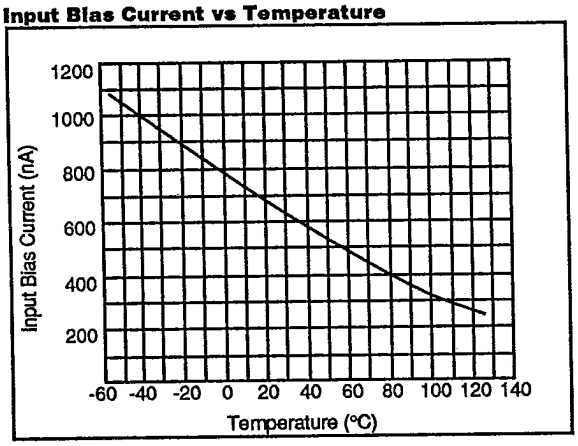


Figure 1c: Small Signal Response

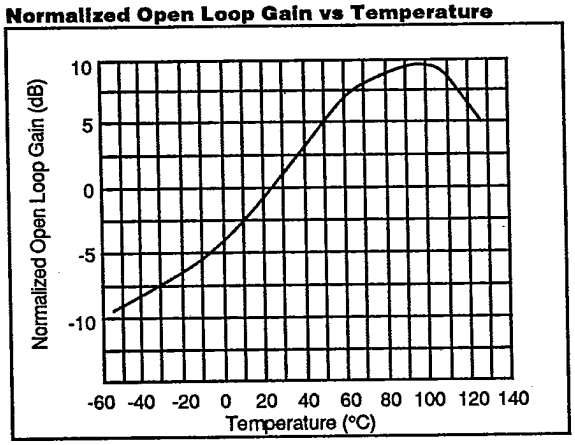


TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A= 25°C unless otherwise stated)

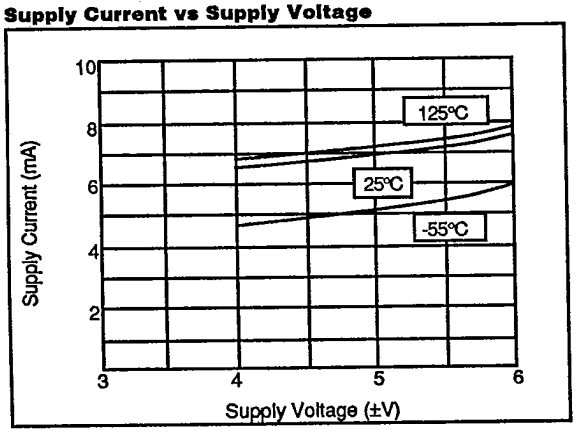
Input Bias Current vs Temperature



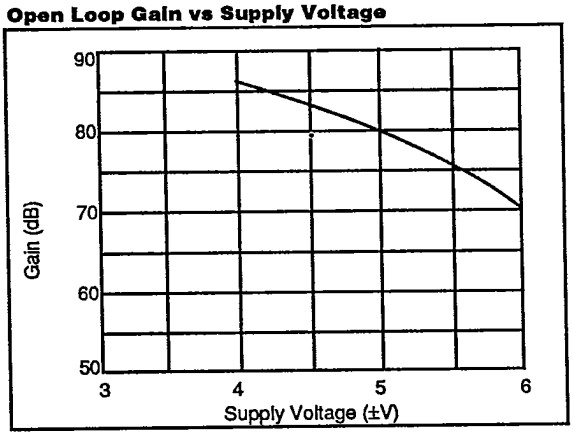
Normalized Open Loop Gain vs Temperature



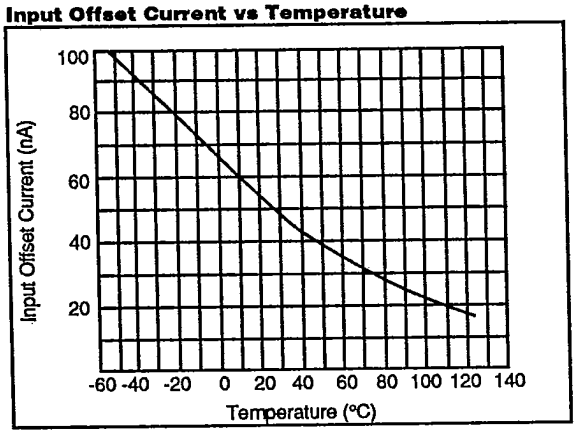
Supply Current vs Supply Voltage



Open Loop Gain vs Supply Voltage

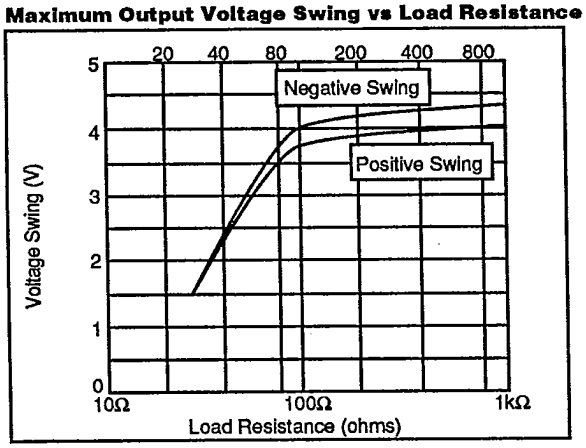


Input Offset Current vs Temperature

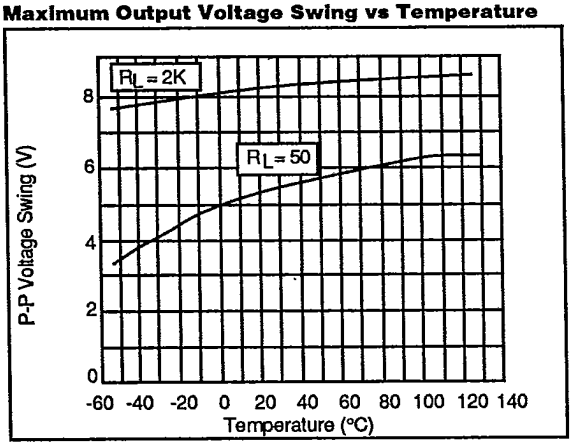


TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A = 25°C unless otherwise stated)

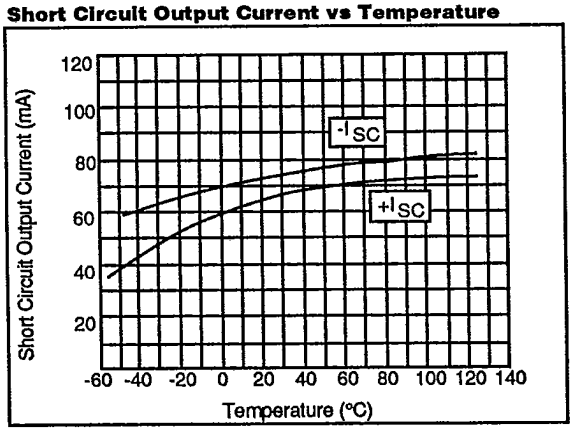
Maximum Output Voltage Swing vs Load Resistance



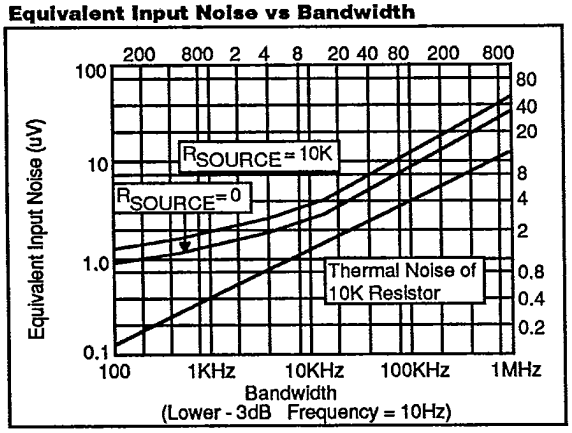
Maximum Output Voltage Swing vs Temperature



Short Circuit Output Current vs Temperature

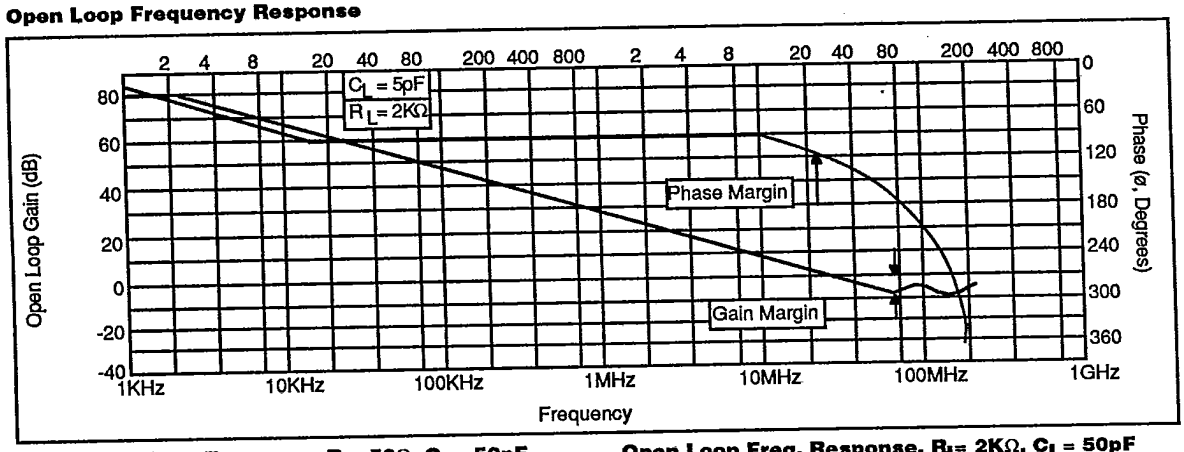


Equivalent Input Noise vs Bandwidth

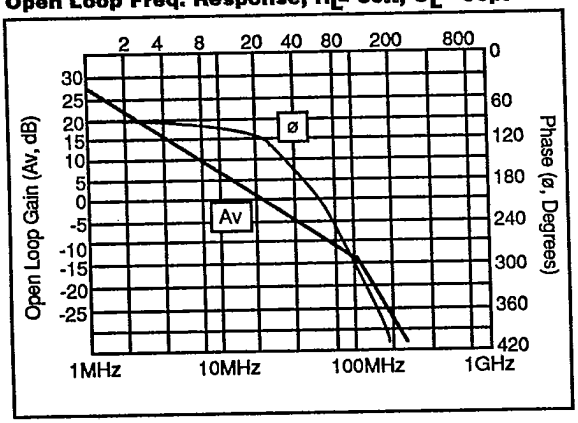


TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A= 25°C unless otherwise stated)

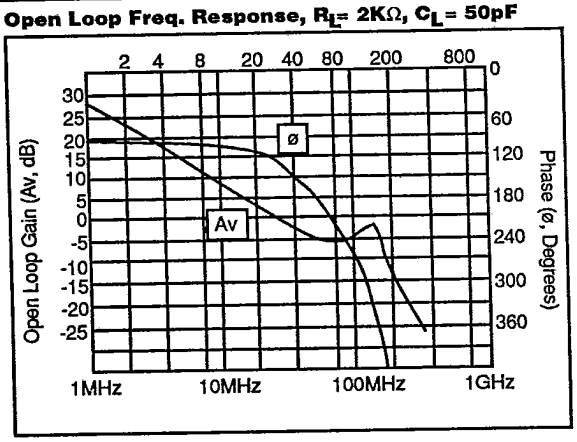
Open Loop Frequency Response



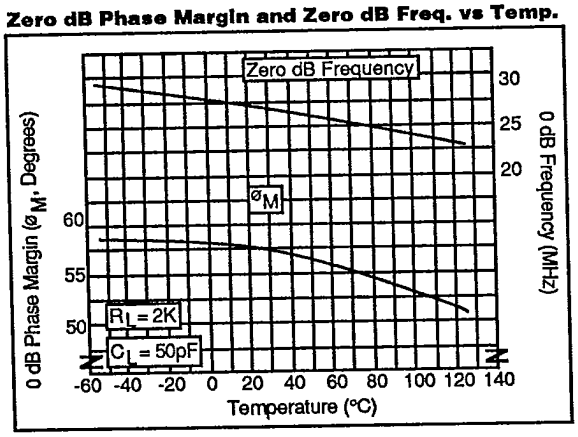
Open Loop Freq. Response, R_L= 50Ω, C_L= 50pF



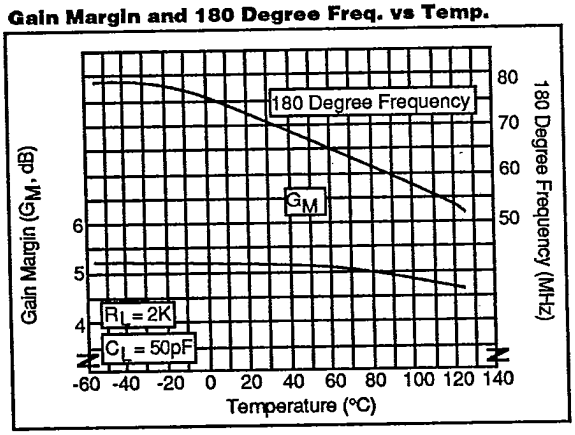
Open Loop Freq. Response, R_L= 2KΩ, C_L= 50pF



Zero dB Phase Margin and Zero dB Freq. vs Temp.



Gain Margin and 180 Degree Freq. vs Temp.



APPLICATION INFORMATION

AC Characteristics

The 28MHz 0dB crossover point of the VA705 is achieved without feed-forward compensation, a technique which can produce long tails in the recovery characteristic. The single pole rolloff follows the classic 20dB/decade slope to frequencies approaching 50MHz. The phase margin of 58°, even with a capacitive load of 50pF, gives stable and predictable performance down to unity gain follower configurations.

At frequencies beyond 50MHz, the 20dB/decade slope is disturbed by an output stage zero, the damping factor of which is dependent upon the load capacitor. This results in loss of gain margin (gain at loop phase = 360°) at frequencies of 70 to 100MHz which at a gain margin of 5dB (R_L = 2k, C_L = 50pF) results in a 10dB peak in the unity gain follower closed loop characteristic (Figure 2).

Figure 2 shows a blow up of the open loop characteristics in the 10MHz to 200MHz frequency range as well as the corresponding unity gain follower characteristics at similar load conditions. It is seen that the output stage zero results in bandwidth extension beyond the 28MHz, 0dB crossover point. In fact, with the proper choice of the R_L,C_L load, the unity gain follower can be "tweaked" to give flat small signal response to 100MHz.

Figure 3 shows corresponding time domain response for a small signal step. As expected there is a strong 80MHz ring for R_L = 2kΩ, C_L = 50pF which disappears at R_L = 50Ω, C_L = 5pF.

Offset Voltage Nulling

The configuration of Figure 4 will give a typical V_{OS} nulling range of ±15mV. If a smaller adjustment range is desired, resistor values R1 = R2 can be increased accordingly. For example, at R1 = 3.6kΩ, the adjustment range is ±5mV. Since pins 1 and 5 are not part of the signal path, AC characteristics are left undisturbed.

Layout Considerations

As with any high-speed wideband amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should be kept as short as possible, and the power supplies bypassed with 0.1µF capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

Figure 4: Vos Nulling Method

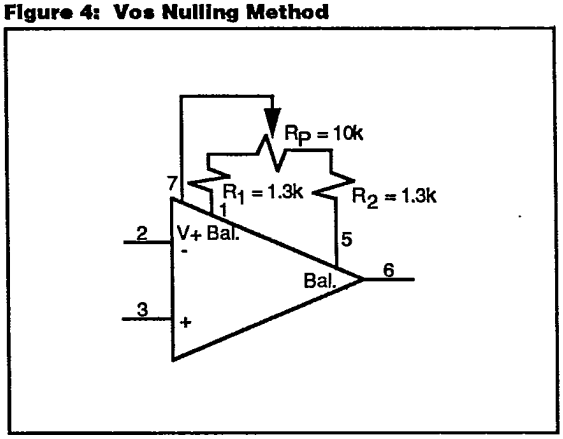


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Figure 2: Unity Gain Follower Frequency Characteristics

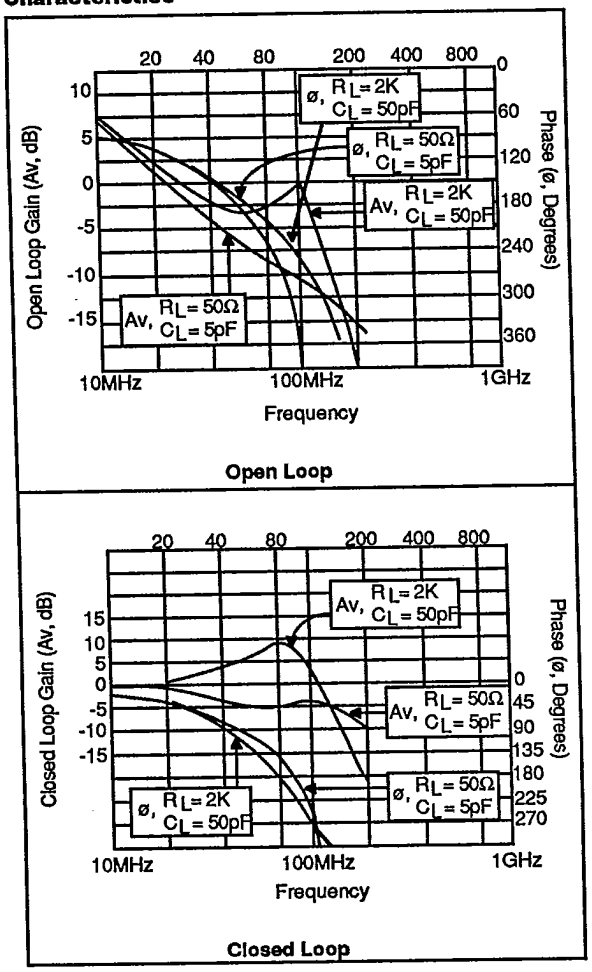

Figure 3: Unity Gain Follower Step Response