T-79-07-10

VA713
HIGH-SPEED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER WITH BUFFER

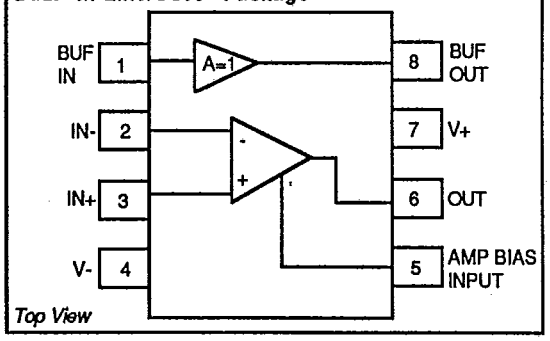
FEATURES
- Low Offset Voltage: 0.5mV
- Controlled Impedance Push-Pull Buffer
- Wide Open Loop Bandwidth: 75MHz OTA, 100MHz Buffer
- Large Output Swing: ±3.8V with 5V Supplies
- Large Output Current: ±5mA OTA, ±20mA Buffer
- Adjustable/Gatable Current-Controlled Gain
- Available in Commercial and Military Versions

APPLICATIONS
- Multiplexers
- Sample/Hold Circuits
- Current-Controlled Filters

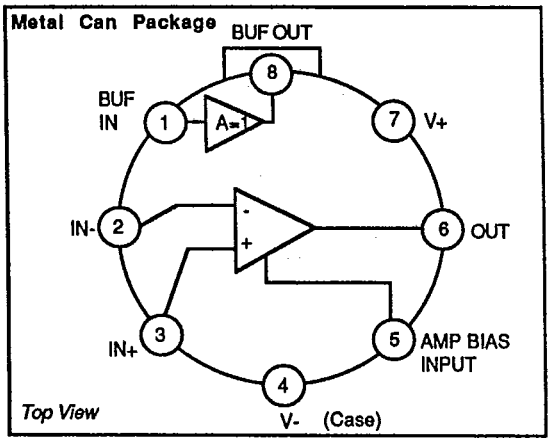
DESCRIPTION
The VA713 is a high-speed operational transconductance amplifier with the added features of current-controlled gain and output buffering. The complementary bipolar process employed with this device combines excellent DC and AC characteristics. Offset voltages are typically 0.5mV while the wideband transistor characteristics provide stable, well-behaved amplifier configurations to 50MHz. The buffer is of the push-pull variety, able to supply ±20mA of output current with an input-to-output offset of less than 20mV. The VA713 is extremely versatile for use in applications such as current-controlled amplifiers, multipliers, sample/hold circuits and VCOs. The device is available in 8-pin DIP, 8-pin surface mount (SOIC) and 8-pin metal can (TO-99) packages.

CONNECTION DIAGRAMS

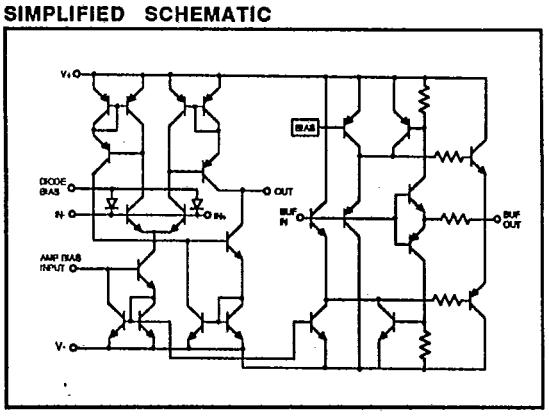
Dual In-Line/SOIC Package



Metal Can Package



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±6V
Differential Input Voltage ..... ±4.5V
Common Mode Input Voltage ..... ±V$_S$
Amp Bias Current ..... 10 mA
Power Dissipation (T_A =70°C, Note 1) 450mW
Output Short Circuit Current Duration: OTA ..... Indefinite
Buffer ..... ≤ P_{MAX}
Operating Temperature Range: VA713J ..... 0° to + 70°C
VA713S ..... -55° to +125°C
Storage Temperature Range ..... -65° to + 150°C
Lead Temperature (Soldering to 60 Sec.) ..... 300°C

Note 1: Power derating above T_A = 70°C to be based on a maximum junction temperature of 150°C and the following thermal resistance factors:

PACKAGES	θ_{JC} (°C/W)	θ_{JA} (°C/W)
DIP	75	180
SOIC	115	180
TO-99	115	250

PACKAGE TYPES AVAILABLE
- 8-Pin Plastic DIP
- 8-Pin CERDIP
- 8-Pin SOIC
- 8-Pin Metal Can, TO-99

ELECTRICAL CHARACTERISTICS (V_S = ±5V, T_A = 25°C, I_{ABC} = 500µA, unless otherwise specified) (Note 1)

PARAMETER (OTA)	SYMBOL	CONDITION	VA713J MIN	VA713J TYP	VA713J MAX	VA713S MIN	VA713S TYP	VA713S MAX	UNITS
Input Offset Voltage	V_{OS}	I_{ABC} = 5µA to 5mA		1	5		0.5	4	mV
		T_A = 0° to 70°C			8				
		T_A = -55° to +125°C						8	
Offset Voltage Change	ΔV_{OS}	I_{ABC} = 5µA to 5mA		3	5		2	4	mV
Input Bias Current	I_B			2.5	5		2.5	5	µA
		T_A = 0° to 70°C			8				
		T_A = -55° to +125°C						10	
Input Offset Current	I_{OS}			0.12	0.6		0.12	0.6	µA
Differential Input Current	I_{DIFF}	I_{ABC} = 0, V_{DIFF} = ±3V		10	200		10	200	nA
Common Mode Range	V_{CM}		±2.75	+4 -3.3		±2.75	+4 -3.3		V
Leakage Current	I_{LEAK}	I_{ABC} = 0, V_{TP} = 0V (Figure 1)		5	100		5	100	nA
		I_{ABC} = 0, V_{TP} = 10V		2	100		2	100	nA
Differential Input Capacitance	C_{IND}			4			4		pF
Differential Input Resistance	R_{IND}	(Note 4)	10	26		10	26		KΩ
Common Mode Input Capacitance	C_{INC}			3			3		pF
Common Mode Input Resistance	R_{INC}	V_{CM} = ±2.75V		1			1		MΩ
Forward Transconductance (Large Signal)	g_m		7700	9900	15000	7700	9900	15000	µmho
		T_A = Full	4000			4000			
Common Mode Rejection Ratio	CMRR	ΔV_{CM} = ±2.75V	80	110		80	110		db
Open Loop Bandwidth	BW	(Figure 2) f - 3DB		75			75		MHz
		Ø(45°)		35			35		MHz
Output Voltage Swing	V_{OUT}	I_{ABC} = 5µA to 5mA, R_L = ∞	±3.5	±4.25		±3.5	±4.25		V
Output Current	I_{OUT}	R_L = 0	350	500	750	350	500	750	µA
		I_{ABC} = 5µA, R_L = 0	3	5	7	3	5	7	
		T_A = Full	300			300			
Output Capacitance	C_{OUT}	(Note 4)		3			3		pF
Output Resistance	R_{OUT}	V_o = ±3.5V (Note 4)		0.5			0.5		MΩ
Slew Rate	SR	Unity Gain (Figure 3, Note 2)		50			50		V/µs
Total Input Noise Voltage	e_N	BW = 10Hz to 100KHz (Fig. 4)		3			3		µVrms
Positive Supply Current	I_{S+}	(Note 3)		1.7	3.0		1.7	3.0	mA
Power Supply Rejection Ratio	PSRR	ΔV_{ps} = ±0.5V	70	86		70	86		db
Amplifier Bias Voltage	V_{ABV}	Measured Pin 5 wrt Pin 4		1.5			1.5		V

Notes: 1. I_{ABC} = (Amplifier Bias Current) The current supplied to the amplifier bias terminal (pin 5) to establish its operating point

2. Slew Rate = f(I_{ABC}) per $SR = \frac{\Delta V_O}{\Delta t} = \frac{io}{C_L} \approx \frac{I_{ABC}}{C_L}$ *where C_L = Total Load Capacitance*

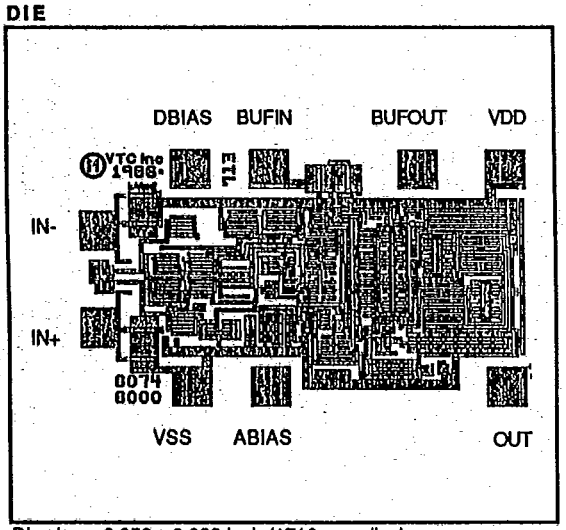
3. Negative Supply Current (I_{S-}) = I_{S+} + I_{ABC}

4. Not tested, guaranteed by design.

ELECTRICAL CHARACTERISTICS (V_S = ±5V, T_A = 25°C, I_{ABC} = 500µA, unless otherwise specified) (Note 1)

PARAMETER (Buffer)	SYMBOL	CONDITION R_L = 150Ω	VA713J			VA713S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Offset Voltage	V_{OS}	V_{IN} = 0V		5			5		mV
Input Bias Current	I_B	V_{IN} = 0V		±0.3	2		±0.3	±2	µA
Input Resistance	R_{IN}	V_{IN} = ±3V		250			250		KΩ
Input Capacitance	C_{IN}			3			3		pF
Output Voltage Swing	V_{OUT}	V_{IN} = ±4V	±3.5	±3.7		±3.5	±3.7		V
Voltage Gain	A_V	V_{IN} = ±3.5V		0.95			0.95		V/V
Output Resistance	R_O	V_{OUT} = ±3V		3			3		Ω
Small Signal Bandwidth	BW	Figure 5 R_L = 2K		120			120		MHz

DIE



Die size = 0.052 x 0.033 inch (1716 sq. miles)
1.32 x 0.84 mm (1.11 sq. mm)

DICE POLICY

Electrical Characteristics

Each die is electrically tested to the commercial or military grade DC parameters to guard band limits at 25°C to guarantee operation over the full temperature range.

Quality Assurance

All dice are 100% visually inspected to the requirement of MIL-STD-883C, Method 2010.2, Condition 3.

All dice are glass passivated with only the bonding pads exposed to provide scratch protection.

All dice are provided with gold backing.

Shipping Packages/Order Information

All dice are packaged in die crates with individual compartments which prevent damage to the die during shipping.

Minimum order for dice is 100, supplied only in multiples of 100.

TEST CIRCUITS

Figure 1: Leakage Current

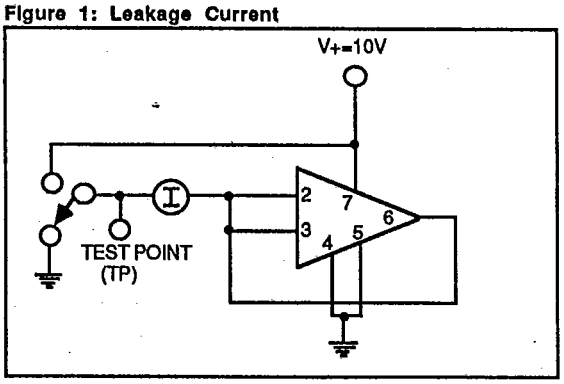


Figure 2: OTA Open Loop Bandwidth

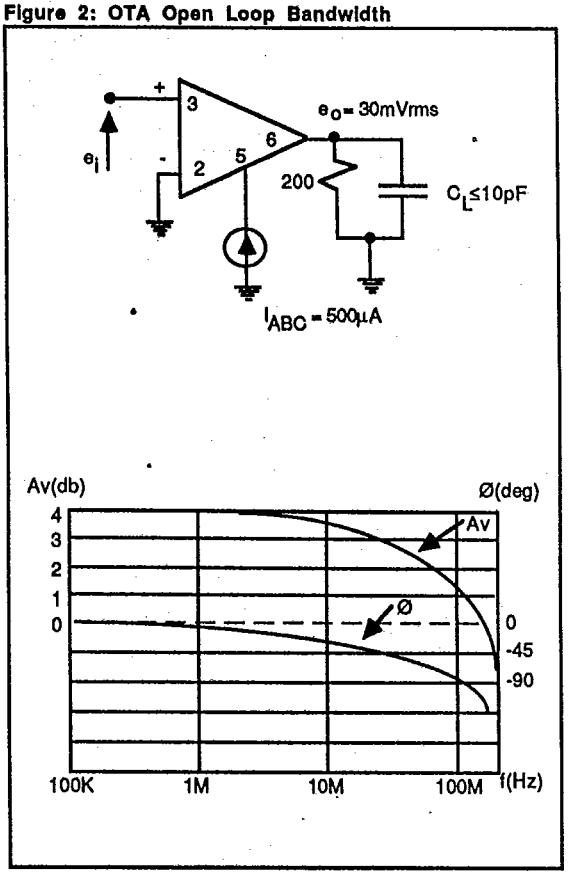


Figure 3: Slew Rate

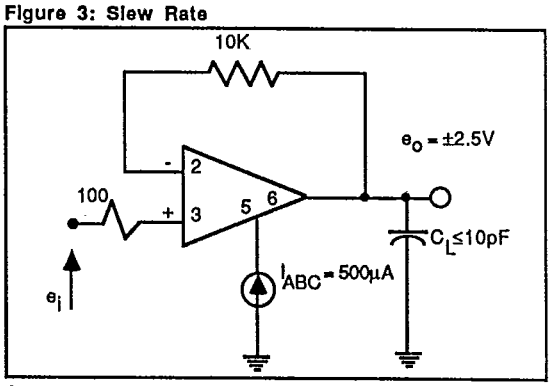


Figure 4: Input Noise Voltage

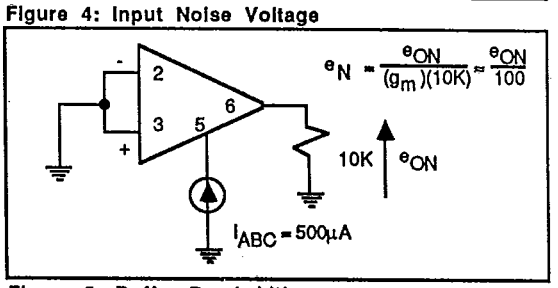
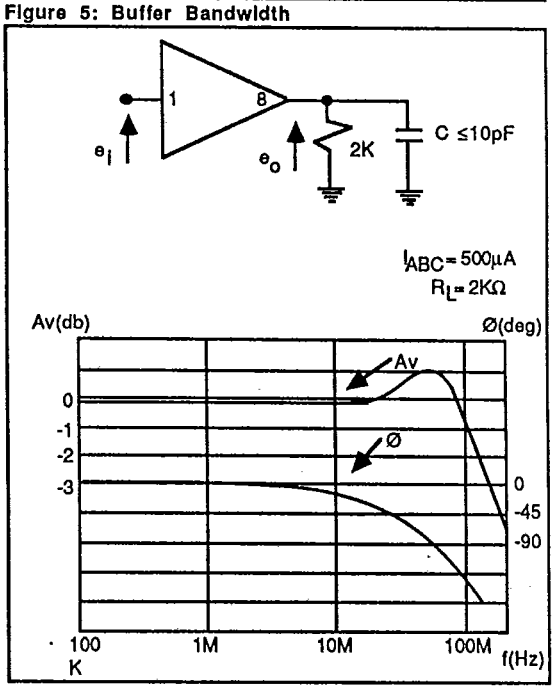
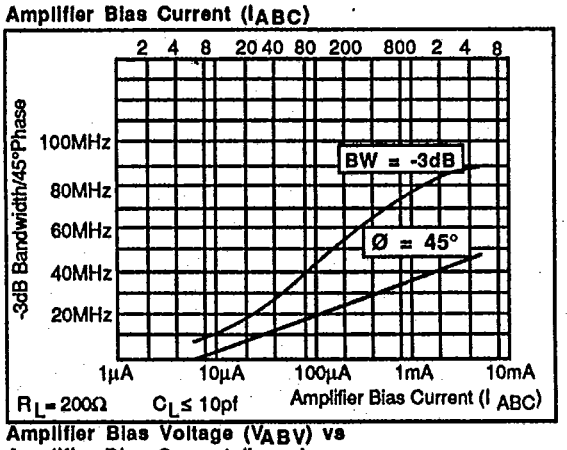


Figure 5: Buffer Bandwidth

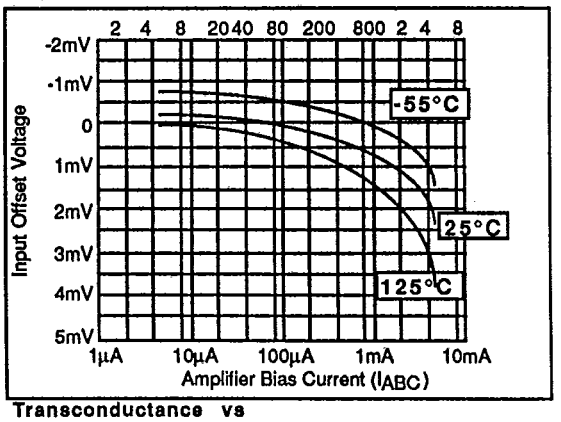


TYPICAL PERFORMANCE CHARACTERISTICS (V_S = ±5V)

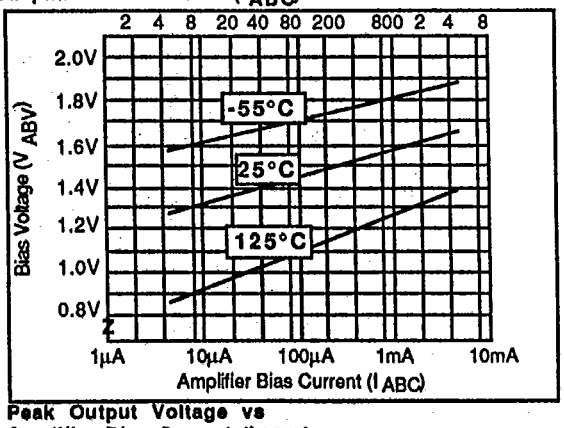
-3dB Bandwidth/45° Phase vs Amplifier Bias Current (I_{ABC})



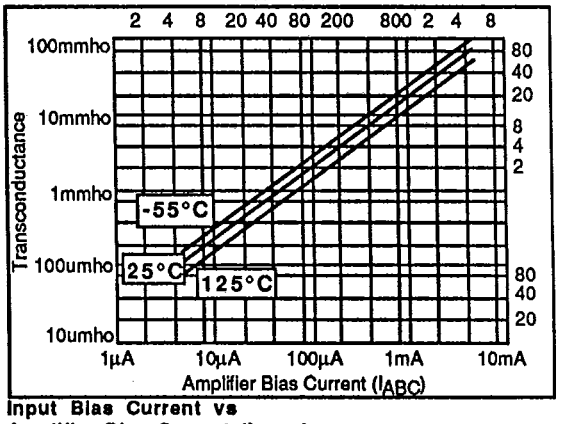
Input Offset Voltage vs Amplifier Bias Current (I_{ABC})



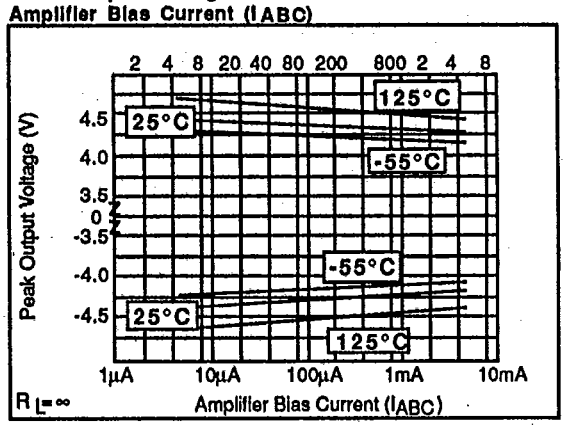
Amplifier Bias Voltage (V_{ABV}) vs Amplifier Bias Current (I_{ABC})



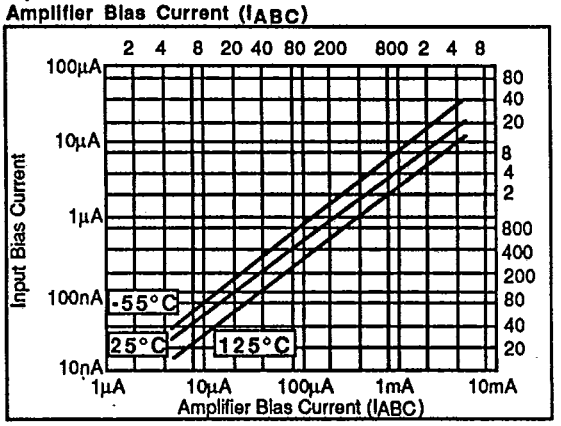
Transconductance vs Amplifier Bias Current (I_{ABC})



Peak Output Voltage vs Amplifier Bias Current (I_{ABC})



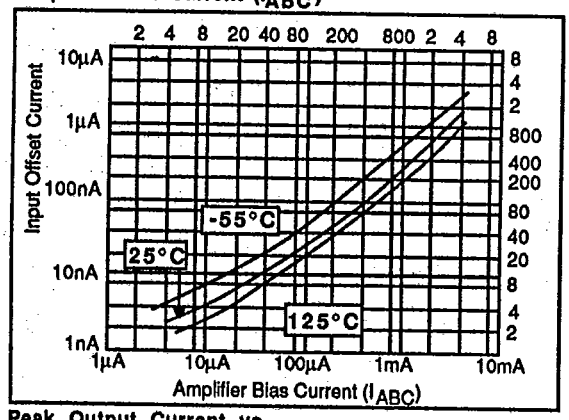
Input Bias Current vs Amplifier Bias Current (I_{ABC})



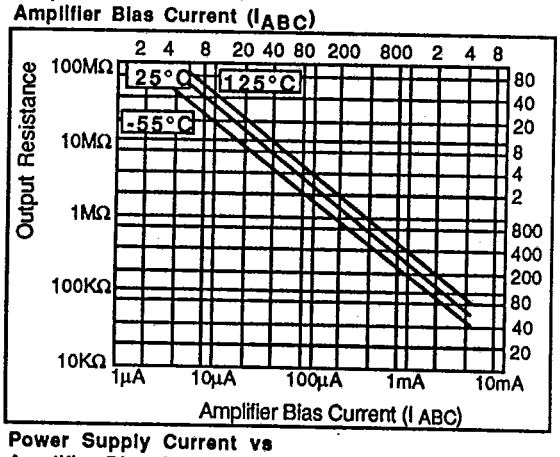
LSP FAMILY DATA SHEETS

TYPICAL PERFORMANCE CHARACTERISTICS (V_S = ±5V)

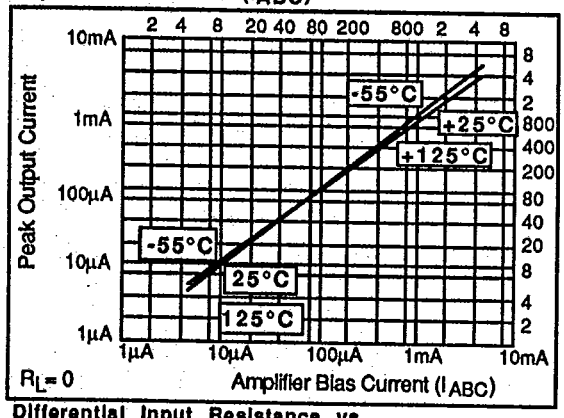
Input Offset Current vs Amplifier Bias Current (I_{ABC})



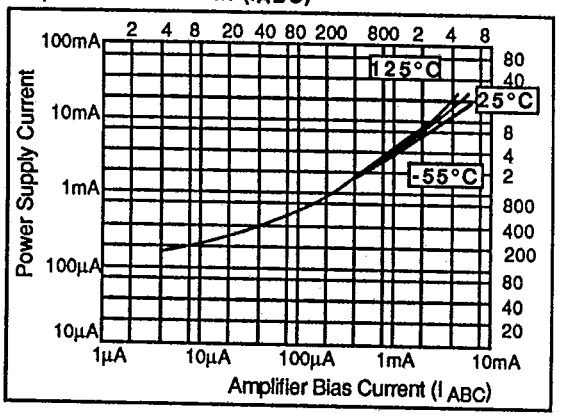
Output Resistance vs Amplifier Bias Current (I_{ABC})



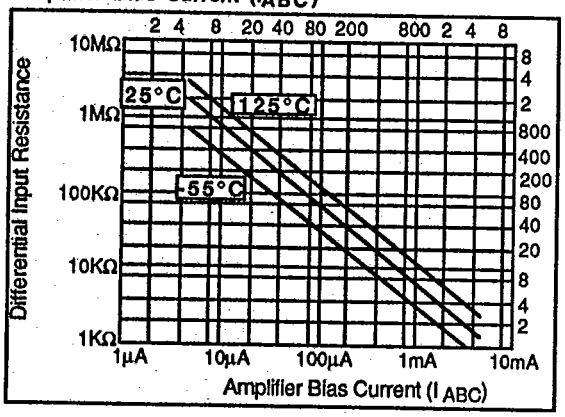
Peak Output Current vs Amplifier Bias Current (I_{ABC})



Power Supply Current vs Amplifier Bias Current (IABC)

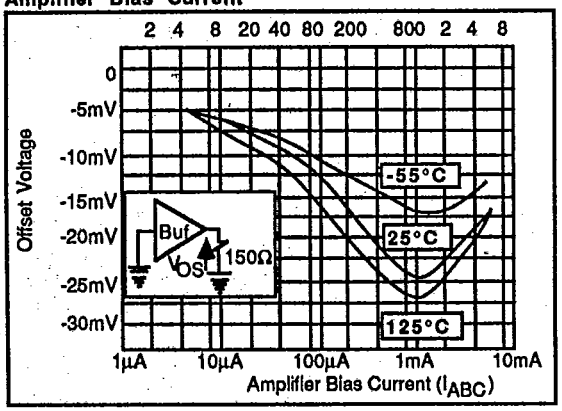


Differential Input Resistance vs Amplifier Bias Current (I_{ABC})

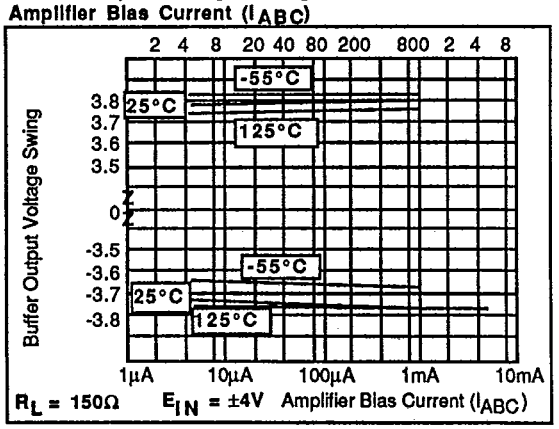


TYPICAL PERFORMANCE CHARACTERISTICS (V_S = ±5V)

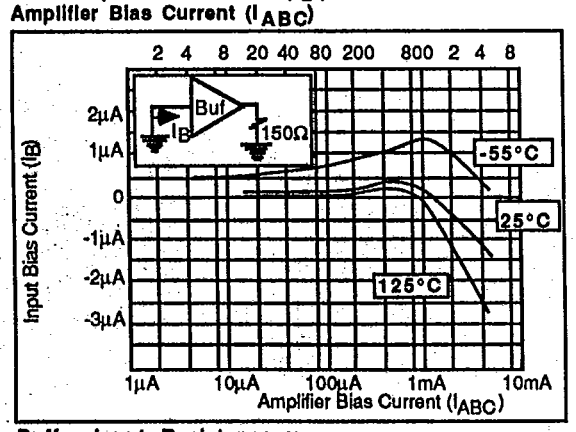
Buffer Offset Voltage vs Amplifier Bias Current



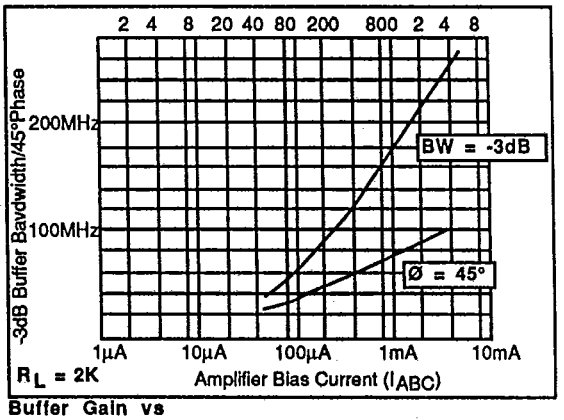
Buffer Output Voltage Swing vs Amplifier Bias Current (I_{ABC})



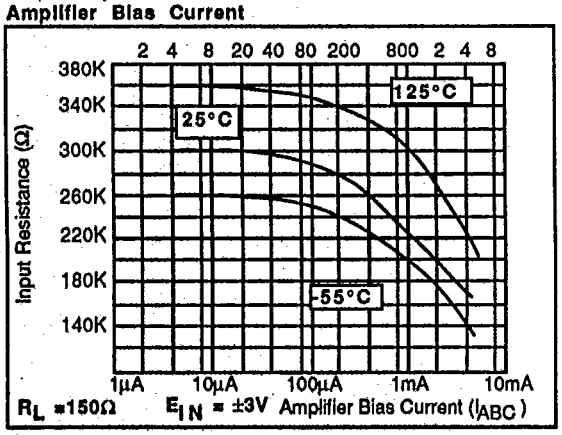
Buffer Input Bias Current (I_B) vs Amplifier Bias Current (I_{ABC})



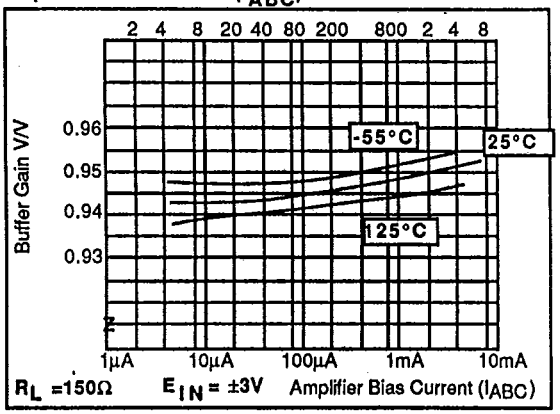
Buffer Bandwidth/45° Phase vs Amplifier Bias Current (I_{ABC})



Buffer Input Resistance vs Amplifier Bias Current



Buffer Gain vs Amplifier Bias Current (I_{ABC})



APPLICATION INFORMATION

General Description

The operational transconductance amplifier (OTA) produces an output current proportional to the differential voltage (V_D) applied at the input according to:

$$I_o = g_m(V_{in+} - V_{in-}) = g_m V_D$$

In addition, the OTA gain (g_m) can be conveniently controlled with an external bias current I_{ABC} to yield:

$$I_o = \frac{I_{ABC}}{2V_T} \cdot V_D$$

$$\text{where } g_m = \frac{I_{ABC}}{2V_T}$$

$$V_T = \text{Thermal Voltage} = \frac{KT}{q} \approx 26\text{mV at } 25°C$$

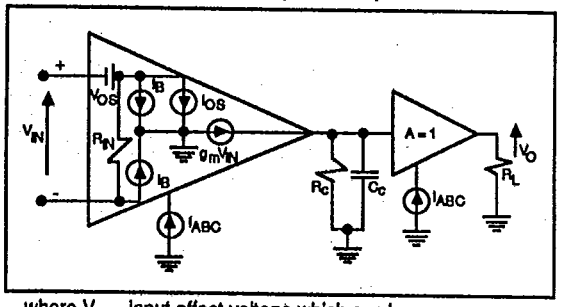
Thus, the OTA becomes a very versatile building block. At a constant I_{ABC} all of the standard operational amplifier circuits can be configured while modulation of I_{ABC} provides for such functions as current controlled active filters, sample/hold amplifiers and multipliers.

The unity gain buffer is of the push-pull variety with an output current capability of ±20mA. A small input to output offset voltage of 20mV insures a ±3V linear output swing without running out of headroom on the OTA. A bandwidth in excess of 100MHz makes it convenient to include the buffer within the feedback loop since phase accumulation is less than 45° even at frequencies to 50MHz. In addition, to maximize the operating current range of the OTA the buffer bias current is varied in proportion to I_{ABC}

OTA as Operational Amplifier

Many of the OTA with buffer applications are based upon the ubiquitous operational amplifier (voltage output device) configuration as shown in Figure 6.

Figure 6: Operational Amplifier Equivalent Circuit



where V_{OS} - Input offset voltage which can be considered independent of I_{ABC}

I_B = Input bias current = $\frac{I_{ABC}}{2\beta}$

β = current gain of input differential pair = 90A/A typical at T = 25°C

I_{OS} = input offset current ≈ 0.05 I_B

$$R_{IN} = \text{input resistance} \approx 200 + \frac{4\beta\, V_T\,(mv)}{I_{ABC}(ma)}$$

$$= 200 + \frac{104\beta}{I_{ABC}(ma)} \text{ at } T = 25°C$$

The open loop voltage gain is determined by $A_V = g_m R_C$ where $R_C = R_{OTA} // R_{BUF}$

R_{OTA} = OTA output impedance = $f(I_{ABC})$
ex: $2.5M\Omega \geq R_{OTA} \geq 60K$ at $0.1mA \leq I_{ABC} \leq 5m$

R_{BUF} = Buffer input impedance = $f(I_{ABC}, R_L)$
ex: $200K \geq R_{BUF} \geq 40K$ at $R_L = 150\Omega$ and $0.1mA \leq I_{ABC} \leq 5mA$

Loop compensation is defined with external capacitor C_C with the 20 db/decade pole set at $f = \frac{1}{2\pi R_C C_C}$

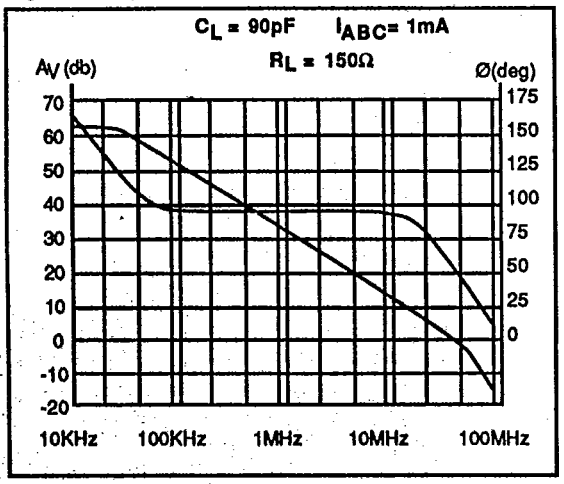
For example with $R_L = 150\Omega$ and $I_{ABC} = 1mA$ the VA713 has the following operational amplifier characteristics:

PARAMETER	*SYMBOL*	*TYPICAL VALUES*	*UNITS*
Offset Voltage	V_{OS}	1	mV
Bias Current	I_B	5.6	µa
Offset Current	I_{OS}	300	na
Input Resistance	R_{IN}	9K	Ω
Common Mode Range	V_{CM}	+4 -3.4	V
Voltage Gain	A_V	1500	V/V
Output Swing	V_O	±3.7	V
Output Resistance	R_O	3.5	Ω
Common Mode Rejection Ratio	CMRR	105	db
+ Power Supply Rejection Ratio	+PSRR	82	db
- Power Supply Rejection Ratio	-PSRR	78	db
Supply Current	I_{ps}	5	mA
Input Noise Voltage	e_N	100	nV/√Hz

As shown in Figure 7, with a compensating capacitor of C_L = 90pf the open loop pole is set at f = 20KHz and the idealized 20 db/decade rolloff characteristic extends to beyond 50MHz.

The 0 db crossover point is f = 30MHz with a phase shift of 60°. This demonstrates that amplifier closed loop configurations will be unity gain stable with a unity gain bandwidth of approximately 30MHz. For applications where unity gain stability is not required, the capacitor value can be reduced with a corresponding extension in gain-bandwidth product.

Figure 7: Operational Amplifier Open Loop Response



Current Controlled Low Pass Filter

Since the gain of the OTA is proportional to I_{ABC}, I_{ABC} modulation becomes a method of bandwidth control for closed loop configurations. As the development in Figure 8 shows, the 2 parameters which determine closed loop bandwidth are $g_m(I_{ABC})$ and C_c. Notice that although R_c sets the open loop bandwidth, R_c drops out of the closed loop bandwidth equation.

Figure 8: OTA Bandwidth Control

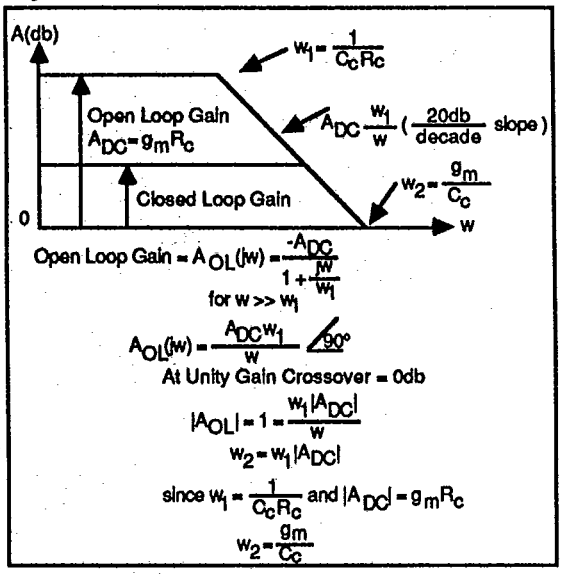
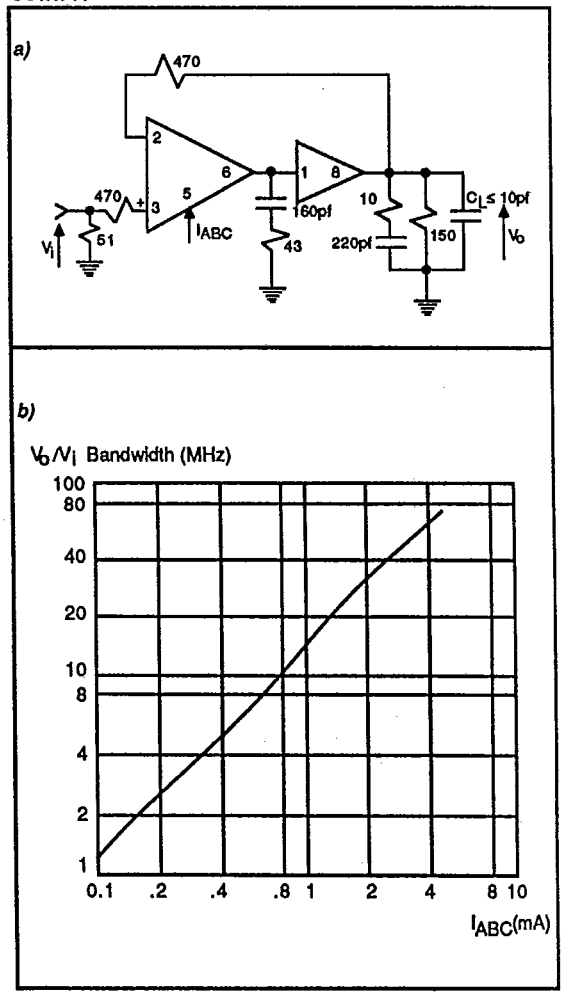


Figure 9a shows an implementation of this bandwidth control technique for a unity gain buffer. With I_{ABC} variations from 100µA to 5mA, corresponding bandwidth variations are from 1.1MHz to 70MHz as shown in Figure 9b.

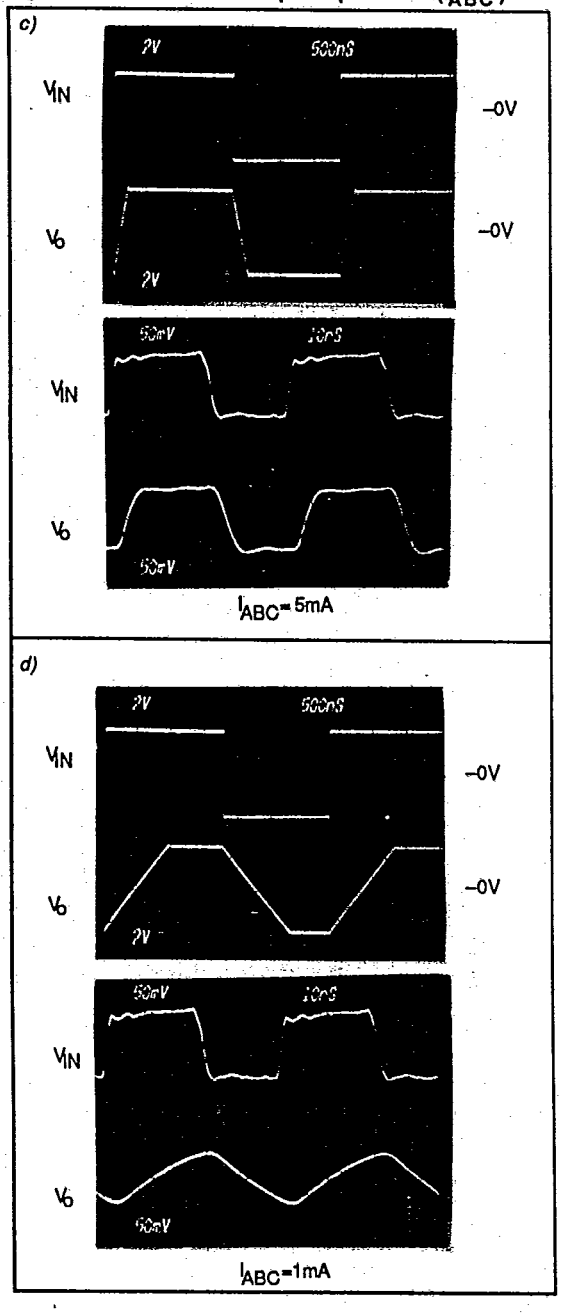
Figures 9a & b: Unity Gain Buffer with Bandwidth Control



LSP FAMILY DATA SHEETS

Figures 9c and 9d show the large and small signal step response for I_{ABC} = 5mA and I_{ABC} = 1mA. In addition to bandwidth variations, as expected, slew rate also varies in proportion to I_{ABC}. SR ≈ 30V/µs at I_{ABC} = 5mA and SR ≈ 7V/µs at I_{ABC} = 1mA.

Figures 9c & d: Buffer Step Response = f(I_{ABC})



Layout Considerations

As with any high-speed circuitry, certain layout considerations are necessary if stable operation is to be ensured and performance is to be optimized. All connections to the OTA should be kept as short as possible, and the power supplies should be bypassed with 0.1uf capacitors, or better yet a combination of 1uf - 10uf electrolytics and 0.01uf ceramic. It is suggested that a ground plane be considered as the best method of maximizing performance because it minimizes stray inductance and unwanted coupling in the ground signal paths. To minimize capacitive effects, resistor values should be kept as small as possible consistent with the application.