

Comlinear CLC416 Dual Low-Power, 120MHz Op Amp

General Description

The Comlinear CLC416 is a dual, wideband (120MHz) op amp. The CLC416 consumes only 39mW per channel and can source or sink an output current of 60mA. These features make the CLC416 a versatile, high-speed solution for demanding applications that are sensitive to both power and cost.

Utilizing Comlinear's proven architectures, this dual current feedback amplifier surpasses the performance of alternative solutions and sets new standards for low power. This power-conserving dual op amp achieves low distortion with -80dBc and -80dBc second and third harmonics respectively. Many high source impedance applications will benefit from the CLC416's $6M\Omega$ input impedance. And finally, designers will have a bipolar part with an exceptionally low 100nA non-inverting bias current.

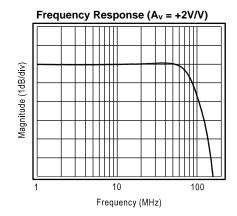
With 0.1dB flatness to 30MHz and low differential gain and phase errors, the CLC416 is an ideal part for professional video processing and distribution. The 120MHz -3dB bandwidth ($A_V = +2$) coupled with a 400V/ μ s slew rate also makes the CLC416 a perfect choice in cost-sensitive applications such as video monitors, fax machines, copiers, and CATV systems.

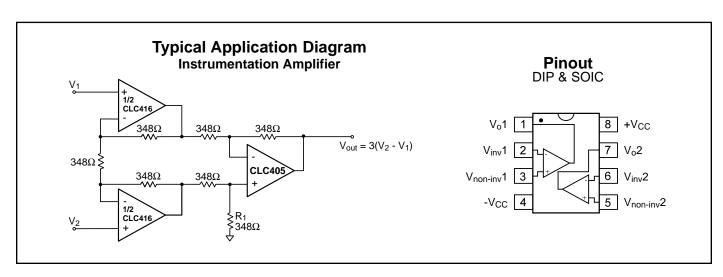
Features

- 0.01%, 0.03° D_G, Dø
- Very low input bias current: 100nA
- High input impedance: 6MΩ
- 120MHz -3dB bandwidth $(A_v = +2)$
- Low power
- High output current: 60mA
- Low-cost

Applications

- Desktop video systems
- Video distribution
- Flash A/D driver
- High-speed driver
- High-source impedance applications
- Professional video processing
- High resolution monitors





CLC416 Electrical Characteristics (A_V = +2, R_f = 348Ω : V_{cc} = \pm 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	MIN	V/MAX RATIN	IGS	UNITS	NOTES
Ambient Temperature	CLC416AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPON							
-3dB bandwidth ±0.1dB bandwidth	$V_{out} < 1.0V_{pp}$ $V_{out} < 5.0V_{pp}$	120 52 30	65 40 15	45 36	45 35	MHz MHz MHz	B 1
gain flatness	$v_{out} < 1.0v_{pp}$	30	15			IVITZ	
peaking rolloff linear phase deviation differential gain	V_{out} < 1.0 V_{pp} V_{out} < 1.0 V_{pp} DC to 200MHz <30MHz <20MHz 4.43MHz, R _L =150 Ω	0.1 0 0.3 0.01	0.7 0.3 0.6 0.04	0.8 0.6 0.7 0.04	1.0 0.6 0.7 0.04	dB dB deg %	B B
differential phase	4.43MHz, R_L =150 Ω	0.03	0.08	0.11	0.12	deg	
TIME DOMAIN RESPONSE rise and fall time settling time to 0.05% overshoot slew rate $A_V = +2$ $A_V = -1$	2V step 2V step 2V step 2V step 1V step	4.3 22 3 400 700	6.5 30 12 300	7.2 38 12 260	7.4 41 12 250	ns ns % V/μs V/μs	
DISTORTION AND NOISE RESP 2nd harmonic distortion 3rd harmonic distortion 2nd harmonic distortion 3rd harmonic distortion equivalent input noise	$\begin{array}{c} \textbf{ONSE} \\ 2V_{pp}, \ 1\text{MHz} \\ 2V_{pp}, \ 1\text{MHz} \\ 2V_{pp}, \ 10\text{MHz} \\ 2V_{pp}, \ 10\text{MHz} \end{array}$	-80 -80 -65 -57	-55 -50	-50 -45	-47 -45	dBc dBc dBc dBc	B B
voltage inverting current non-inverting current crosstalk, input referred	>1MHz >1MHz >1MHz 2V _{pp} , 10MHz	5 12 3 72	6.3 15 3.8 66	6.6 16 4.0 66	6.7 17 4.2 66	nV√Hz pA√Hz pA√Hz dB	
STATIC DC PERFORMANCE input offset voltage average drift		1 30	5	7 50	8 50	mV μV/°C	Α
input bias current	non-inverting	100	900	1600	2800	nA	Α
average drift input bias current average drift	inverting	3 1 17	5	8 6 40	11 8 45	nA/°C μA nA/°C	A
power supply rejection ratio common-mode rejection ratio supply current per channel	DC DC R _L = ∞	52 50 3.9	47 45 4.5	47 45 4.6	45 43 4.9	dB dB mA	B A
MISCELLANEOUS PERFORMAN		1					-,
input resistance input capacitance common mode input range output voltage range output voltage range output current	non-inverting non-inverting $R_L = 100\Omega$ $R_L = \infty$	6 1 ±2.2 +3.5,-2.9 +4.0,-3.4	3 2 ±1.8 +3.1/-2.8 +3.9/-3.3	2.4 2 ±1.7 +2.9/-2.7 +3.8/-3.2 38	1 2 ±1.5 +2.4/-1.7 +3.7/-2.8 20	MΩ pF V V	
output resistance, closed loop		60 0.06	44 0.2	0.25	0.4	mA Ω	

Recommended gain range ±1 to ±40V/V

Transistor count = 110

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

2

Absolute Maximum Ratings

supply voltage $\pm 7V$ I_{out} is short circuit protected to ground common-mode input voltage $\pm Vcc$ maximum junction temperature $+175^{\circ}C$ storage temperature range $+50^{\circ}C$ to $+150^{\circ}C$ lead temperature (soldering 10 sec) $+300^{\circ}C$ ESD rating (human body model) $+300^{\circ}C$

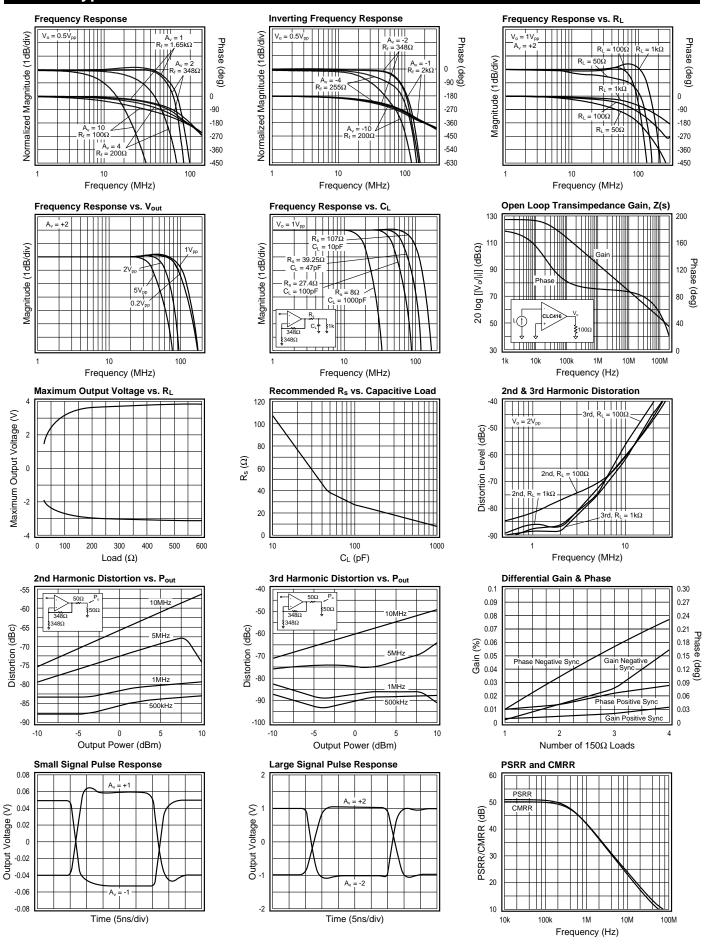
Ordering Information							
Model	Temperature Range	Description					
CLC416AJP CLC416AJE	-40°C to +85°C -40°C to +85°C	8-pin PDIP 8-pin SOIC					

Notes

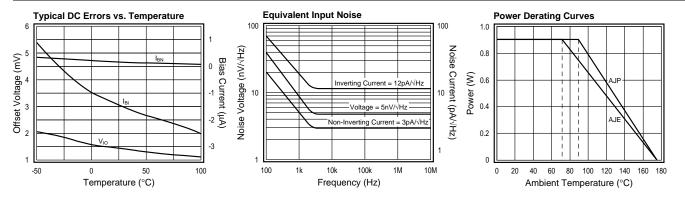
- 1) At temps < 0°C, spec is guaranteed for R_L = 500Ω .
- A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
- B) J-level: spec is sample tested at +25°C.

Package Thermal Resistance						
Package	θјс	θ_{JA}				
Plastic (AJP)	80°C/W	95°C/W				
Surface Mount (AJE)	95°C/W	115°C/W				

CLC416 Typical Performance Characteristics ($V_{cc} = \pm 5V$, $A_v = +2$, $R_f = 348\Omega$, $R_L = 100\Omega$; unless specified)



CLC416 Typical Performance Characteristics ($V_{cc} = \pm 5V$, $A_v = +2$, $R_f = 348\Omega$, $R_L = 100\Omega$; unless specified)



CLC416 OPERATION

Description

The CLC416 is a dual current feedback amplifier with the following features:

- Differential gain and phase errors of 0.01% and 0.03° into a 150Ω load
- Low, 3.9mA, supply current per amplifier

The professional video quality differential gain and phase errors and low power capabilities of the CLC416 make this product a good choice for video applications.

Gain

The non-inverting and inverting gain equations for the CLC416 are as follows:

Non-inverting Gain:
$$1 + \frac{R_f}{R_g}$$

Inverting Gain: $-\frac{R_f}{R}$

Where R_f is the feedback resistor and R_g is the gain setting resistor. Figure 1 shows the general non-inverting gain configuration including the recommended bypass capacitors.

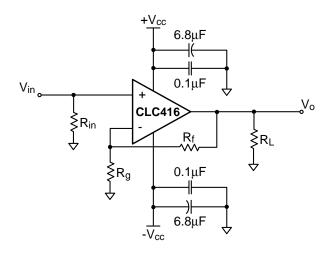


Figure 1: Recommended Non-Inverting Gain Circuit

Feedback Resistor Selection

The feedback resistor, R_f , determines the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC416, at a gain of +2V/V, is achieved with R_f equal to 348Ω . The frequency response plots in the typical performance section illustrate the recommended R_f for several gains. Within limits, R_f can be adjusted to optimize the frequency response.

- Decrease R_f to peak frequency response and extend bandwidth
- Increase R_f to roll off frequency response and reduce bandwidth

As a rule of thumb, if the recommended R_f is doubled, the bandwidth will be cut in half.

Channel Matching

Channel matching and crosstalk efficiency are largely dependent on board layout. The layout of Comlinear's dual amplifier evaluation boards are designed to produce optimum channel matching and isolation. Typical channel matching for the CLC416 is shown in Figure 2.

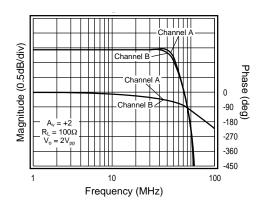


Figure 2: Channel Matching

The CLC416's channel-to-channel isolation is better than 70dB for input frequencies of 4MHz. Input referred crosstalk vs. frequency is illustrated in Figure 3.

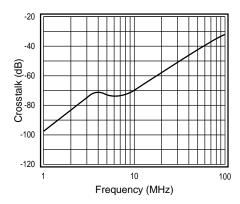


Figure 3: Input Referred Crosstalk vs. Frequency

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC416 will improve stability. The R_s vs. Capacitive Load plot, in the Typical Performance section, gives the recommended series resistance value for optimum flatness at various capacitive loads.

Power Dissipation

The power dissipation of an amplifier can be described in two conditions:

- Quiescent Power Dissipation -P_O (No Load Condition)
- Total Power Dissipation P_T (with Load Condition)

The following steps can be taken to determine the power consumption for each CLC416 amplifier:

- 1. Determine the quiescent power $P_{O} = I_{os} (V_{CO} V_{FF})$
- $$\begin{split} &P_Q = I_{cc} \; (V_{CC} V_{EE}) \\ 2. \; & \text{Determine the RMS power at the output stage} \\ &P_O = (V_{cc} V_{load}) \; (I_{load}), \; \text{where } V_{load} \; \text{and } I_{load} \\ & \text{are the RMS voltage and current across the} \\ & \text{external load}. \end{split}$$
- 3. Determine the total RMS power $P_T = P_O + P_O$

Add the total RMS powers for both channels to determine the power dissipated by the dual.

The maximum power that the package can dissipate at a given temperature is illustrated in the *Power Derating* curves in the *Typical Performance* section. The power derating curve for any package can be derived by utilizing the following equation:

$$P = \frac{(175^{\circ} - Tamb)}{\theta_{JA}}$$

where: T_{amb} = Ambient temperature (°C) θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides

evaluation boards for the CLC416 (730038 - DIP, 730036-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

Supply bypassing is required for best performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. Other layout factors play a major role in high frequency performance. The following are recommended as a basis for high frequency layout:

- 1. Include 6.8μF tantalum and 0.1μF ceramic capacitors on both supplies.
- 2. Place the $6.8\mu F$ capacitors within 0.75 inches of the power pins.
- 3. Place the $0.1\mu F$ capacitors within 0.1 inches of the power pins.
- 4. Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- 5. Minimize all trace lengths to reduce series inductances.

Additional information is included in the evaluation board literature.

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for Comlinear's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The *readme* file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for Comlinear's Op Amps, contains schematics and a reproduction of the *readme* file.

Applications Circuits

Instrumentation Amplifier

An instrumentation circuit is shown on the front page and reproduced in Figure 4. The DC CMRR can be fine tuned by adjusting $R_{\rm 1}$.

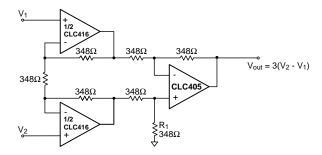


Figure 4: Instrumentation Amplifier

Differential Line Receiver

Figure 5 illustrates a Differential Line Receiver. The circuit will convert differential signals to single-ended signals.

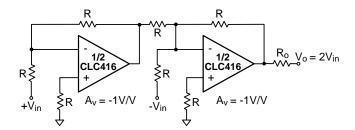


Figure 5: Differential Line Receiver

Bandpass Filter

Figure 6 illustrates a low-sensitivity bandpass filter and design equations. This topology utilizes the CLC416's closely matched amplifiers to obtain low op-amp sensitivity at high frequencies. The CLC405 is used as a buffer to obtain low output impedance. The overall circuit gain is unity. For additional gain, the CLC405 can be configured as a non-inverting amplifier.

To design the filter, choose C and then determine values for R and R_1 based on the desired resonant frequency (f_r) and Q factor.

Figure 7 illustrates a bandpass filter with Q=10 and $f_{\rm r}=1{\rm MHz}$. The component values used are listed below:

 $R_1 = 4.9k\Omega$

 $R = 499\Omega$

C = 330pF

 $R_f = 2k\Omega$

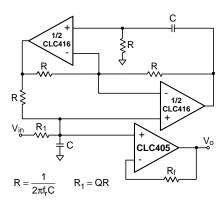


Figure 6: Bandpass Filter Topology

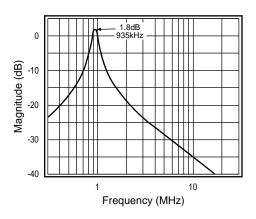


Figure 7: Bandpass Response

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at 1-800-272-9959 or fax 1-800-737-7018.

Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

- 1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation

1111 West Bardin Road Arlington, TX 76017 Tel: 1(800) 272-9959 Fax: 1(800) 737-7018

National Semiconductor Europe

Fax: (+49) 0-180-530 85 86 E-mail: europe.support.nsc.com Deutsch Tel: (+49) 0-180-530 85 85 English Tel: (+49) 0-180-532 78 32 Francais Tel: (+49) 0-180-532 93 58 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.

13th Floor, Straight Block Ocean Centre, 5 Canton Road Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600

Fax: (852) 2736-9960

National Semiconductor Japan Ltd.

Tel: 81-043-299-2309 Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.