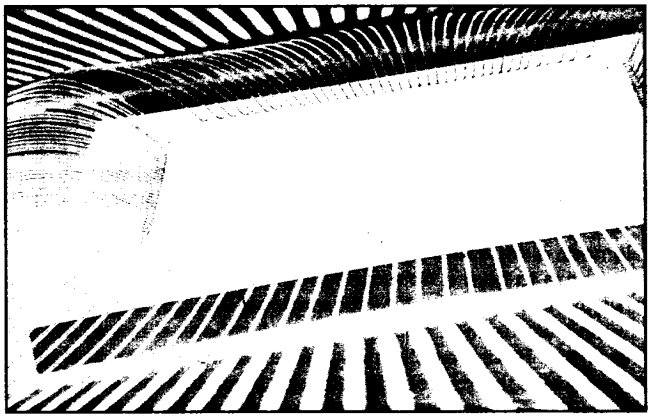
GEC PLESSEY
SEMICONDUCTORS

MARCH 1993

DS3697-2.0

CLR70000

1.0μ (0.8μ L eff) CMOS GATE ARRAYS



Photograph of Bonding Trials on CLR70000

GENERAL DESCRIPTION

Advances in process geometry have resulted in denser and denser core logic. As a consequence the Industries 'pad to gate' ratio (total number of pads vs number of available gates) has been reducing and the number of pad limited designs is rapidly increasing. The CLR70000 employs a completely new design of peripheral cell which is based on a state-of-the-art pad pitch allowing more pads per silicon area. The architecture of the arrays has been optimised to suit the popular JEDEC/EIAJ compliant QFP package types. Couple this with the proven CLA70000 0.8μ (Leff) CMOS core and it's associated libraries and the CLR70000 is well positioned to combat todays fast growing QFP and 'pad limited' CMOS Gate Array applications.

FEATURES

- 1.0μ (0.8μ Leff) twin well, epitaxial CMOS process
- Architecture optimised for Quad Flat Packs
- New peripheral design employing state-of-the-art pad pitch
- 12K to 54K available gates on a channelless array architecture
- Low power consumption (<5μW/gate/MHz)
- Programmable slew controlled outputs.
- 24mA drive capability
- ESD protection in excess of 2kV
- Fully compatible with CLA70000's extensive and proven core libraries.
- Supports JTAG/BIST test philosophies (IEEE 1149-1 Test Procedures)
- Design libraries available on Industry Standard workstations

CLR70000 FAMILY

ARRAY	RAW GATES	PADS	PACKAGE
CLR73000	12200	104	MQFP100 FQFP100 TQFP100
CLR74000	19100	128	MQFP120 MQFP128
CLR75000	30900	160	MQFP144 TQFP144 MQFP160
CLR76000	53900	208	FQFP208

CONTENTS

CMOS PROCESS TECHNOLOGY

The CLR70000 arrays are based on GEC Plessey Semiconductors well proven 0.8µ CMOS process, manufactured at GPS's advanced , Class 10, six-inch wafer fabrication facility. The process is a twin well, self aligned oxide-isolated technology, with an effective channel length of 0.8µ (1.0µ drawn), giving a low defect density, high reliability, and inherently low power dissipation. The process has excellent immunity to latch-up, and ESD, and exhibits stable performance characteristics.

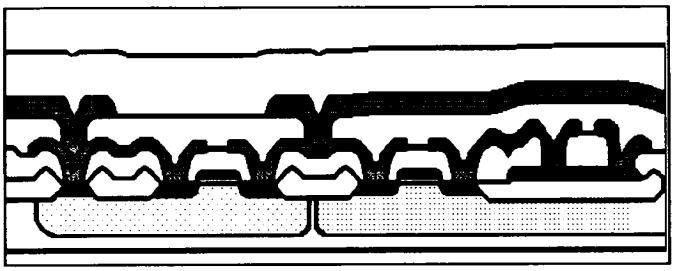


Figure 1 : VQ' Process Cross Section

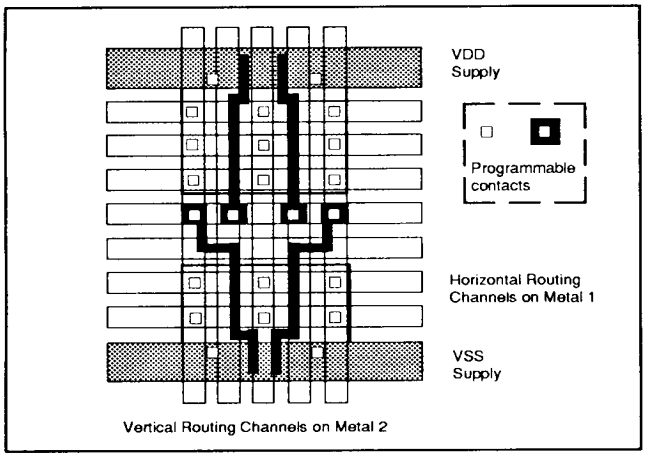


Figure 2 : Core Cell Design showing Cell Transparency

CORE CELL DESIGN

The CLR70000 core is totally compatible with the well proven CLA70000 core. A four transistor group (2 NMOS and 2 PMOS) (fig 2.) forms the basic cell of the core array. This array element is repeated in a regular fashion over the complete core area to give a homogeneous 'Full Field' (sea of gates) array. This lends itself to hierarchical design, allowing pre-routed user defined subcircuits to be repeated anywhere on the array. The core cell structure has been carefully designed to maximise the number of nets which may be routed through the cell. This enables optimal routing for both data flow and control signal distribution schemes thus giving very high overall utilisation figures. This feature is of particular benefit in designs using highly structured blocks such as memory or arithmetic functions.

INPUT/OUTPUT BUFFER DESIGN

The CLR70000 employs a new generation of I/O cell taking advantage of design and assembly advances and new innovative pad layout techniques.

The peripheral cells are fully programmable as Input, Output, VDD or GND, and they are designed to offer several interfacing options, TTL and CMOS for example. The cells already contain input 'pull-up' and 'pull-down' resistors and Electro Static Discharge protection elements. Components for implementing Schmitt Triggers, TTL threshold detectors, tristate control, and flip-flops for signal re-timing are also included. A range of output buffers is available with various output drive currents to match system requirements.

Noise transients due to a large number of simultaneously switching outputs are an increasing problem as bus widths widen (The supply pad location, inductance of the bond wires and package leads are also factors). CLR70000 Arrays offer several I/O buffers with the capability to control the output slew (di/dt) which are invaluable in controlling these transients when driving large capacitive loads such as busses.

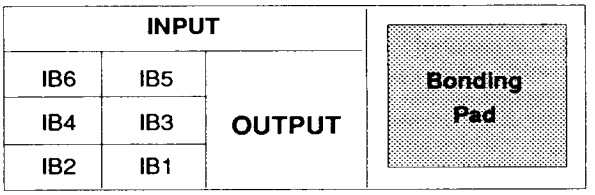
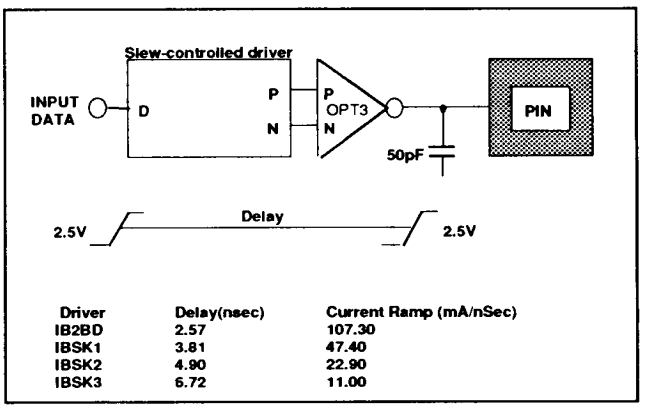


Figure 3 : CLR70000 Peripheral Cell



Driver	Delay(nsec)	Current Ramp (mA/nSec)
IB2BD	2.57	107.30
IBSK1	3.81	47.40
IBSK2	4.90	22.90
IBSK3	6.72	11.00

Figure 4 : Slew Rate Control

CELL LIBRARIES

Core Cells

The CLR70000 array family employs the extensive CLA70000 core cell libraries developed from a broad range of ASIC experience over more than 15 years. Gate level and SSI functions are included in the MICROCELL Library, for implementation of 'glue' logic and customer specific macros. To increase design productivity, the MACROCELL Library contains optimised SSI macro functions similar to standard TTL and CMOS logic families. A higher level of cells, particularly suitable for digital signal processing functions are to be found in the DSP MACROCELL Library. Memory cells (RAM and ROM) are individually generated within the PARACELL Library. To aid in testing of devices the BIST Library contains JTAG/IEEE-1149.1 elements facilitating Built-In-Self-Test methods such as scan path and signature analysis. More detailed information on all these libraries can be found in the CLA70000 datasheet, the CLA70000 design manual and the BIST application guide.

PERIPHERAL CELLS

INTERMEDIATE BUFFER CELLS

Cell	Description	Cell	Description
NPIBCMOS1	CMOS input buffer + large 2 input NAND gate	NPIBSK1	Driver with slewed outputs
NPIBCMOS2	CMOS input buffer + data latch	NPIBSK2	Driver with slewed outputs
NPIBTTL1	TTL input buffer + large 2 input NAND gate	NPIBSK3	Driver with slewed outputs
NPIBBTL2	TTL input buffer + data latch	NPIBTRID	Tri-state driver
NPIBST1	Input Schmitt buffer with CMOS switching levels	NPIBTRID1	Tri-state driver with slewed outputs + 2 inverters
NPIBST2	Input Schmitt buffer with 2V switching levels	NPIBTRID2	Tri-state driver with slewed outputs + 2 inverters
NPIBGATE	NAND2/NOR2 gates	NPIBTRID3	Tri-state driver with slewed outputs + 2 inverters
NPIBCLKB	Large clock driver	NPIB2BD	Dual high powered inverters
NPIBDF	Master-slave D type flip flop	NPDRV3	Clock driver
NPIBDFA	Master-slave D type flip flop	NPDRV6	Clock driver

OUTPUT CELLS

Cell	Description	Cell	Description
NPOP1	Smallest drive output cell	NPOPOD1	Smallest drive open-drain output cell
NPOP2	Small drive output cell	NPOPOD2	Small drive open-drain output cell
NPOP3	Standard drive output cell	NPOPOD3	Standard drive open-drain output cell
NPOP6	Medium drive output cell	NPOPOD6	Medium drive open-drain output cell
NPOP12	Large drive output cell	NPOPOD12	Large drive open-drain output cell
NPOP5B	Standard drive non-inverting output cell	NPOPOD5B	Standard drive non-inverting open-drain output cell
NPOP11B	Large drive non-inverting output cell	NPOPOD11B	Large drive non-inverting open-drain output cell
NPOPT1	Smallest drive tri-state output cell	NPOPOS1	Smallest drive open-source output cell
NPOPT2	Small drive tri-state output cell	NPOPOS2	Small drive open-source output cell
NPOPT3	Standard drive tri-state output cell	NPOPOS3	Standard drive open-source output cell
NPOPT6	Medium drive tri-state output cell	NPOPOS6	Medium drive open-source output cell
NPOPT12	Large drive tri-state output cell	NPOPOS12	Large drive open-source output cell
NPOP4TB	Standard drive non-inverting tri-state output cell	NPOPOS5B	Standard drive non-inverting open-source output cell
NPOP10TB	Large drive non-inverting tri-state output cell	NPOPOS11B	Large drive non-inverting open-source output cell

INPUT CELLS

Cell	Description
NPIPNR	Input cell with no pull up or down resistors
NPIPR1P	Input cell with 1KOhm pull up resistor
NPIPR1M	Input cell with 1KOhm pull down resistor
NPIPR2P	Input cell with 2KOhm pull up resistor
NPIPR2M	Input cell with 2KOhm pull down resistor
NPIPR3P	Input cell with 4KOhm pull up resistor
NPIPR3M	Input cell with 4KOhm pull down resistor
NPIPR4P	Input cell with 100KOhm pull up resistor
NPIPR4M	Input cell with 100K Ohm pull down resistor

OSCILLATOR CELLS *

Cell	Description
NPOSC1	1 to 5MHz Crystal Oscillator
NPOSC2	5 to 20MHz Crystal Oscillator
NPOSC4	15 to 40MHz Crystal Oscillator
NPLPOSC	Low Power 32KHz Crystal Oscillator
NPOSC1ENB	1 to 5MHz Crystal Oscillator with Pwr Down
NPOSC2ENB	5 to 20MHz Crystal Oscillator with Pwr Down
NPOSC3ENB	32KHz to 1MHz Crystal Osc. with Pwr Down
NPOSC4ENB	15 to 40MHz Crystal Osc. with Pwr Down

* In development, please confirm status with local Design Centre

POWER SUPPLY CELLS

Cell	Description	Cell	Description
NPOPVP	VDD power cell for Outputs	NPLAVDD	VDD power cell for Logic Array
NPOPVM	GND power cell for Outputs	NPLAGND	GND power cell for Logic Array
NPIBVP	VDD power cell for Buffers	NPIBLAVDD	VDD power cell for Buffer and Logic Array
NPIBVM	GND power cell for Buffers	NPIBLAGND	GND power cell for Buffer and Logic Array
NPLAVP	VDD power cell for Logic Array	NPALLVP	VDD power cell for All rails
NPLAVM	GND power cell for Logic Array	NPALLVM	GND power cell for All rails
NPIBLAVP	VDD power cell for Buffer and Logic Array	NPALLVDD	VDD power cell for All rails
NPIBLAVM	GND power cell for Buffer and Logic Array	NPALLGND	GND power cell for All rails

Our Libraries are continually being enhanced, so please contact your local Design Centre for the latest information.

DC ELECTRICAL CHARACTERISTICS

All characteristics at Commercial Grade voltage and temperature (0 - 70°C, 4.5V -5.5V)

CHARACTERISTIC	SYM	VALUE Min	VALUE Typ	VALUE Max	UNIT	CONDITIONS
LOW LEVEL INPUT VOLTAGE	VIL				V	
TTL Inputs (NPIBTTL1/NPIBTTL2)				0.8		
CMOS Inputs (NPIBCMOS1/NPIBCMOS2)				1.0		
HIGH LEVEL INPUT VOLTAGE	VIH				V	
TTL Inputs (NPIBTTL1/NPIBTTL2)		2.0				
CMOS Inputs (NPIBCMOS1/NPIBCMOS2)		VDD - 1.0				
INPUT HYSTERESIS					V	
(NPIBST1) Rising	VT+		3.1			VIL to VIH
Falling	VT-		1.9			VIH to VIL
(NPIBST2) Rising	VT+		1.7			VIL to VIH
Falling	VT-		1.1			VIH to VIL
INPUT CURRENT/RESISTANCE (CMOS / TTL INPUTS)	IIN					
No Resistor		-1		+1	µA	VIN = VDD or VSS
Inputs with 1Kohm Resistors		0.5		2	KΩ	
Inputs with 2Kohm Resistors		1		4	KΩ	
Inputs with 4Kohm Resistors		2		8	KΩ	
Inputs with 75Kohm Resistors		25		250	KΩ	
HIGH LEVEL OUTPUT VOLTAGE	VOH				V	
All outputs			VDD - 0.05			IOH = -1µA
Smallest drive cell NPOP1/NPOPT1/NPOPOS1		VDD - 1.0	VDD - 0.5			IOH = -2mA
Low drive cell NPOP2/NPOPT2/NPOPOS2		VDD - 1.0	VDD - 0.5			IOH = -4mA
Standard drive cell NPOP3/NPOPT3/NPOPOS3		VDD - 1.0	VDD - 0.5			IOH = -6mA
Medium drive cell NPOP6/NPOPT6/NPOPOS6		VDD - 1.0	VDD - 0.5			IOH = -12mA
Large drive cell NPOP12/NPOPT12/NPOPOS12		VDD - 1.0	VDD - 0.5			IOH = -24mA
LOW LEVEL OUTPUT VOLTAGE	VOL				V	
All outputs			VDD + 0.05			IOL = 1µA
Smallest drive cell NPOP1/NPOPT1/NPOPOD1			0.2	0.4		IOL = 2mA
Low drive cell NPOP2/NPOPT2/NPOPOD2			0.2	0.4		IOL = 4mA
Standard drive cell NPOP3/NPOPT3/NPOPOD3			0.2	0.4		IOL = 6mA
Medium drive cell NPOP6/NPOPT6/NPOPOD6			0.2	0.4		IOL = 12mA
Large drive cell NPOP12/NPOPT12/NPOPOD12			0.2	0.4		IOL = 24mA
TRISTATE OUTPUT LEAKAGE CURRENT	IOZ				µA	
All open drain output cells		-1		1		VOH = VSS or VDD
OUTPUT SHORT CIRCUIT CURRENT	IOS				mA	
Standard outputs NPOP3/NPOPT3/NPOPOS3		21	45	75		VDD = MAX, VOUT = GND
(See note 1) NPOP3/NPOPT3/NPOPOD3		54	102	165		VDD = MAX, VOUT = VDD
OPERATING SUPPLY CURRENT (per gate) (see note 2)	IDDOP		1		µA/MHz	
INPUT CAPACITANCE	CI		5		pF	ANY INPUTS (see note 3)
OUTPUT CAPACITANCE	COUT		5		pF	ANY OUTPUT (see note 3)
BIDIRECTIONAL PIN CAPACITANCE	CVO		7		pF	ANY I/O PIN (see note 4)

Note 1: Standard driver output NPOP3 etc. Short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.
Note 2: Excluding peripheral buffers.
Note 3: Excludes package leadframe capacitance or bidirectional pins.
Note 4: Excludes package.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
Supply Voltage	- 0.5	7.0	V
Input Voltage	- 0.5	VDD+0.5	V
Output Voltage	- 0.5	VDD+0.5	V

Operation above these absolute maximum ratings or prolonged periods above the recommended operating limits may permanently damage device characteristics and may affect reliability.

Storage Temperature:			
Plastic	- 40	125	degree C

RECOMMENDED OPERATING LIMITS

PARAMETER	MIN	MAX	UNITS
Supply Voltage	3.0	5.5	V
Input Voltage	VSS	VDD	V
Output Voltage	VSS	VDD	V
Current per pad		100	mA
Operating Temperature:			
Commercial Grade	0	70	degree C
Industrial Grade	-40	85	degree C

DESIGN TOOLS

The focus of the GEC Plessey design tool methodology is that of maintaining an open CAD system with all interfaces standardized via EDIF 2.0 . This enables us to provide full support for a variety of 3rd party ASIC design tools and facilitates rapid updating of associated libraries. It also provides an interface to the GEC Plessey (PDS2) design system, which offers a total design environment including behavioral and functional level modelling.

PDS2 - THE GPS ASIC DESIGN SYSTEM

- Behavioral, Functional, and Gate Level Modelling
- VHDL and Third Party Links
- Supports Hierarchical Design Techniques
- EDIF 2.0 Interface

PDS2 is GPS's own proprietary ASIC design system. It provides a fully-integrated, technology independent VLSI design environment for all GPS CMOS SemiCustom products.

PDS2 runs on Digital Equipment Corporation computers and is self configuring according to the available machine resources. It comprises design capture (schematic capture or VHDL), testability analysis, logic simulation, fault simulation, auto place and route, and back annotation. The system offers full support for hierarchical design techniques, maintained from design capture through to layout, as well as advanced design management tools. PDS2 may be used either at a GPS Design Centre or under licence at the customer's premises. A three day training course is available for first time users.

THIRD PARTY SOFTWARE SUPPORT

- Design Kits for major industry standard ASIC design software tools
- All libraries include fully detailed timing information
- EDIF 2.0 Interface
- Post layout back annotation available

GPS supports a wide range of third party design tools including IKOS, Mentor, Verilog, and Viewlogic. The design kits offer fully detailed timing information for all cell libraries, netlist extraction utilities, and post layout back annotation capability where applicable. An example of a workstation design flow is shown in the figure 5 (opposite). Please contact your local GEC Plessey Semiconductor's sales office for further information about support of particular tools.

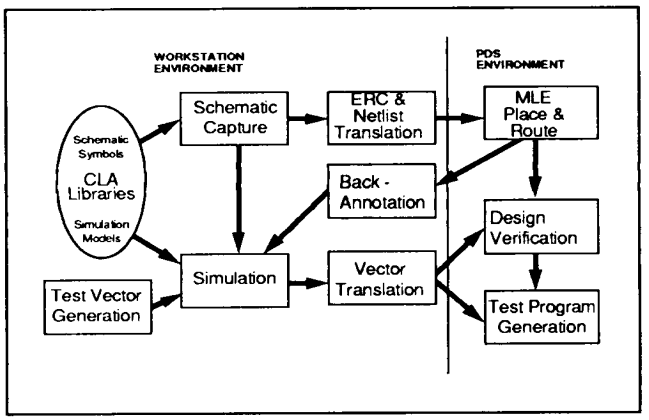


Figure 5 : Workstation Design Flow

DESIGN SUPPORT

Design support is available from various centres worldwide each of which is connected to our Headquarters via high speed data links. A design centre engineer is assigned to each customers circuit, to ensure good communication, and a smooth and efficient design flow.

As part of the design process GPS operates a thorough design audit procedure to verify compliance with customer specification and to ensure manufacturability. The procedure includes four separate review meetings, with the customer, held at key stages of the design. The standard design audit procedure is outlined opposite.

Review 1:	Held at the beginning of the design cycle to check and agree on specifications and design timescales.
Review 2	Held after Logic Simulation and prior to Layout. Checks to ensure satisfactory functionality, timing performance, and adequate fault coverage
Review 3	Held after Layout and Post layout Simulation. Verification of design performance after insertion of actual track loads. Final check of all device specifications before prototype manufacture.
Review 4	Held after prototype delivery. Confirms that the devices meet the specification and are suitable for full scale production.

CLR70000
PACKAGING

The CLR70000 arrays are available in a range of EIAJ/JEDEC compatible Plastic Quad Flat Packs, included in this range are 1.4mm thick and 0.5mm lead pitch variants. The range of packages currently available for the CLR70000 is tabulated below (fig 6). Footprint compatible ceramic packages are also available for fast prototyping (ceramic package for 208 pin and TQFP are in development please confirm availability). Our package portfolio is continually being updated, please consult your local design centre for latest information.

Array	Package	Pins	Approx. Dimensions (mm)			
			L	W	H	P
CLR73	FQFP	100	14	14	2.0	0.50
	MQFP	100	20	14	2.7	0.65
	TQFP	100	14	14	1.4	0.50
CLR74	MQFP	120	28	28	3.5	0.80
	MQFP	128	28	28	3.5	0.80
CLR75	MQFP	144	28	28	3.5	0.65
	TQFP	144	20	20	1.4	0.50
	MQFP	160	28	28	3.5	0.65
CLR76	FQFP	208	28	28	3.5	0.50

Figure 6 : Matrix of Available Plastic Packages

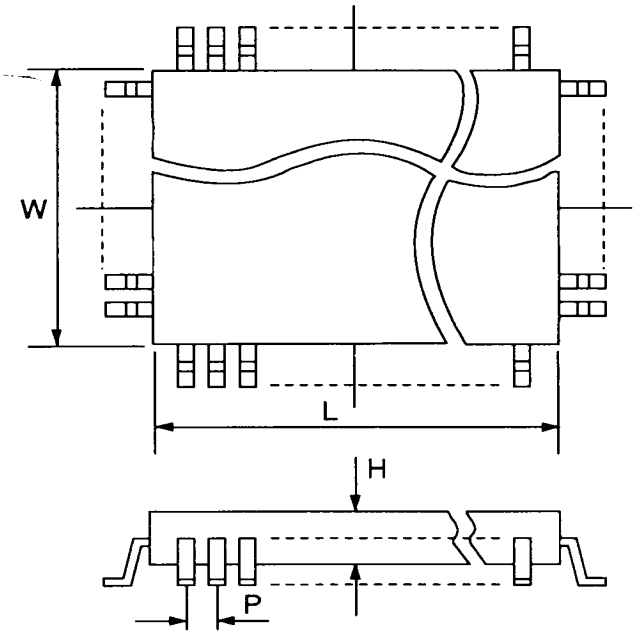


Figure 7 : QFP Outline Drawing

Note : MQFP = Metric Quad Flat Pack
FQFP = Fine Pitch Quad Flat Pack
TQFP = Thin Quad Flat Pack

PRIMARY SEMI-CUSTOM DESIGN CENTRES

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