CIRRUS LOGIC®

CL-SH5600

Preliminary Product Bulletin

Advanced Data Integrity Automated PC/AT Disk Controller

FEATURES

General

- **New generation of automated PC/AT disk controller architecture with advanced data integrity capabilities, including:**
  - — Multiple-burst, 'on-the-fly' error correction
  - — Header ID on-the-fly error correction
  - — Buffer Block CRC
- **Compatible with high-density disk drive technology**
- **Buffer manager and format sequencer sections are compatible with counterpart CL-SH5700 SCSI disk controller**
- **Complete hardware automation of host-to-disk and disk-to-host transfers**
- **Automatic update of PC/AT task file registers**
- **100-pin PQFP/VQFP package (2.7-3.35 mm/1.4 mm height)**
- **Low-power, CMOS technology**

Buffer Manager

- **Supports streaming mode: automatic host and disk operation in the same circular buffer simultaneously, with a pacing mechanism to prevent buffer overrun and underrun**
- **Direct buffer addressing up to 128K bytes of SRAM and 4 Mbytes of DRAM**
- **Buffer memory throughput of up to 20 Mbytes-per-second**
- **Five-channel (local microcontroller, host, disk, 'on-the-fly' correction, and DRAM refresh) circular buffer control with priority resolution**

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OVERVIEW

The CL-SH5600 is a member of the latest generation of disk controllers from Cirrus Logic. The device offers advanced data integrity features required by the error characteristics of high-density disk drive technology. The SCSI counterpart, the CL-SH5700, is an advanced data integrity SCSI disk controller with a buffer manager and format sequencer compatible with the CL-SH5600.

The CL-SH5600 provides a large portion of the hardware necessary to build a PC/AT Winchester disk controller. The CL-SH5600 is typically configured with buffer memory and a microcontroller (with system RAM and ROM) to create a complete, intelligent PC/AT Winchester disk controller. The CL-SH5600 design combines the advanced data integrity features with a Winchester disk formatter,

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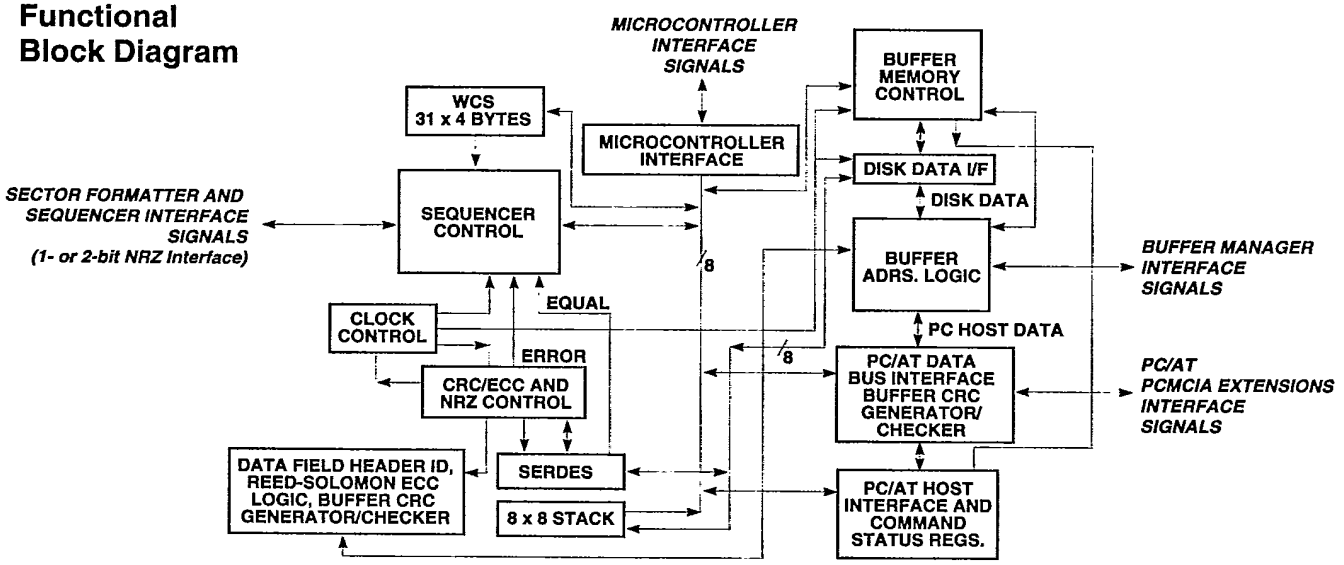
Functional Block Diagram



OVERVIEW (cont.)

a five-channel buffer memory manager, and extensive hardware support for the PC/AT host interface.

The CL-SH5600 performs in hardware many of the buffer-management, task-file-updating, and disk-handling functions previously handled by firmware. The result is minimal microprocessor intervention during data transfers. Its high level of automation makes the CL-SH5600 ideal for both high-performance and low-cost, single-microprocessor disk drive designs.

The full streaming feature of the CL-SH5600 buffer manager allows the host and disk to transfer data from the same circular buffer simultaneously with a mechanism to prevent buffer overrun/underrun. Registers, pointers, and timers are updated by hardware to control the transfer of data between the disk and buffer and between the buffer and host without microprocessor intervention.

The automatic task file management feature updates the PC/AT task file registers whenever a sector is transferred to or from the host, without generating an interrupt to the disk drive microprocessor. The CL-SH5600 provides a handshake for programmed I/O or DMA data transfers on the PC/AT bus at rates up to 6 Mwords-per-second.

The CL-SH5600 disk formatter comprises a serializer/deserializer, a flexible RAM-based sequencer, and CRC/ECC generation circuitry. It supports disk data rates of up to 44 Mbits per second for the single-bit NRZ interface, and 72 Mbits per second for the 2-bit NRZ interface. A proprietary split-data-field technique optimizes disk capacity by allowing use of embedded servo positioning systems with zoned recording formats.

Several advanced data integrity features are offered by the CL-SH5600. The data field error correction code (ECC) consists of a three-way interleaved Reed-Solomon code with programmable redundancy of 4, 5, or 6 bytes-per-interleave, or a total of 12, 15, or 18 bytes of redundancy, respectively. The on-the-fly correction capability can be programmed for 1-, 2-, or up to 3-burst correction. At 6 bytes of redundancy-per-interleave, the maximum correction capability is for a single error burst of 65 bits, or three error bursts, each 17 bits in length.

The buffer block CRC is a programmable feature, offering 4, 5, or 6 bytes of redundancy. It adds another level of protection against data field ECC error misdetection and/or miscorrection. Optionally, the buffer block CRC can be enabled for use in the buffer memory, offering additional protection against buffer memory errors. In this mode, the buffer block CRC is generated at the host interface, carried through to the disk during disk-write operations, and brought back to the host interface during disk-read operations, where it is checked and removed from the data transfer stream. This offers a very comprehensive, overlapped carry-through error protection scheme for the entire disk subsystem.

The header ID ECC consists of a Reed-Solomon code with programmable redundancy of 6, 7, or 8 bytes, covering up to 12 bytes of header ID data. Correction on the ID is performed on-the-fly for a single-burst error and the correction span is programmable for a burst of 5, 9, or 13 bits. The header ID error correction capability offered by the CL-SH5600 reduces the 'header not found' error, which is the dominant error in many of today's disk drive systems.

The CL-SH5600 buffer manager controls up to 128 Kbytes of SRAM and 4 Mbytes of DRAM buffer memory with five-channel circular buffer control and priority resolution. The five channels supported are: local microcontroller, host, disk, 'on-the-fly' correction, and DRAM refresh. The buffer manager supports full-track multi-sector data transfers without microprocessor intervention, enabling lower-cost, single-microprocessor disk drive designs. It also allows buffer segmentation for user-defined caching algorithms, or a protected-memory area in buffer memory.

The CL-SH5600 interfaces directly to a microcontroller and supports both multiplexed and non-multiplexed, Intel®- and Motorola®-type architectures (e.g., 8051, 80196, 68HC11, and 68HC16). Both interrupt and polled processor interface operations are supported. Extensive interrupt masking capability allows for user selection of the required disk and host-interface events.

CL-SH5600

PC/AT Disk Controller

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FEATURES (cont.)

- Separate address pointers for local microcontroller, host, and disk operations
- Fixed or variable buffer segmentation with byte resolution for user-defined caching and read look-ahead
- Supports concurrent host and disk transfers from separate segments
- Supports multi-track minimal latency operations with correct ordering of data in the buffer
- Auto-write buffer pointer

Formatter Interface

- Programmable Reed-Solomon error correction code (ECC) allows for 'on-the-fly' correction of up to a single 65-bit error burst or three 17-bit bursts. The code can be programmed for lower ECC overhead and correction capability
- Optional buffer block CRC of 4, 5, or 6 bytes, provides added buffer memory protection and reduces the data field misdetection/miscorrection probability
- Programmable Reed-Solomon ECC allows 'on-the-fly' correction on the header ID of up to 13-bit error burst
- Single- and double-bit NRZ rates of 44 and 72 Mbits/second, respectively
- Automatic, full-track read/write operations with overrun/underrun logic to stop multi-sector transfers when the buffer is full/empty
- Full-track multi-sector transfer capability without local processor intervention
- Automatic WCS branch commands automate retry algorithms and defect management
- Split-data-field operation for embedded servo positioning systems
- Programmable read synchronization time-out and two-index time-out circuits for sector searches
- Programmable RAM-based disk formatter writable control store (WCS) of 31 x 4 bytes

Microcontroller Interface

- Support for high-speed processors (e.g., 8051, 68HC11, 68HC16, HPC460X3, 80196)
- Support for multiplexed and non-multiplexed address and data bus microcontroller interfaces
- Supports interrupt or polled processor interface
- Supports Intel®- or Motorola®-type processor register map
- Supports direct microcontroller access to buffer memory and five external switches
- Supports scheduled access to WCS and buffer memory
- Supports separate host and disk interrupt structures
- Three-level power-down capability when idle

PC/AT Interface

- True real-time hardware and software compatibility with PC/AT computers
- Supports automatic update of PC/AT task file and release of data blocks
- Provides programmable logic to speed command response
- Supports automatic write and multiple-mode PC/AT transfers
- Host data transfer under programmed I/O, DMA, or demand mode DMA (EISA Type 'B')
- Supports enhanced ATA timings for PIO mode 3 and multi-word DMA mode 1
- 8- and 16-bit data transfers on the host bus
- Programmable and auto wait state generation for compatibility with any host speed
- Direct bus interface with programmable 12/24-mA drivers on-chip
- AT master/slave protocol

ADVANTAGES

Unique Features	Benefits
■ Advanced data integrity features: — Multi-burst 'on-the-fly' correction — Header ID ECC with on-the-fly correction	❒ Compatible with high-density disk drive technology.
■ Buffer block CRC	❒ Buffer memory protection, overlapped carry-through error detection, reduced misdetection/miscorrection probability on data field ECC.
■ Full streaming mode	❒ Better performance with minimal firmware and microcontroller overhead.
■ DRAM support	❒ Allows larger buffer sizes for better caching performance.
■ Automatic task file management	❒ Requires less firmware overhead; provides higher performance.
■ Disk data rates of up to 72 Mbits/second	❒ Ideal for high-performance disk drive applications.
■ Proprietary split-data-field support	❒ Optimizes disk capacity, enables use of zoned recording formats.