



8Mx72 EDO DRAM 3.3V DIMM MODULE

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
WPDE8M72V-60MDC	60ns	20ns	110ns	30ns
WPDE8M72V-70MDC	70ns	25ns	130ns	33ns

- Fast Page with EDO Mode operation
- CAS-before-RAS refresh capability
- RAS-only refresh capability
- LVTTTL compatible inputs and outputs
- +3.3V $\pm$ 0.3V power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- ECC Optimized
- Gold edge connectors

GENERAL DESCRIPTION

The WPDE8M72V-XMDC is a 8M x 72 bit Dynamic RAM high density memory module. The module consists of thirty-six 4M x 4 bit DRAMs in 24-pin TSOP packages. The DRAMs are mounted in stacks of two on a 168-pin glass epoxy substrate. A 0.1 μ F decoupling capacitor is mounted for each DRAM. Selected inputs and outputs are buffered for improved performance and easier memory subsystem design.

The WPDE8M72V-XMDC is a Dual In-line Memory Module with gold edge connections, 3.3V power supply, EDO, and 4K refresh. The WPDE8M72V-XMDC is optimized for ECC and intended for mounting into 168-pin edge connector sockets.

**PIN CONFIGURATION**

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	25	NC	49	V _{CC}	73	V _{CC}	97	DQ ₄₅	121	A ₉	145	NC
2	DQ ₀	26	V _{CC}	50	NC	74	DQ ₃₂	98	DQ ₄₆	122	A ₁₁	146	NC
3	DQ ₁	27	$\overline{WE}_0$	51	NC	75	DQ ₃₃	99	DQ ₄₇	123	NC	147	NC
4	DQ ₂	28	$\overline{CAS}_0$	52	DQ ₁₈	76	DQ ₃₄	100	DQ ₄₈	124	V _{CC}	148	NC
5	DQ ₃	29	NC	53	DQ ₁₉	77	DQ ₃₅	101	DQ ₄₉	125	NC	149	DQ ₆₁
6	V _{CC}	30	$\overline{RAS}_0$	54	V _{SS}	78	V _{SS}	102	V _{CC}	126	B ₀	150	DQ ₆₂
7	DQ ₄	31	$\overline{OE}_0$	55	DQ ₂₀	79	PD ₁	103	DQ ₅₀	127	V _{SS}	151	DQ ₆₃
8	DQ ₅	32	V _{SS}	56	DQ ₂₁	80	PD ₃	104	DQ ₅₁	128	NC	152	V _{SS}
9	DQ ₆	33	A ₀	57	DQ ₂₂	81	PD ₅	105	DQ ₅₂	129	$\overline{RAS}_3$	153	DQ ₆₄
10	DQ ₇	34	A ₂	58	DQ ₂₃	82	PD ₇	106	DQ ₅₃	130	NC	154	DQ ₆₅
11	DQ ₈	35	A ₄	59	V _{CC}	83	ID ₀	107	V _{SS}	131	NC	155	DQ ₆₆
12	V _{SS}	36	A ₆	60	DQ ₂₄	84	V _{CC}	108	NC	132	$\overline{PDE}$	156	DQ ₆₇
13	DQ ₉	37	A ₈	61	NC	85	V _{SS}	109	NC	133	V _{CC}	157	V _{CC}
14	DQ ₁₀	38	A ₁₀	62	NC	86	DQ ₃₆	110	V _{CC}	134	NC	158	DQ ₆₈
15	DQ ₁₁	39	NC	63	NC	87	DQ ₃₇	111	NC	135	NC	159	DQ ₆₉
16	DQ ₁₂	40	V _{CC}	64	NC	88	DQ ₃₈	112	NC	136	DQ ₅₄	160	DQ ₇₀
17	DQ ₁₃	41	NC	65	DQ ₂₅	89	DQ ₃₉	113	NC	137	DQ ₅₅	161	DQ ₇₁
18	V _{CC}	42	NC	66	DQ ₂₆	90	V _{CC}	114	$\overline{RAS}_1$	138	V _{SS}	162	V _{SS}
19	DQ ₁₄	43	V _{SS}	67	DQ ₂₇	91	DQ ₄₀	115	NC	139	DQ ₅₆	163	PD ₂
20	DQ ₁₅	44	$\overline{OE}_2$	68	V _{SS}	92	DQ ₄₁	116	V _{SS}	140	DQ ₅₇	164	PD ₄
21	DQ ₁₆	45	$\overline{RAS}_2$	69	DQ ₂₈	93	DQ ₄₂	117	A ₁	141	DQ ₅₈	165	PD ₆
22	DQ ₁₇	46	$\overline{CAS}_4$	70	DQ ₂₉	94	DQ ₄₃	118	A ₃	142	DQ ₅₉	166	PD ₈
23	V _{SS}	47	NC	71	DQ ₃₀	95	DQ ₄₄	119	A ₅	143	V _{CC}	167	ID ₁
24	NC	48	$\overline{WE}_2$	72	DQ ₃₁	96	V _{SS}	120	A ₇	144	DQ ₆₀	168	V _{CC}

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**PIN CONFIGURATION** (continued)**Pin Names**

Pin Name	Pin Function
A_0, B_0, A_1-A_{11}	Address Inputs (Buffered)
DQ_x	Data In/Out
$\overline{WE}_0, \overline{WE}_2$	Read/Write Input (Buffered)
$\overline{OE}_0, \overline{OE}_2$	Output Enable (Buffered)
$\overline{RAS}_0-\overline{RAS}_3$	Row Address Strobe
$\overline{CAS}_0, \overline{CAS}_4$	Column Address Strobe (Buffered)
PD_1-PD_8	Presence Detect (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID_0-ID_1	ID Bits
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Presence Detect

For 8Mx72 Bits Configuration with 4M x 4 Bits chips and 4K Refresh:

$PD_1=V_{SS}, PD_2=V_{SS}, PD_3=V_{CC}, PD_4=V_{CC}$

For Fast Page with EDO:

$PD_5=V_{CC}$

Speed:

Pin	60ns	70ns
PD_6	V_{CC}	V_{SS}
PD_7	V_{CC}	V_{CC}

For ECC:

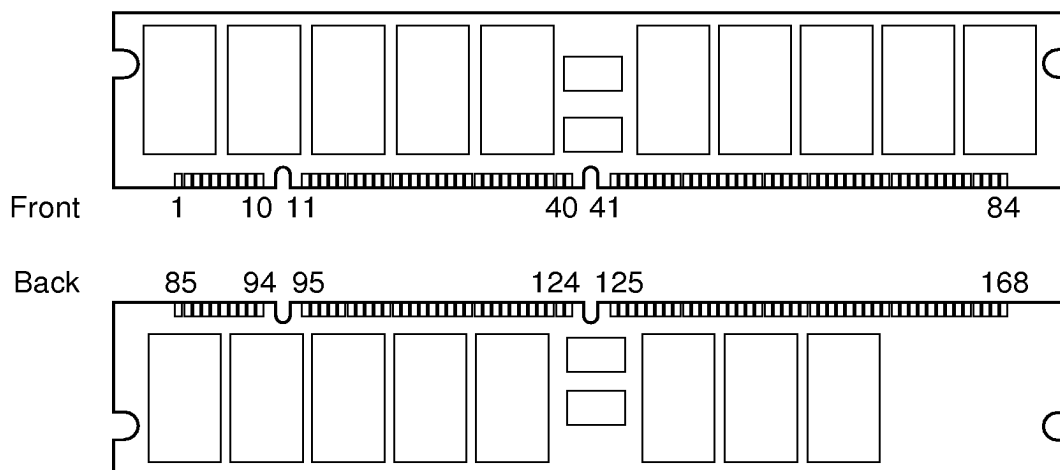
$PD_8=V_{SS}$

For x72 ECC:

$ID_0=V_{SS}$

For Normal Refresh Mode:

$ID_1=V_{SS}$





WPDE8M72V-XMDC

**ABSOLUTE MAXIMUM RATINGS***

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS} ; $T_A=0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+0.3^*$	V
Input Low Voltage	V_{IL}	-0.3**	—	0.8	V

* $V_{CC}+1.3\text{V}/15\text{ns}$. Pulse width is measured at V_{CC} .

** $-1.3\text{V}/15\text{ns}$. Pulse width is measured at V_{SS} .

**DC AND OPERATION CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling @ $t_{\text{RC}}=\text{min.}$)	WPDE8M72V-60 WPDE8M72V-70	I_{CC1}	— —	1476 1296	mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{WE}}=V_{\text{IH}}$)		I_{CC2}	—	100	mA
RAS-Only Refresh Current* ($\overline{\text{CAS}}=V_{\text{IH}}$, RAS Cycling @ $t_{\text{RC}}=\text{min.}$)	WPDE8M72V-60 WPDE8M72V-70	I_{CC3}	— —	1476 1296	mA mA
EDO Mode Current* ($\overline{\text{RAS}}=V_{\text{IL}}$, $\overline{\text{CAS}}$ Cycling @ $t_{\text{PC}}=\text{min.}$)	WPDE8M72V-60 WPDE8M72V-70	I_{CC4}	— —	1656 1476	mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{WE}}=V_{\text{CC}}-0.2\text{V}$)		I_{CC5}	—	30	mA
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @ $t_{\text{RC}}=\text{min.}$)	WPDE8M72V-60 WPDE8M72V-70	I_{CC6}	— —	1476 1296	mA mA
Input Leakage Current (Any input $0 \leq V_{\text{IN}} \leq V_{\text{CC}} + 0.3\text{V}$; all other pins not under test = 0V)	All but $\overline{\text{RAS}}$ $\overline{\text{RAS}}$	I_{IL}	-5 -45	5 45	μA μA
Output Leakage Current (Data out is disabled; $0 \leq V_{\text{OUT}} \leq V_{\text{CC}}$)		I_{OL}	-10	10	μA
Output High Voltage Level ($I_{\text{OH}} = -2\text{mA}$)		V_{OH}	2.4	—	V
Output Low Voltage Level ($I_{\text{OL}} = 2\text{mA}$)		V_{OL}	—	0.4	V

* I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , address can be changed maximum once while $\overline{\text{RAS}}=V_{\text{IL}}$. In I_{CC4} , address can be changed maximum once within one EDO mode cycle.

CAPACITANCE ($T_{\text{A}}=25\text{ }^{\circ}\text{C}$; $V_{\text{CC}}=3.3\text{V}$; $f=1\text{Mhz}$)

Item	Symbol	Min	Max	Units
Input Capacitance (A_0 , B_0 , A_{1-11} , $\overline{\text{CAS}}_x$, $\overline{\text{WE}}_x$, $\overline{\text{OE}}_x$)	C_{IN1}	—	13	pF
Input Capacitance ($\overline{\text{RAS}}_x$)	C_{IN2}	—	63	pF
Input/Output Capacitance (DQ_x)	C_{DQ1}	—	14	pF

**AC CHARACTERISTICS**(0 °C ≤ T_A ≤ 70 °C; V_{CC} = 3.3V ± 0.3V; V_{IH}/V_{IL} = 2.0/0.8V; V_{OH}/V_{OL} = 2.0/0.8V; See notes 1 and 2; Output loading C_L = 100pF)

Parameter	Symbol	WPDE8M72V-60		WPDE8M72V-70		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		ns	
Read-modify-write cycle time	t _{RWC}	155		185		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		60		70	ns	3,4,11
Access time from $\overline{\text{CAS}}$	t _{CAC}		20		25	ns	3,4,5,15
Access time from column address	t _{AA}		35		40	ns	3,11,15
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	8		8		ns	3,15
$\overline{\text{OE}}$ to output in Low-Z	t _{OLZ}	8		8		ns	3,15
Output buffer turn-off delay from $\overline{\text{CAS}}$	t _{CEZ}	8	20	8	25	ns	7,12,13,15
Transition time (rise and fall)	t _T	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	40		50		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	20		25		ns	15
$\overline{\text{CAS}}$ hold time	t _{CSH}	43		48		ns	15
$\overline{\text{CAS}}$ pulse width	t _{CAS}	10	10,000	15	10,000	ns	14
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	18	40	18	45	ns	4,15
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	13	25	13	30	ns	11,15
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10		10		ns	15
Row address set-up time	t _{ASR}	5		5		ns	15
Row address hold time	t _{RAH}	8		8		ns	15
Column address set-up time	t _{ASC}	0		0		ns	
Column address hold time	t _{CAH}	10		15		ns	
Col. addr. hold time ref. to $\overline{\text{RAS}}$	t _{AR}	43		53		ns	6,15
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	35		40		ns	15
Read command set-up time	t _{RCS}	0		0		ns	
Read command hold referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		ns	9
Read command hold referenced to $\overline{\text{RAS}}$	t _{RRH}	-2		-2		ns	9,15
Write command hold time	t _{WCH}	10		15		ns	
Write command hold referenced to $\overline{\text{RAS}}$	t _{WCR}	45		55		ns	6
Write command pulse width	t _{WP}	10		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	20		25		ns	15
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	10		15		ns	
Data set-up time	t _{DS}	-2		-2		ns	10,15

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AC CHARACTERISTICS (continued)

Parameter	Symbol	WPDE8M72V-60		WPDE8M72V-70		Unit	Notes
		Min	Max	Min	Max		
Data hold time	t_{DH}	15		20		ns	10,15
Data hold time referenced to $\overline{RAS}$	t_{DHR}	45		55		ns	6
Refresh period (2K refresh)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40		50		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	83		98		ns	8,15
Column address to $\overline{WE}$ delay time	t_{AWD}	55		65		ns	8
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	60		70		ns	
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	5		5		ns	15
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	8		13		ns	15
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	15
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45	ns	3,15
Hyper Page cycle time	t_{HPC}	30		33		ns	14
Hyper Page read-modify-write cycle time	t_{HPRWC}	77		92		ns	14
$\overline{CAS}$ precharge time (Hyper Page cycle)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	t_{RASP}	60	200,000	70	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHPC}	40		45		ns	15
$\overline{OE}$ access time	t_{OEA}		20		25	ns	15
$\overline{OE}$ to data delay	t_{OED}	20		25		ns	15
Output buffer turn off delay from $\overline{OE}$	t_{OEZ}	5	20	5	25	ns	7,12,15
$\overline{OE}$ command hold time	t_{OEH}	15		20		ns	
$\overline{WE}$ to $\overline{RAS}$ precharge (C-B-R refresh)	t_{WRP}	15		15		ns	15
$\overline{WE}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	8		8		ns	15
Output data hold time	t_{DOH}	10		10		ns	15
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	15	3	20	ns	7,12,13
Output buffer turn off delay from $\overline{WE}$	t_{WEZ}	3	20	3	25	ns	7,12,15
$\overline{WE}$ to data delay	t_{WED}	20		25		ns	15
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time t_{OEP}	5		5		ns		
$\overline{WE}$ pulse width (Hyper Page cycle)	t_{WPE}	5		5		ns	
$\overline{PDE}$ to valid PD bitt _{PD}		10		10	ns		
$\overline{PDE}$ to PD bit inactive	t_{PDOFF}	2	7	2	7	ns	

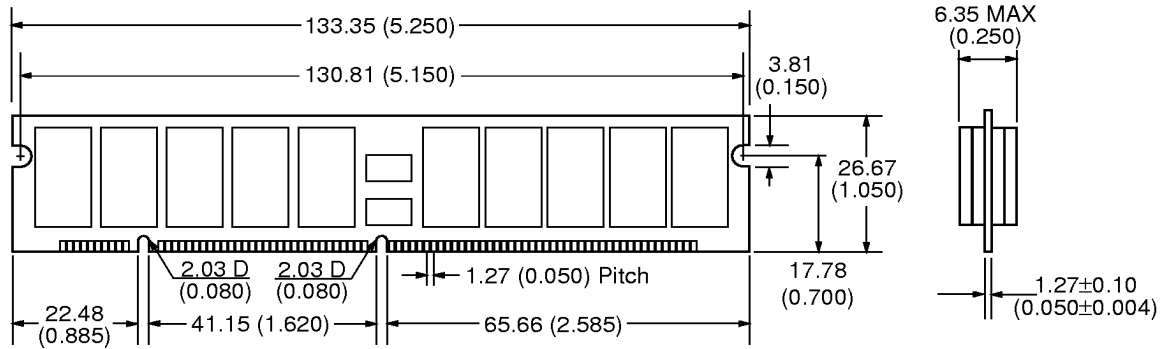
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AC CHARACTERISTICS (continued)

Notes

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF, $V_{OH}=2.0\text{V}$ and $V_{OL}=0.8\text{V}$.
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes the $t_{RCD} \geq t_{RCD}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\text{max})$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are non-restrictive operation parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$, and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the WE leading edge in read-write cycles.
11. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. $t_{CEZ}(\text{max})$, $t_{REZ}(\text{max})$, $t_{WEZ}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
13. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
14. $t_{ASC} \geq t_{CP}(\text{min})$.
15. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

**PACKAGE: 168-PIN DIMM**

±0.13 (±0.005) TOLERANCE UNLESS OTHERWISE SPECIFIED

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHEMICALLY IN INCHES

ORDERING INFORMATION

W P D E 8M72 V - X M D C X

LEAD FINISH:

T = Tin Edge Connectors

Blank = Gold Edge Connectors

DEVICE GRADE:

C = Commercial

0 to + 70°C

PACKAGE TYPE:

MD = 168 pin DIMM

ACCESS TIME (ns)

3.3V ± 0.3V Supply Voltage

ORGANIZATION, 8M x 72

E = Extended Data Out Mode (EDO)

DRAM

Plastic Module

WHITE MICROELECTRONICS