

TEXAS INSTR (ASIC/MEMORY)

CMS209, CMS210, CMS212,
CMS213, CMS214, CMS216
CMOS OTP PROM MEMORY CARDS

SMNS209A—JUNE 1991—REVISED JANUARY 1993

- Card Size (85 mm × 54 mm × 3.6 mm)
- Organization . . . From 64K × 8 to 256K × 16
- Single 5-V Power Supply (Read Mode)
- Utilizes QFP (Quad Flat Package) CMOS OTP PROMs (One Time Programmable Read-Only Memories)
- 8-Bit or 16-Bit Data Width
- Low Power Dissipation
- Operating Free-Air Temperature Range 0°C to 55°C
- Standard 60-Pin Two-Piece Connector With Orientation Guide Allows Memory Technology/Capacity Upgrade/Downgrade
- All Inputs/Outputs and Clocks are Fully TTL Compatible
- 3-State Output
- Performance Ranges:
CMS2xx-200 200 ns Access Time (Max)
CMS2xx-250 250 ns Access Time (Max)

description

The CMS2xx series are TI standard Memory Cards designed to be used either as an internal memory system or as an external add-on memory.

These cards are offered with densities of 512K to 4 Megabit, one time electrically programmable read-only memories organized from 65 536 × 8 bits to 262 144 × 16 bits in a standard card package. A card is comprised of from 1 to 8 TMS27PC512s in 44-lead plastic quad flat packages (QFP) and one decoder in a 16-pin small outline package (SOP) mounted on top of the substrate together with three 0.1 μF decoupling capacitors.

The TMS27PC512 is described in the TMS27PC512 data sheet and is electrically tested and processed according to TI's MIL-STD-883B (as amended for commercial applications) flows prior to assembly.

60-PIN MEMORY CARD
(CONNECTOR VIEW)

NC	1	□	□	2	NC
NC	3	□	□	4	NC
A12	5	□	□	6	CD1
A7	7	□	□	8	A15
A6	9	□	□	10	A16
A5	11	□	□	12	A17
A4	13	□	□	14	NC
A3	15	□	□	16	NC
A2	17	□	□	18	NC
A1	19	□	□	20	NC
A0	21	□	□	22	NC
D0	23	□	□	24	D8
D1	25	□	□	26	D9
D2	27	□	□	28	D10
GND	29	□	□	30	GND
D3	31	□	□	32	GND
D4	33	□	□	34	D11
D5	35	□	□	36	D12
D6	37	□	□	38	D13
D7	39	□	□	40	D14
OE	41	□	□	42	D15
A10	43	□	□	44	NC
OE/Vpp	45	□	□	46	NC
A11	47	□	□	48	NC
A9	49	□	□	50	NC
A8	51	□	□	52	NC
A13	53	□	□	54	NC
A14	55	□	□	56	NC
NC	57	□	□	58	CD2
VCC	59	□	□	60	VCC

PIN NOMENCLATURE

A0-A17	Address Input†
D0-D15	Data Output‡
CE	Card Enable
OE / Vpp	Output Enable/Programming Voltage
CD1, CD2	Card Detect
GND	Ground
VCC	5-V Power Supply
NC	No Connection

† Address signal A17 (pin12) is not connected for CMS209/213 and CMS210/214 cards. Address Signal A16 (pin 10) is not connected for CMS209/213 cards.

‡ Data out signals D8-D15 are not connected for all memory cards CMS213/214/216 organized by 8.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**CMS209, CMS210, CMS212,
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CMOS OTP PROM MEMORY CARDS**

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PRODUCT LIST	MEMORY CAPACITY (KB)	ORGANIZATION	ACCESS TIME (ns)	CONNECTOR TYPE
CMS209	128	64K × 16	200/250	Two-piece 60-pin
CMS210	256	128K × 16	200/250	Two-piece 60-pin
CMS212	512	256K × 16	200/250	Two-piece 60-pin
CMS213	64	64K × 8	200/250	Two-piece 60-pin
CMS214	128	128K × 8	200/250	Two-piece 60-pin
CMS216	256	256K × 8	200/250	Two-piece 60-pin

operation

The CMS2xx series operates as an array of TMS27PC512s and one decoder connected as shown in the functional block diagrams. The most significant address lines A16 and A17 are used to select one of the four possible device pairs. There are seven modes of operation listed in the following table.

programming

The CMS2xx series can be programmed using the TI SNAP! Pulse programming algorithm; refer to the TI TMS27PC512 data sheet for details of its operation.

FUNCTION	MODE						
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAMMING INHIBIT	SIGNATURE MODE
CE	V _{IL}	V _{IL}	V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IL}
OE/V _{PP}	V _{IL}	V _{IH}	X	V _{PP}	V _{IL}	V _{PP}	V _{IL}
V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
A9	X†	X	X	X	X	X	V _H ‡
A0	X	X	X	X	X	X	V _{IL}
D0–D7	Data Out	HI–Z	HI–Z	Data In	Data Out	HI–Z	CODE
							MFG
							97
D8–D15	Data Out	HI–Z	HI–Z	Data In	Data Out	HI–Z	85

† X can be V_{IL} or V_{IH}.

‡ V_H = 12 V ± 0.5 V.

Refer to the appropriate TMS27PC512 data sheet for details of its operation.

This card has a device recognition mode.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[§]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	–0.5 V to 14 V
Input voltage range (see Note 1): All inputs except A9	–0.5 V to 6.5 V
A9	–0.5 V to 13.5 V
Output voltage range (see Note 1)	–0.5 V to V_{CC}
Operating free-air temperature range	0°C to 55°C
Storage temperature range	–40°C to 70°C
Connector insertion cycle	5000

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT		
V _{CC}	Supply voltage	Read mode (see Note 2)		4.75	5	5.25	V
		Fast programming algorithm		5.75	6	6.25	V
		SNAPI Pulse programming algorithm		6.25	6.5	6.75	V
OE/V _{PP}	Supply voltage	Fast programming algorithm		12	12.5	13	V
		SNAPI Pulse programming algorithm		12.75	13.0	13.25	V
V _{IH}	High-level input voltage	2		V _{CC}		V	
V _{IL}	Low-level input voltage	0		0.8		V	
T _A	Operating free-air temperature	0		55		°C	

NOTE 2: V_{CC} must be applied before or at the same time as $\overline{OE}/V_{PP}$ and removed after or at the same time as $\overline{OE}/V_{PP}$.

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -400 mA	2.4		V
V _{OL}	Low-level output voltage	I _{OL} = 2.1 mA		0.45	V
I _I	Input current (leakage)	V _I = 0 to 5.5 V		±10	μA
I _{OZH}	High-level output current (leakage)	All address inputs, $\overline{CE}$ or $\overline{OE}$ = V _{IH} , V _O = V _{CC}		+10	μA
I _{OZL}	Low-level output current (leakage)	$\overline{CE}$ or $\overline{OE}$ = V _{IH} , V _O = 0 V		-10	μA

PARAMETER		TEST CONDITIONS	CMS209	CMS210	CMS212	UNIT
I _{PP}	$\overline{OE}$ /V _{PP} supply current (during program pulse)	V _{PP} = 13 V	100	100	100	mA
I _{CC1}	V _{CC} supply current (standby)	TTL-input level $\overline{CE}$ = V _{IH} V _{CC} = 5.5 V	8	16	32	mA
		CMOS-input level $\overline{CE}$ = V _{CC} V _{CC} = 5.5 V	7	14	28	mA
I _{CC2}	V _{CC} supply current (active)	V _{CC} = 5.5 V, $\overline{CE}$ = V _{IL} , t _{cycle} = minimum cycle time, outputs open, address not complemented	100	100	100	mA

PARAMETER		TEST CONDITIONS	CMS213	CMS214	CMS216	UNIT
I _{PP}	$\overline{OE}$ /V _{PP} supply current (during program pulse)	V _{PP} = 13 V	50	50	50	mA
I _{CC1}	V _{CC} supply current (standby)	TTL-input level $\overline{CE}$ = V _{IH} V _{CC} = 5.5 V	4	8	16	mA
		CMOS-input level $\overline{CE}$ = V _{CC} V _{CC} = 5.5 V	3.5	7	14	mA
I _{CC2}	V _{CC} supply current (active)	V _{CC} = 5.5 V, $\overline{CE}$ = V _{IL} , t _{cycle} = minimum cycle time, outputs open, address not complemented	50	50	50	mA

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4)

PARAMETER	TEST CONDITIONS (SEE NOTES 3 AND 4)	CMS2xx-200		CMS2xx-250		UNIT
		MIN	MAX	MIN	MAX	
$t_a(A)$ Access time from address	$C_L = 100$ PF, 1 Series 74 TTL load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		200		250	ns
$t_{(CE)}$ Access time from chip enable			200		250	ns
$t_{en(OE/VPP)}$ Output enable time from $\overline{OE}/V_{PP}$			75		120	ns
t_{dis} Output disable time from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first†		0	80	0	80	ns
$t_{v(A)}$ Output data valid time after change of address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurs first†		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

NOTES: 3. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low.

4. Common test conditions apply for the t_{dis} except during programming.**capacitance over recommended ranges of supply voltage and operating free-air temperature
 $f = 1$ MHz‡**

PARAMETER		TEST CONDITIONS	MAX	UNIT
C_i Input capacitance	CMS213	$V_i = 0$ V $f = 1$ MHz $T_A = 25^\circ\text{C}$	10	pF
	CMS209		20	
	CMS214		20	
	CMS210		40	
	CMS216		40	
	CMS212		80	
$C_{i(OE/VPP)}$ Input capacitance, output enable/programming voltage	CMS213	$V_i = 0$ V $f = 1$ MHz $T_A = 25^\circ\text{C}$	25	pF
	CMS209		50	
	CMS214		50	
	CMS210		100	
	CMS216		100	
	CMS212		200	
C_o Output capacitance	CMS213	$V_O = 0$ V $f = 1$ MHz $T_A = 25^\circ\text{C}$	15	pF
	CMS209		15	
	CMS214		30	
	CMS210		30	
	CMS216		60	
	CMS212		60	

‡ Capacitance measurements are made on sample basis only.

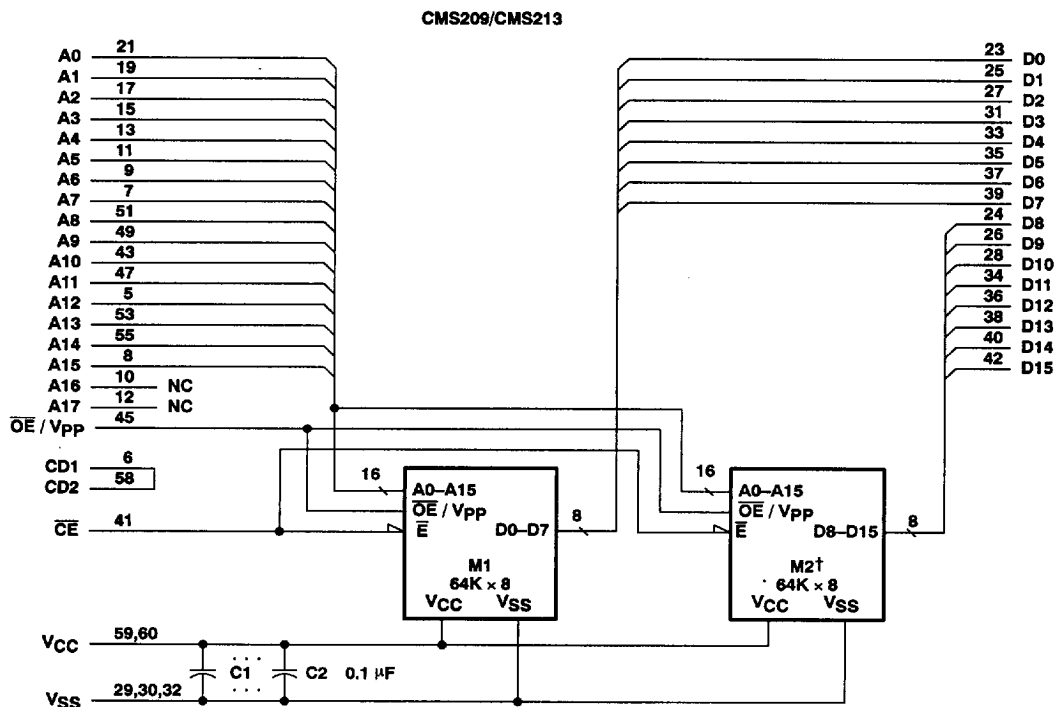
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functional block diagram

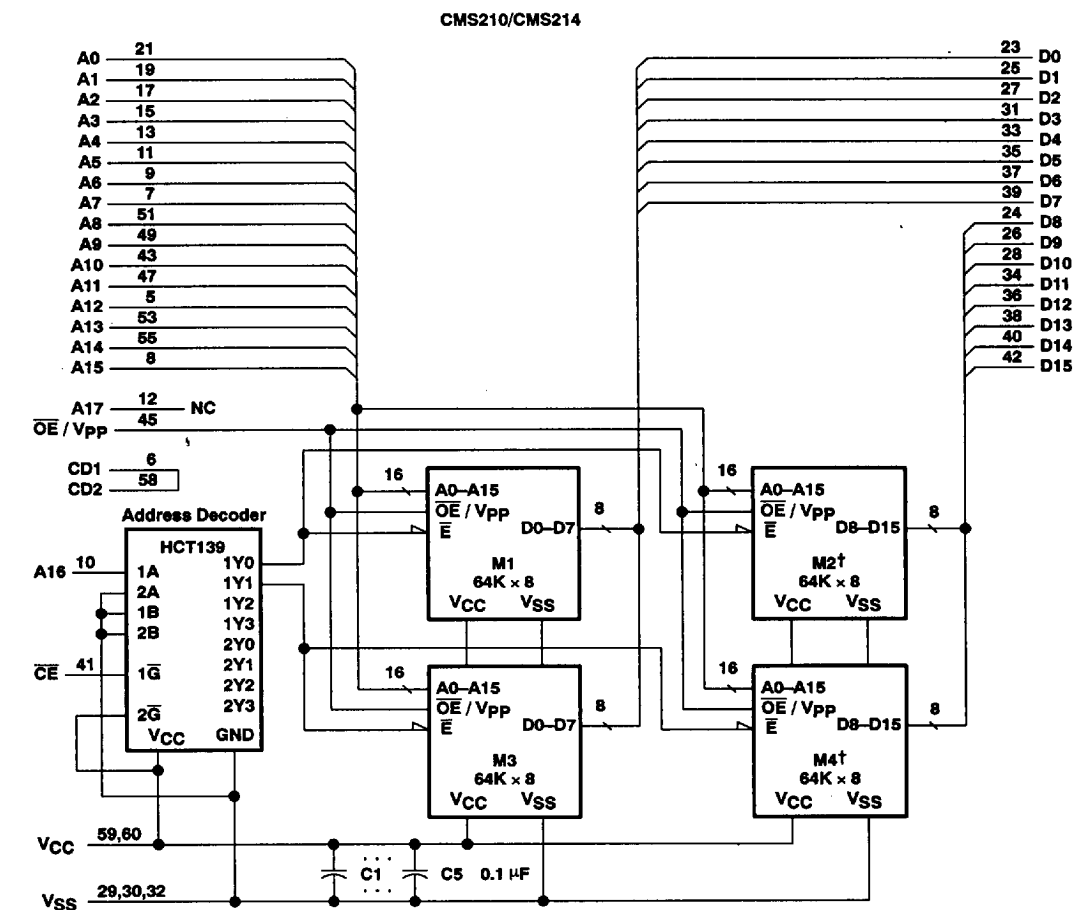


† Memory device M2 is used for CMS209 only.

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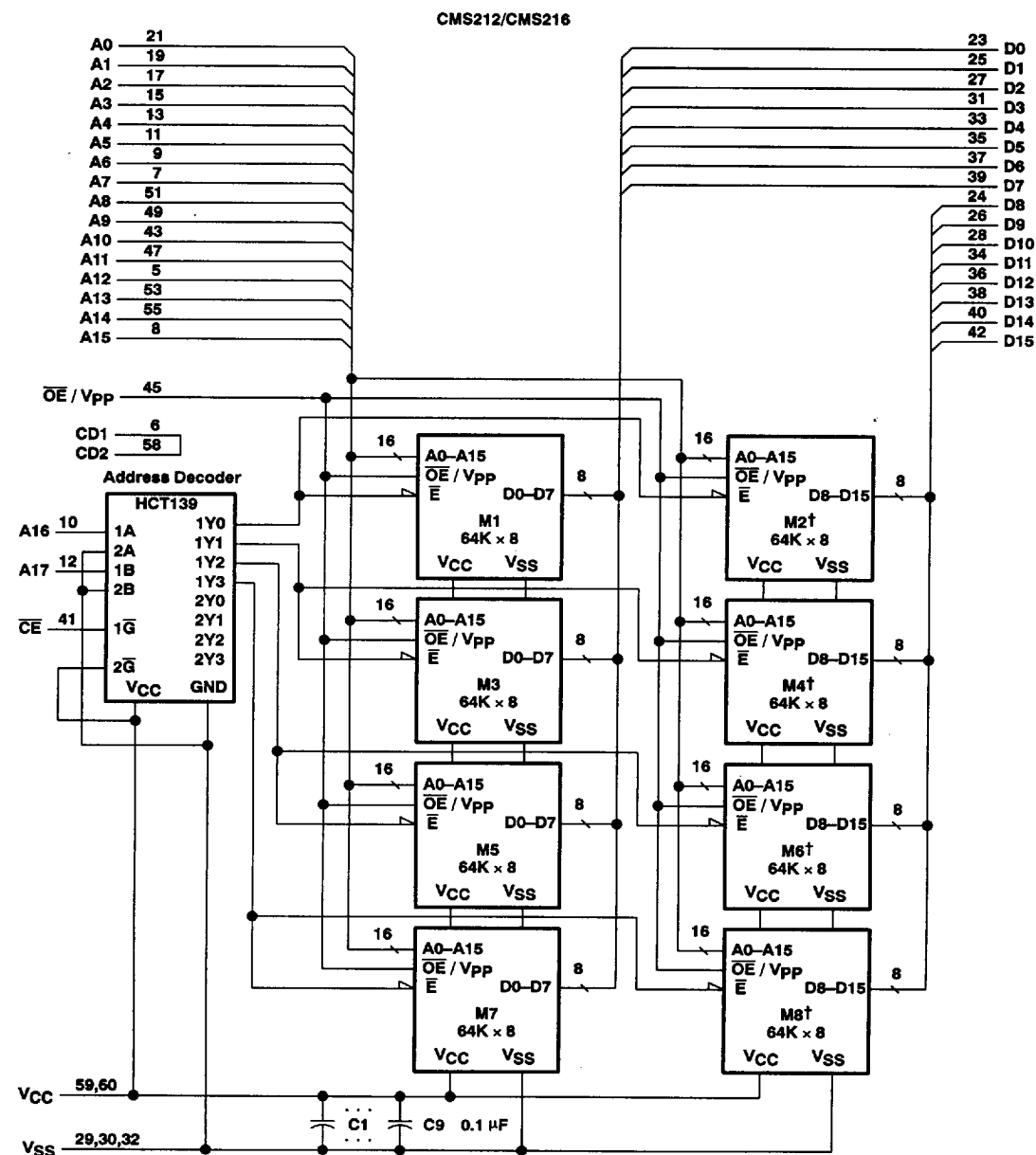
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functional block diagram



† Memory devices M2 and M4 are used for CMS210 only.

functional block diagram



† Memory devices M2, M4, M6 and M8 are used for CMS212 only.