



WPF512K8-XXX

512Kx8 MONOLITHIC FLASH

PRELIMINARY*

FEATURES

■ Packaging

- 32 Lead, Plastic J-Leaded Chip Carrier PLCC
- 32 Lead, Plastic Thin Small Outline Package TSOP

- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range

- **Electrical and Speed Characteristics for:**

- Military Temperature (-55°C to +125°C)
- Industrial Temperature (-40°C to +85°C)

- Burn-in and Temperature Cycling Available

- 10,000 Erase/Program Cycles

- ## ■ Sector Erase Architecture

- 8 equal size sectors of 64K bytes each
 - Any combination of sectors can be concurrently erased.
- Also supports full chip erase

- Organized as 512Kx8

- 5 Volt Programming. 5V $\pm$ 10% Supply.

- Low Power CMOS, 30mA Read Current, Typical

- ## ■ Embedded Erase and Program Algorithms

- ### ■ TTL Compatible Inputs and CMOS Outputs

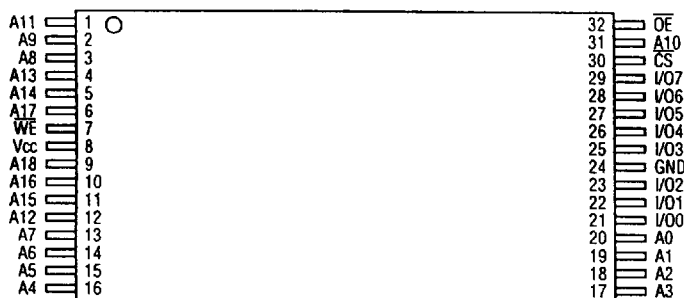
- Page Program Operation and Internal Program Control Time.

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

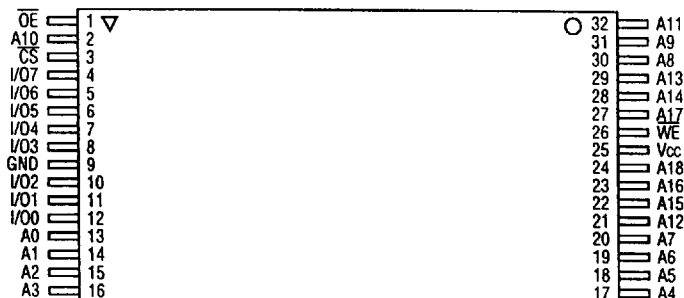
Note: Programming information available upon request.

PIN CONFIGURATIONS

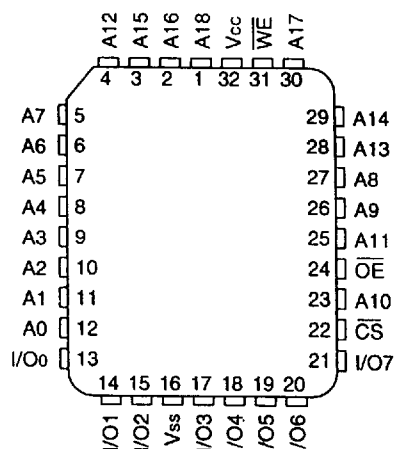
**32 TSOP (STANDARD)
TOP VIEW**



32 TSOP (REVERSE) TOP VIEW



32 PLCC TOP VIEW



PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
$\overline{\text{CS}}$	Chip Select
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
Vcc	+5.0V Power
Vss	Ground

**ABSOLUTE MAXIMUM RATINGS**

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage (Vcc) (1)	-2.0 to +7.0	V
Signal Voltage Range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention	10 years	
Endurance (erase/program cycles)	10,000	
A9 Voltage for sector protect (Vio) (3)	-2.0 to +14.0	V

NOTES:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot Vss to -2.0 V for periods of up to 20nS. Maximum DC voltage on output and I/O pins is Vcc + 0.5V. During voltage transitions, outputs may overshoot to Vcc + 2.0 V for periods of up to 20nS.
3. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20nS. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20nS.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	Vcc + 0.5	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C
A9 Volatage for Sector Protect	V _{IO}	11.5	12.5	V

CAPACITANCE(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C _{AD}	V _{IO} = 0 V, f = 1.0 MHz	15	pF
Output Enable capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Write Enable capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Chip Select capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C _{I/O}	V _{IO} = 0 V, f = 1.0 MHz	15	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE(Vcc = 5.0V, Vss = 0V, T_A = -55°C to +125°C)

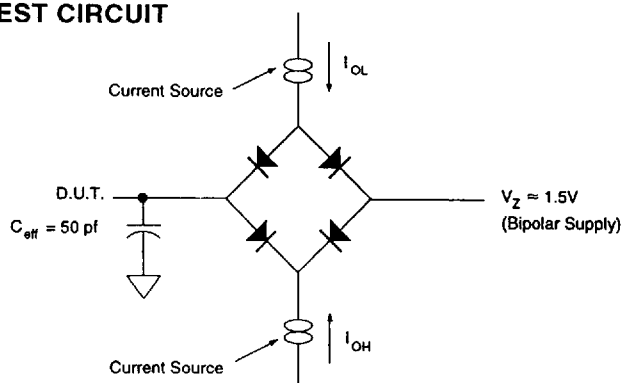
Parameter	Symbol	Conditions	Min		Unit
				Max	
Input Leakage Current	I _{LI}	Vcc = 5.5, V _{IN} = GND to Vcc		10	μA
Output Leakage Current	I _{LOx32}	Vcc = 5.5, V _{IN} = GND to Vcc		10	μA
Vcc Active Current for Read (1)	I _{CC1}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}$		50	mA
Vcc Active Current for Program or Erase (2)	I _{CC2}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$		60	mA
Vcc Standby Current	I _{CC4}	Vcc = 5.5, $\overline{CS} = V_{IH}, f = 5\text{MHz}$		1.6	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, Vcc = 4.5		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, Vcc = 4.5	0.85 x Vcc		V
Low Vcc Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc - 0.3V

**AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED**
($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max			
Write Cycle Time	t _{AVAV}	t _{WC}	70		90		120		150		nS
Write Enable Setup Time	t _{WLEL}	t _{WS}	0		0		0		0		nS
Chip Select Pulse Width	t _{ELEH}	t _{CP}	45		45		50		50		nS
Address Setup Time	t _{AVEL}	t _{AS}	0		0		0		0		nS
Data Setup Time	t _{DVEH}	t _{DS}	45		45		50		50		nS
Data Hold Time	t _{ENDX}	t _{DH}	0		0		0		0		nS
Address Hold Time	t _{ELAX}	t _{AH}	45		45		50		50		nS
Chip Select Pulse Width High	t _{ENEL}	t _{CPH}	20		20		20		20		nS
Duration of Byte Programming Operation	t _{WHWH1}		16		16		16		16		μS
Sector Erase Time	t _{WHWH2}			30		30		30		30	Sec
Read Recovery Time	t _{GHEL}		0		0		0		0		μS
Chip Programming Time				50		50		50		50	Sec
Chip Erase Time	t _{WHWH2}			120		120		120		120	Sec

AC TEST CIRCUIT**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	70		90		120		150		nS
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		0		nS
Write Enable Pulse Width	t _{WLWH}	t _{WP}	45		45		50		50		nS
Address Setup Time	t _{AVWH}	t _{AS}	0		0		0		0		nS
Data Setup Time	t _{DVWH}	t _{DS}	45		45		50		50		nS
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		nS
Address Hold Time	t _{WHAX}	t _{AH}	45		45		50		50		nS
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		20		nS
Duration of Byte Programming Operation	t _{WHWH1}		16		16		16		16		μS
Sector Erase Time	t _{WHWH2}			30		30		30		30	Sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		0		μS
V _{CC} Set-up Time	t _{VCS}		50		50		50		50		μS
Chip Programming Time				50		50		50		50	Sec
Output Enable Setup Time		t _{OES}	0		0		0		0		nS
Output Enable Hold Time (1)		t _{OEH}	10		10		10		10		nS
Chip Erase Time	t _{WHWH2}			120		120		120		120	Sec

1. For Toggle and Data Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

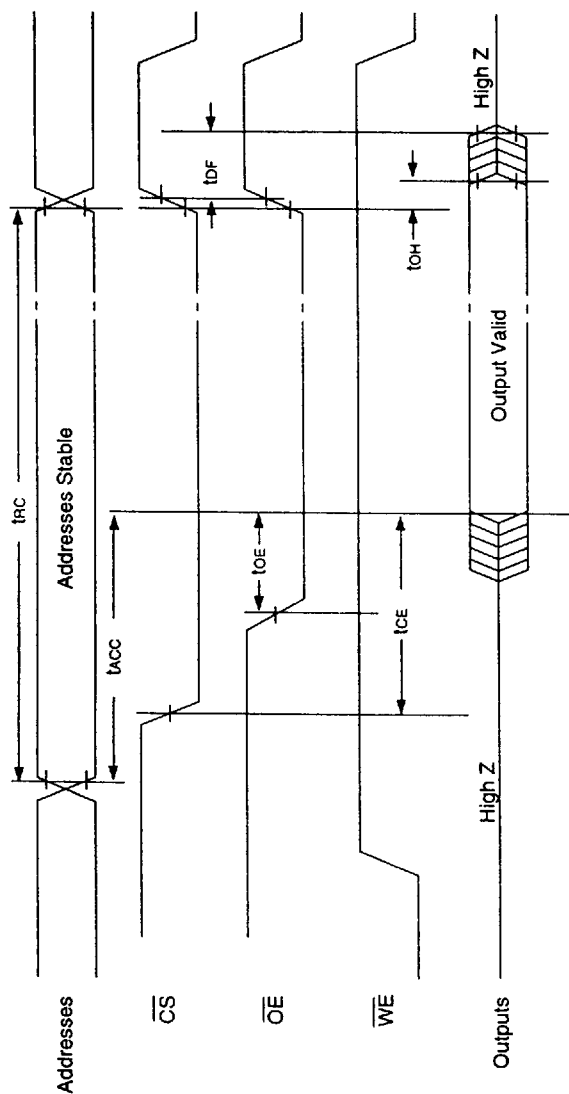
(V_{CC} = 5.0V, T_A = -55°C to +125°C)

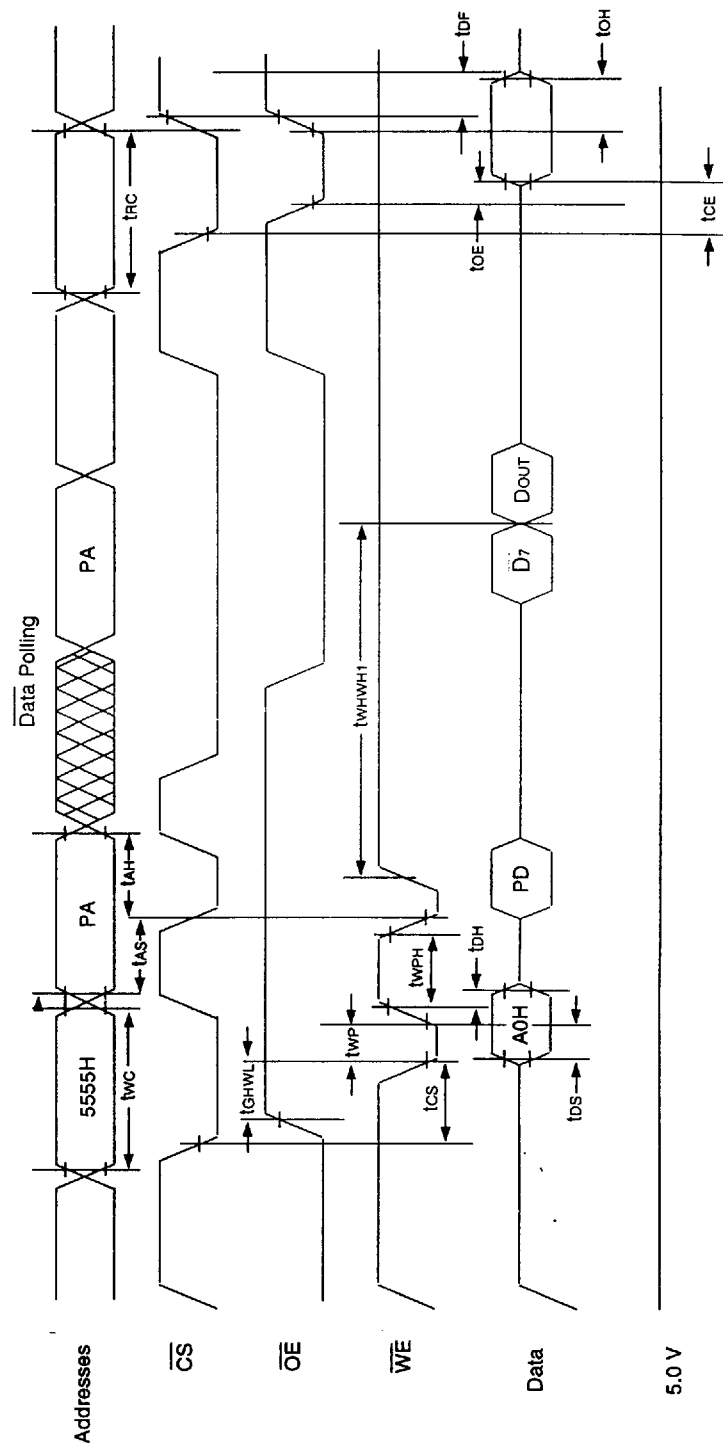
Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	70		90		120		150		nS
Address Access Time	t _{AVQV}	t _{ACC}		70		90		120		150	nS
Chip Select Access Time	t _{ELQV}	t _{CE}		70		90		120		150	nS
Output Enable to Output Valid	t _{GLQV}	t _{OE}		35		35		50		55	nS
Chip Select to Output High Z (1)	t _{EHQZ}	t _{DF}		20		20		30		35	nS
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		20		30		35	nS
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		0		nS

1. Guaranteed by design, but not tested

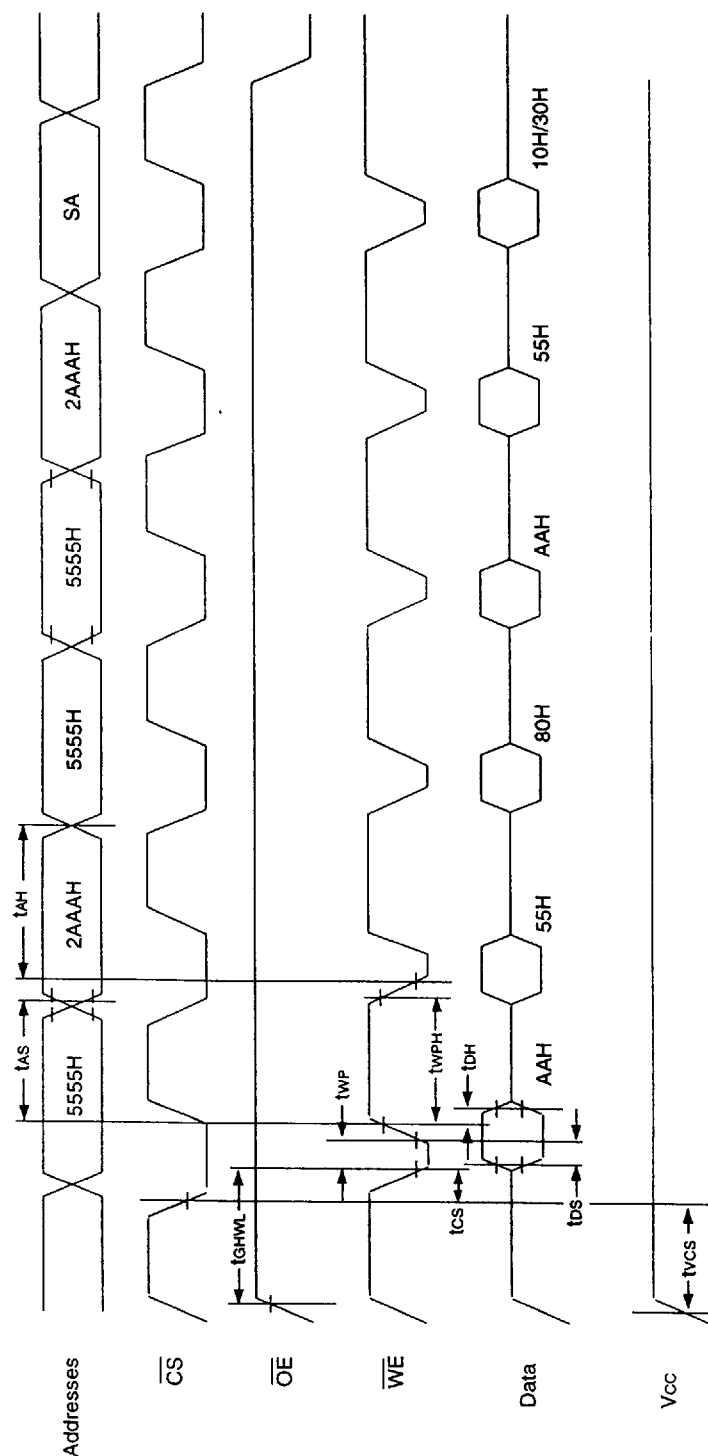


AC WAVEFORMS FOR READ OPERATIONS

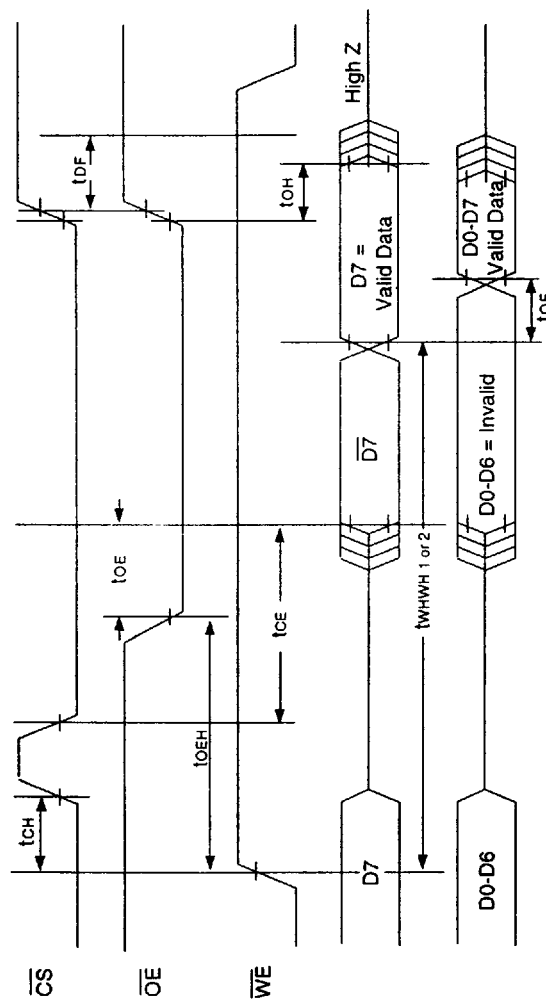


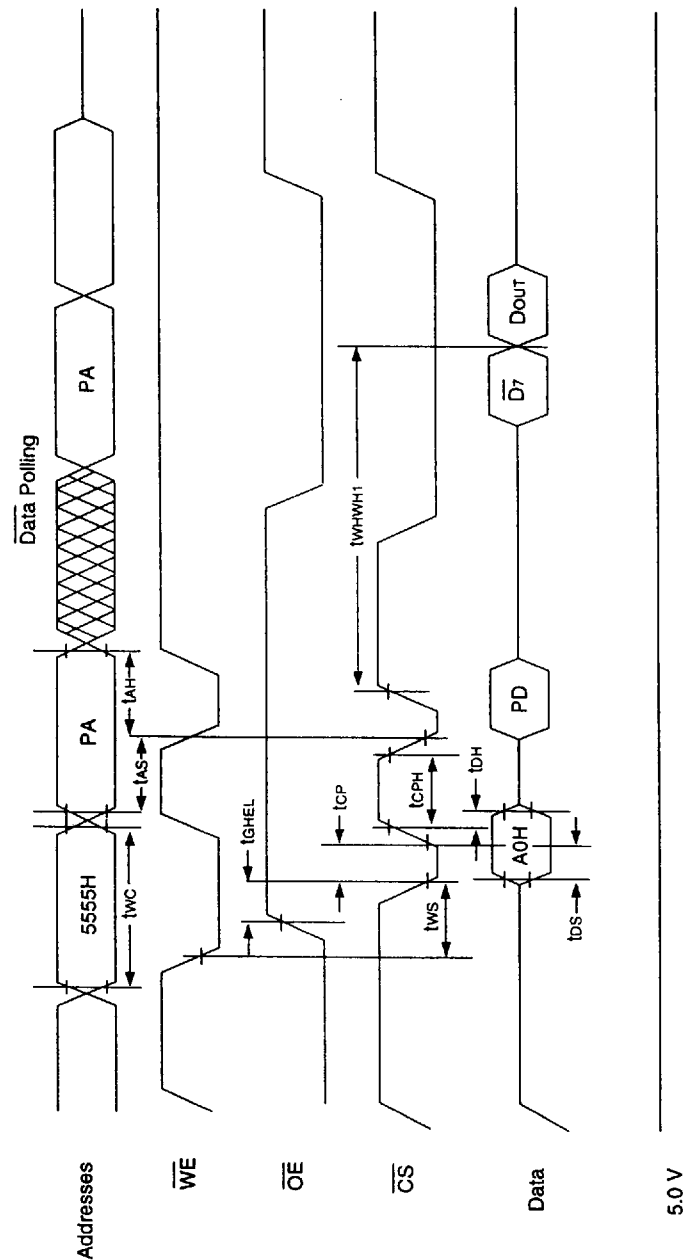
**WRITE/ERASE/PROGRAM
OPERATION, WE CONTROLLED****NOTES:**

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. Dout is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

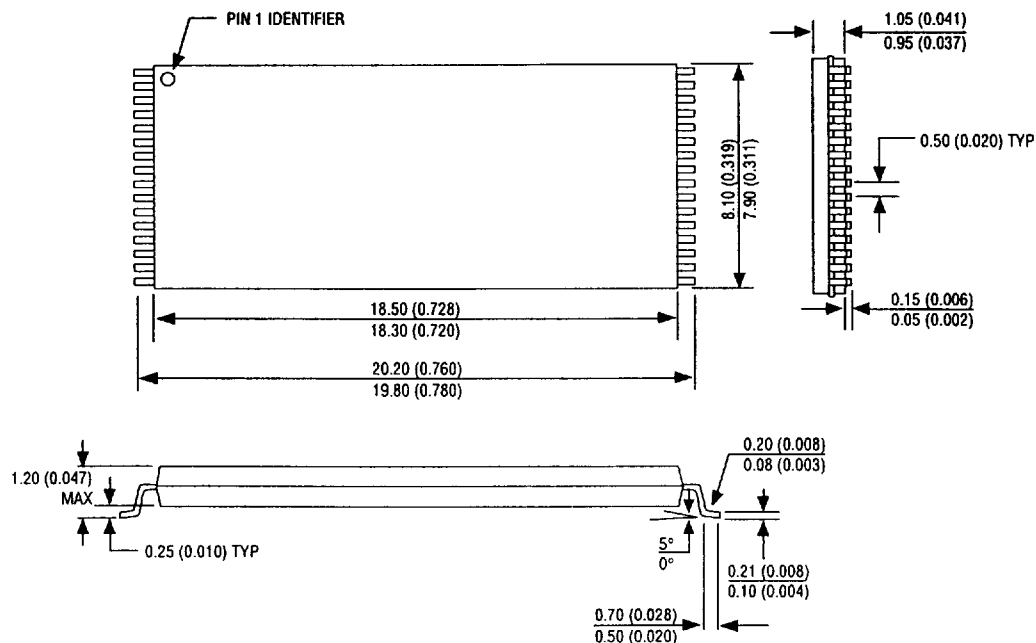
**AC WAVEFORMS CHIP/SECTOR
ERASE OPERATIONS****NOTE:**

1. SA is the sector address for Sector Erase.

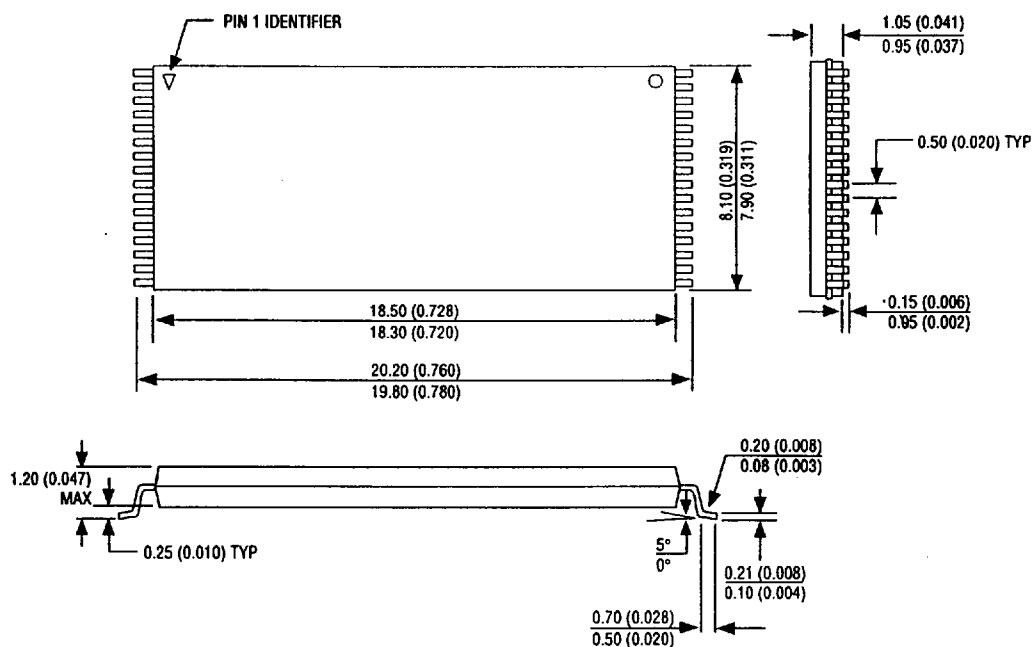
**AC WAVEFORMS FOR DATA POLLING
DURING EMBEDDED ALGORITHM OPERATIONS**

**ALTERNATE CS CONTROLLED
PROGRAMMING OPERATION TIMINGS****NOTES:**

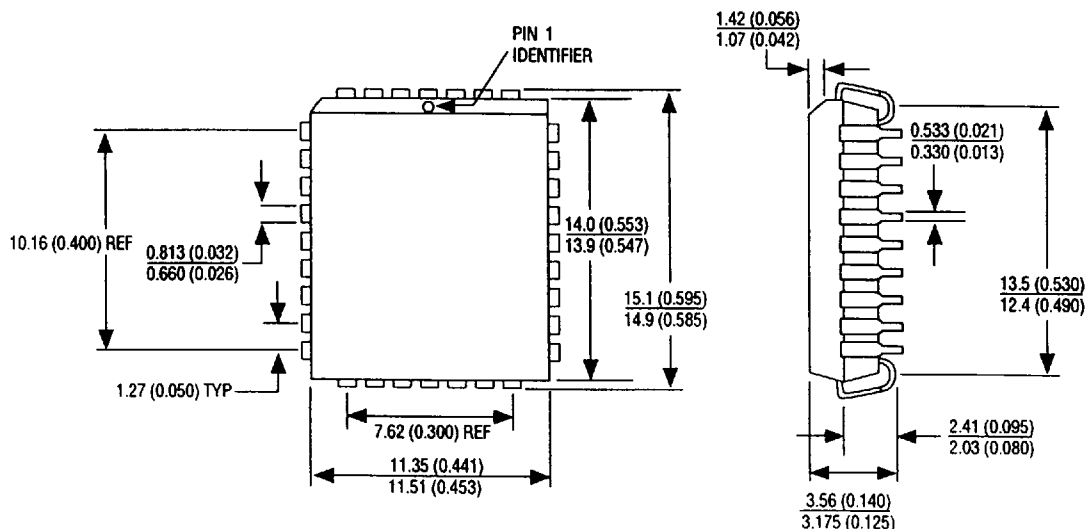
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. Dout is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

**32 LEAD, STANDARD PLASTIC TSOP PACKAGE DIMENSION**

DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, REVERSED PLASTIC TSOP PACKAGE DIMENSION

DIMENSIONS IN MILLIMETERS AND (INCHES)

**32 LEAD, PLASTIC J-LEADED PLCC PACKAGE DIMENSION**

DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION**W P F 512K 8 X - XXX X X****DEVICE GRADE:**

M = Military Temperature -55°C to +125°C

I = Industrial Temperature -40°C to +85°C

PACKAGE:

TF = 32 lead Plastic TSOP

TR = 32 lead Plastic TSOP Reverse

PL = 32 lead Plastic LCC (J-lead)

ACCESS TIME in nS**IMPROVEMENT MARK**

B = Burn-in

T = Temperature Cycle

C = Burn-in and Temp Cycle

ORGANIZATION, 512K x 8**FLASH****PLASTIC PLUS™****WHITE MICROELECTRONICS**