CN8331/CN8332/CN8333

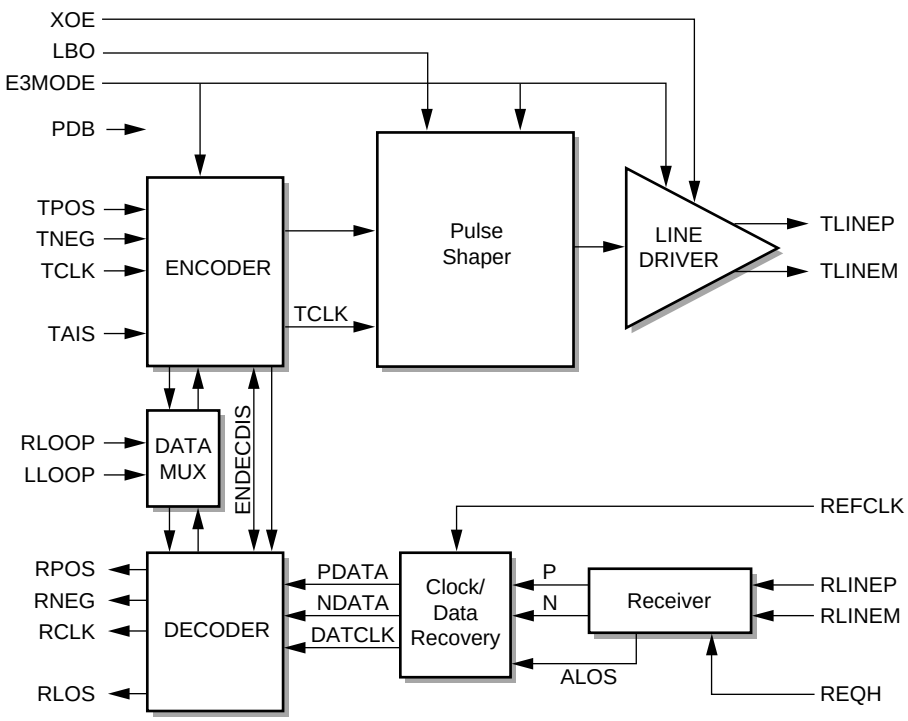
Single/Dual/Triple E3/DS3/STS-1 Line Interface Unit

The CN8333 is a three-channel, E3/DS3/STS-1 fully-integrated Line Interface Unit (LIU). It is configured via external pins and does not need a microprocessor interface. Each channel has an independent equalizer on the receive side requiring no user configuration. Also, each channel has a programmable transmit pulse shaper that can be set to ensure that the cross-connect pulse mask requirement is met for transmit cable length up to 450 feet. The CN8332 is a dual-channel, and the CN8331 is a single-channel LIU with performance identical to the CN8333.

The CN8333 gives the user new economies of scale in concentrator applications where three DS3 or STS-1 channels are concentrated into a single STS-3 channel. By including three independent transceivers on a chip, significant external components are eliminated, with the exception of 1:1 coupling transformers, termination resistors, and supply bypass capacitors.

NOTE: In this document "x" is used to represent the number of channels: x = 1 (CN8331), x = 2 (CN8332), and x = 3 (CN8333).

Functional Block Diagram (only one Channel is shown)



Distinguishing Features

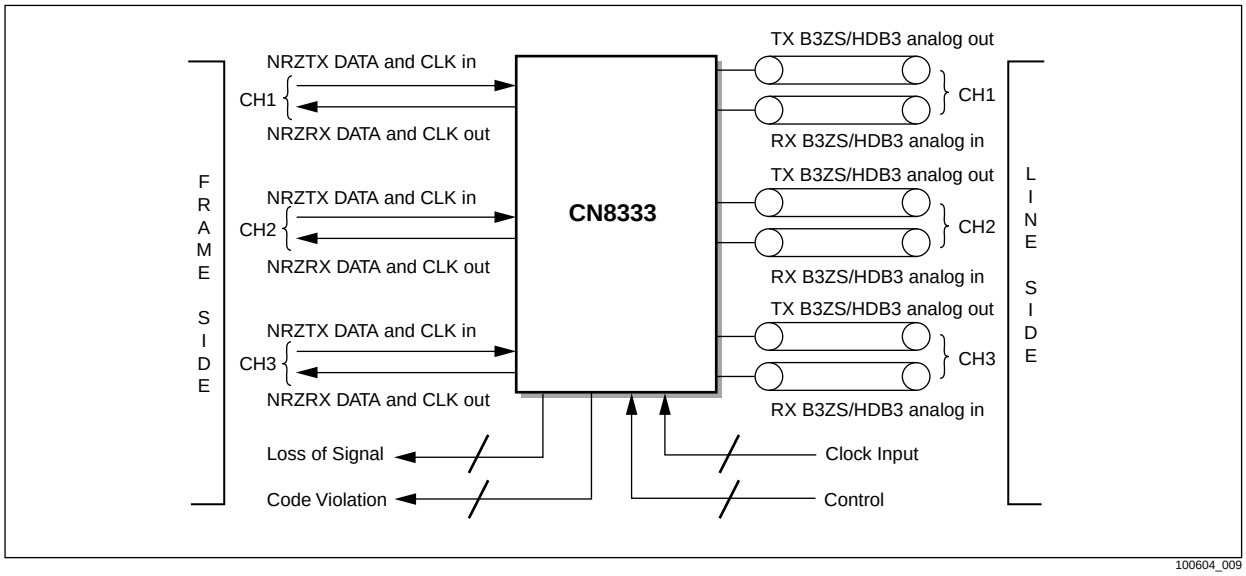
- Can be used as a data transceiver over a maximum of 900 feet of Type 734/728 coaxial cable or equivalent in an on-premise environment
- Programmable pulse filtering to meet cross-connect pulse masks (*ANSI T1.102-1993*)
- Meets jitter specifications of *Bellcore GR499* and GR253
- Large input dynamic range
- Alarms for coding violation and loss of signal
- Full diagnostic loopback capability
- Uses a minimum of external components
- Compatible with *ITU-T G.703, G.823*
- Independent power down mode per channel
- Easily interfaced to the DS3/E3 Framer IC (CN8342/3/4/6/8 and CN8330)
- Selectable B3ZS/HDB3 encoding/decoding
- Superior input receiver sensitivity (< 25mV)

Physical Characteristics

- 80-pin ETQFP package
- Single 3.3 V power supply
- 1 W maximum power dissipation (CN8333)
- –40 °C to +85 °C temperature range
- 5 V-tolerant pins
- TTL digital pins

Applications

- Digital Cross Connect Systems
- Routers
- ATM Switches
- Channelized Line Aggregation Units
- Test Equipment
- Channel Service Units
- Multiplexers



Ordering Information

Model Number	Package	Operating Temperature
CN8331EXF	80-Pin ETQFP	–40 °C to 85 °C
CN8332EXF	80-Pin ETQFP	–40 °C to 85 °C
CN8333EXF	80-Pin ETQFP	–40 °C to 85 °C

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1.0 Pin Description

1.1 Pin Assignments

Figures 1-1 (CN8331), 1-2 (CN8332), and 1-3 (CN8333) illustrate pin assignments for the 80-pin Exposed Thin Quad Flat Package (ETQFP). Table 1-1 lists the pin definitions and gives additional information for each pin. The input/output (I/O) column is coded as follows:

I = Input
O = Output
I/O = Bidirectional
P = Power

When a channel is disabled (i.e., the PDBx pin is tied low or not connected), all receive and transmit analog circuitry powers down. Analog inputs (RLINE) are ignored and analog outputs (TLINE) are high impedance. Digital inputs of a powered-down channel are still active, but ignored. Overall noise on the device can be lowered by not driving the digital inputs of a powered-down channel.

NOTE: When power is disconnected from the device, TLINE pins are low impedance to ground if driven by more than one forward-bias diode voltage (0.7 V) below ground. Additionally, driving TLINE, a forward-bias diode voltage above the VGG pin, creates a low impedance path from the TLINE pin to the VGG pin. Otherwise, the TLINE pins are high impedance.

Figure 1-1. CN8331 Pin Diagram

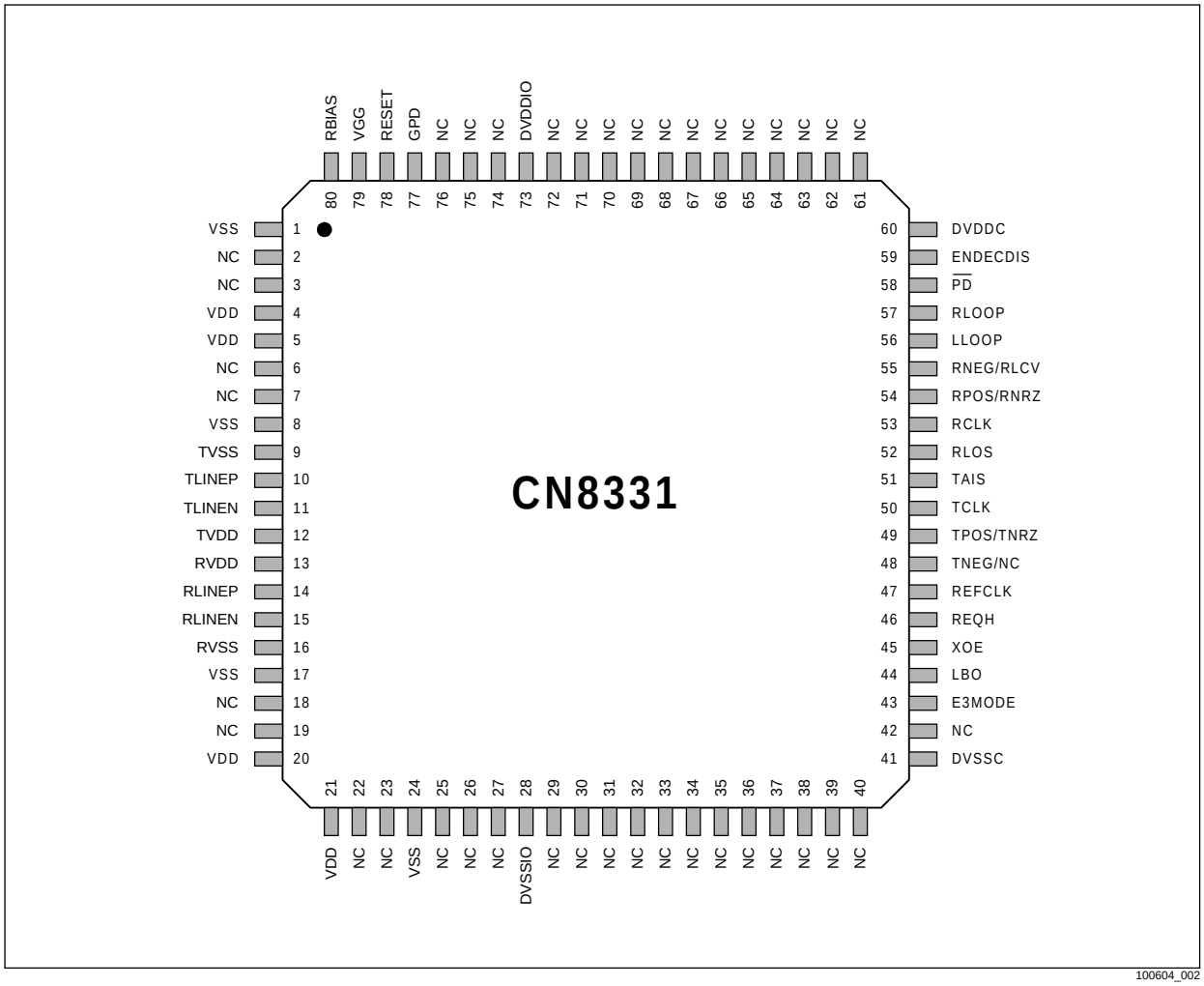

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Figure 1-2. CN8332 Pin Diagram

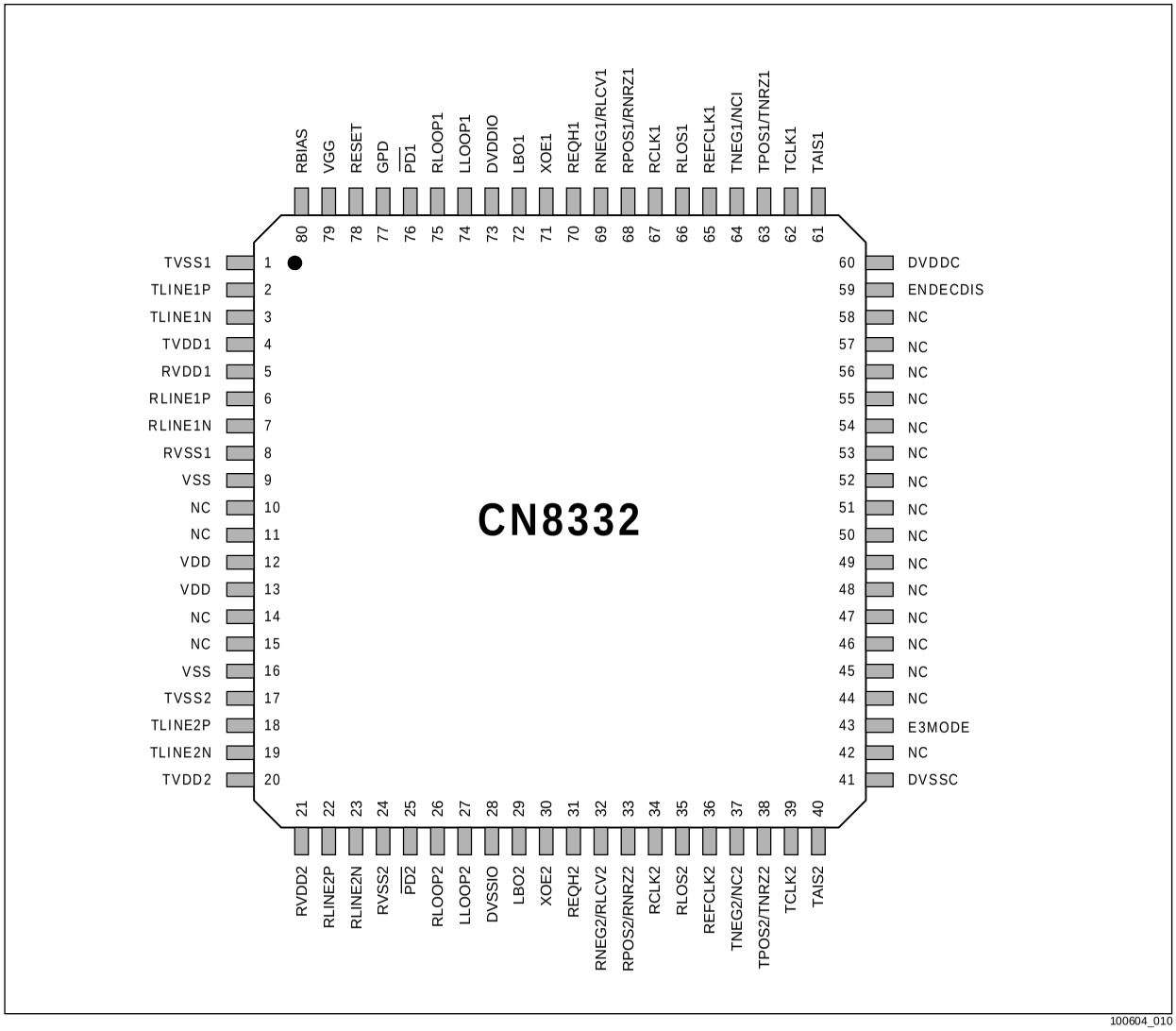

Figure 1-3. CN8333 Pin Diagram

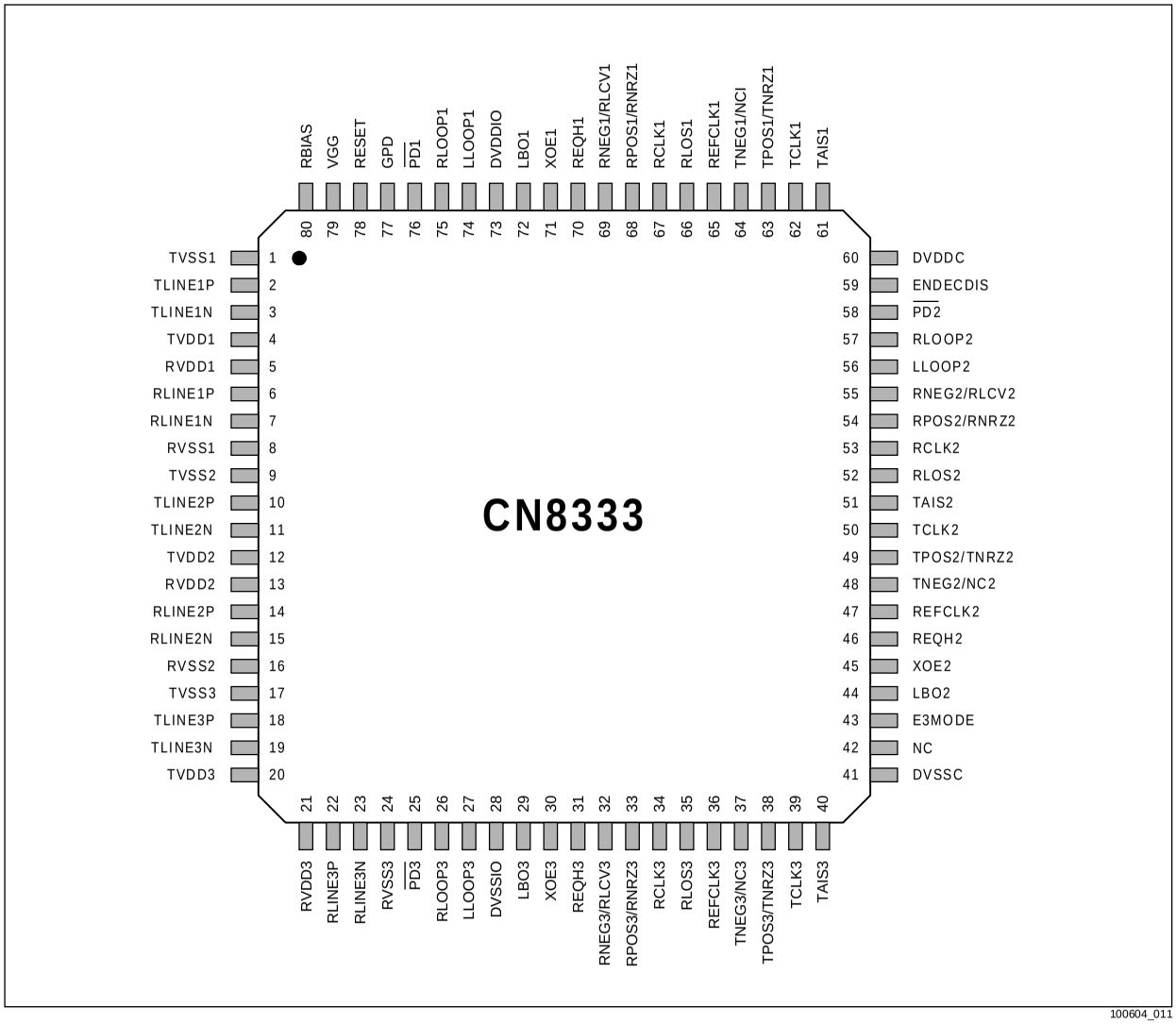

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Table 1-1. CN8331/CN8332/CN8333 Pin Definitions *(1 of 6)*

Pin #			Signal Name	Description	I/O/P	Notes
CN8331	CN8332	CN8333				
Coaxial Line Pins						
14	6	6	RLINEP/ RLINE1P	Line 1 positive receive data	I	Differential inputs for each channel from its respective receive coax line. The RX expects balanced differential inputs, usually achieved using a 1:1 transformer. The inputs are internally DC biased to 1.9 V.
15	7	7	RLINEN/ RLINE1N	Line 1 negative receive data	I	
—	22	14	RLINE2P	Line 2 positive receive data	I	
—	23	15	RLINE2N	Line 2 negative receive data	I	
—	—	22	RLINE3P	Line 3 positive receive data	I	
—	—	23	RLINE3N	Line 3 negative receive data	I	
10	2	2	TLINEP/ TLINE1P	Line 1 positive transmit data	O	Differential, coax-driver balanced outputs for pulse-shaped AMI B3ZS/HDB3 encoded waveforms for each channel. These pins should be connected to the primary side of the 1:1 transformer through two backmatch resistors (see Appendix B).
11	3	3	TLINEN/ TLINE1N	Line 1 negative transmit data	O	
—	18	10	TLINE2P	Line 2 positive transmit data	O	
—	19	11	TLINE2N	Line 2 negative transmit data	O	
—	—	18	TLINE3P	Line 3 positive transmit data	O	
—	—	19	TLINE3N	Line 3 negative transmit data	O	
Digital Data Pins						
54	68	68	RPOS/ RPOS1/ RNRZ/ RNRZ1	RX1 AMI + data/ NRZ data output	O	Resynchronized receive data intended to be strobed out by the corresponding RCLK. When ENDECDIS = 1, these outputs are positive and negative AMI data (RPOS and RNEG). When ENDECDIS = 0, these outputs are decoded NRZ data (RNRZ) and line code violation (RLCV). A line code violation is indicated when RLCV = 1. See notes on the ENDECDIS pin, next page.
55	69	69	RNEG/ RNEG1/ RLCV/ RLCV1	RX1 AMI – data/line code violation	O	
—	33	54	RPOS2/ RNRZ2	RX2 AMI + data/ NRZ data output	O	
—	32	55	RNEG2/ RLCV2	RX2 AMI – data/line code violation	O	
—	—	33	RPOS3/ RNRZ3	RX3 AMI + data/ NRZ data output	O	
—	—	32	RNEG3/ RLCV3	RX3 AMI – data/line code violation	O	

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Table 1-1. CN8331/CN8332/CN8333 Pin Definitions *(2 of 6)*

Pin #			Signal Name	Description	I/O/P	Notes
CN8331	CN8332	CN8333				
53	67	67	RCLK/ RCLK1	Receive clock Ch1	O	Recovered clock for each channel receiver, intended for strobing the corresponding RDAT into the following framer or logic.
—	34	53	RCLK2	Receive clock Ch2	O	
—	—	34	RCLK3	Receive clock Ch3	O	
49	63	63	TPOS/ TPOS1/ TNRZ/ TNRZ1	Ch1 transmit Positive rail or NRZ data	I	Synchronized transmit data intended to be strobed in by the corresponding TCLK. When ENDECDIS = 1, these inputs are expected to be positive and negative AMI data (TPOS and TNEG). When ENDECDIS = 0, these inputs are expected to be uncoded NRZ data (TNRZ) and no connects (NC). See notes on the ENDECDIS pin.
48	64	64	TNEG/ TNEG1/ NC/ NC1	Ch1 transmit Negative rail or no connect data	I	
—	38	49	TPOS2/ TNRZ2	Ch2 transmit Positive/NRZ data	I	
—	37	48	TNEG2/ NC2	Ch2 transmit Negative data	I	
—	—	38	TPOS3/ TNRZ3	Ch3 transmit Positive/NRZ data	I	
—	—	37	TNEG3/ NC3	Ch3 transmit Negative data	I	
50	62	62	TCLK/ TCLK1	Transmit clock Ch1	I	Transmit bit clock input for strobing with transmit data into the CN833x.
—	39	50	TCLK2	Transmit clock Ch2	I	
—	—	39	TCLK3	Transmit clock Ch3	I	
52	66	66	RLOS/ RLOS1	Loss of signal Ch1	O	Loss Of Signal (LOS) indication for each channel, as determined by insufficient pulse density. Signal loss detected when RLOS = 1. An LOS will be asserted when 175±75 zeros occur in a row and deasserted when the pulse density is between 28% and 33% (DS3/STS-1) (i.e., a 1's density).
—	35	52	RLOS2	Loss of signal Ch2	O	
—	—	35	RLOS3	Loss of signal Ch3	O	

Table 1-1. CN8331/CN8332/CN8333 Pin Definitions *(3 of 6)*

Pin #			Signal Name	Description	I/O/P	Notes
CN8331	CN8332	CN8333				
Control Signals						
59	59	59	ENDECDIS	Encoder/decoder disable (for all channels)	I	1 = Dual rail pulse coded data format. Input transmit data pins TPOS, TNRZ, TNEG and NC are interpreted as TPOS and TNEG (encoded positive and negative rail data). Output receive data pins RPOS and RNRZ, and RNEG and RLCV are interpreted as RPOS and RNEG, with RPOS having a positive pulse in place of every positive AMI pulse and RNEG having a negative pulse in place of every negative AMI pulse. 0 = NRZ format. Transmit data pins TPOS and TNEG are interpreted as TNRZ and NC (not connected). Receive data pins RPOS and RNEG are interpreted as RNRZ and RLCV. In this mode, all line code violations are reported as active high on RLCV.
—	61	61	TAIS1	Transmit Ch1 AIS mode enable	I	Transmission of Alarm Indication Signal (AIS) for a given channel. Replace transmit data with AIS signal. The AMI form of AIS supported is alternating 1s. (+1, -1, +1, -1, +1, ...) Looping takes precedence over AIS. 1 = AIS mode enabled 0 = AIS mode disabled
51	—	51	TAIS/ TAIS2	Transmit Ch2 AIS mode enable	I	
40	40	40	TAIS2/ TAIS3	Transmit Ch3 AIS mode enable	I	
43	43	43	E3MODE	E3MODE	I	When the pin is set to high, it enables the E3 mode on all channels, instead of the DS3/STS-1 mode. This also changes the pulse shaper to E3 mode and overrides all LBO pins. It also changes the encoder/decoder from B3ZS mode to HDB3 mode. 1 = E3 mode 0 = DS3/STS-1 mode
44	72	72	LBO/ LBO1	Transmit line Ch1 build-out mode	I	Line build-out mode per channel, based on the length of cable on the transmit side of the cross-connect block. This bit is overridden and the pulse shaper is disabled (no pulse shaping) if E3MODE = 1. 1 = Inserts line build-out into the transmit channel. Usually used when the transmit cable is less than 350 feet in length. 0 = Line build-out bypassed (not inserted). Usually used when the transmit cable is greater than 350 feet in length.
—	29	44	LBO2	Transmit line Ch2 build-out mode	I	
—	—	29	LBO3	Transmit line Ch3 build-out mode	I	

Table 1-1. CN8331/CN8332/CN8333 Pin Definitions *(4 of 6)*

Pin #			Signal Name	Description	I/O/P	Notes
CN8331	CN8332	CN8333				
56	74	74	LLOOP/ LLOOP1	Local loopback enable Ch1	I	Local loopback enable per channel. The transmit data is looped back immediately from the encoder to the decoder in place of the received data. 1 = local loopback enabled 0 = local loopback disabled
—	27	56	LLOOP2	Local loopback enable Ch2	I	
—	—	27	LLOOP3	Local loopback enable Ch3	I	
57	75	75	RLOOP/ RLOOP1	Remote loopback enable Ch1	I	Remote loopback enable per channel. The receive data, retimed after clock recovery, is looped back into the AMI generator in place of the transmit data. 1 = remote loopback enabled 0 = remote loopback disabled
—	26	57	RLOOP2	Remote loopback enable Ch2	I	
—	—	26	RLOOP3	Remote loopback enable Ch3	I	
45	71	71	XOE/ XOE1	Transmit output enable Ch1	I	Transmit output enable per channel. 1 = transmit line output driver enabled 0 = transmit output driver set to high impedance state
—	30	45	XOE2	Transmit output enable Ch2	I	
—	—	30	XOE3	Transmit output enable Ch3	I	
—	70	70	REQH1	Ch1 Receive High EQ Gain Enable	I	The equalizer in the CN833x has two gain settings. The higher gain setting is designed to optimally equalize a nominally-shaped (meets the pulse template), pulse-driven DS3 or STS-1 waveform that is driven through 0–900 feet of cable. Square-shaped pulses such as E3 or DS3-HIGH require less high-frequency gain and should use the low EQ gain setting. REQH = 1 high EQ gain (DS3/STS-1 modes) REQH = 0 low EQ gain (E3/DS3 Square Modes)
46	—	46	REQH/ REQH2	Ch2 Receive High EQ Gain Enable	I	
—	31	31	REQH3	Ch3 Receive High EQ Gain Enable	I	
Power/Ground						
12	4	4	TVDD/ TVDD1	TX power Ch1	P	Power pins for transmit circuitry per channel (3.3 V).
—	20	12	TVDD2	TX power Ch2	P	
—	—	20	TVDD3	TX power Ch3	P	
9	1	1	TVSS/ TVSS1	TX ground Ch1	P	Ground pins for transmit circuitry per channel.
—	17	9	TVSS2	TX ground Ch2	P	
—	—	17	TVSS3	TX ground Ch3	P	
13	5	5	RVDD/ RVDD1	RX power Ch1	P	Power pins for receive circuitry per channel (3.3 V).
—	13	13	RVDD2	RX power Ch2	P	
—	—	21	RVDD3	RX power Ch3	P	Connect to 3.3 V power.

Table 1-1. CN8331/CN8332/CN8333 Pin Definitions *(5 of 6)*

Pin #			Signal Name	Description	I/O/P	Notes
CN8331	CN8332	CN8333				
16	8	8	RVSS RVSS1	RX ground Ch1	P	Ground pins for receive circuitry per channel.
—	24	16	RVSS2	RX ground Ch2	P	
—	—	24	RVSS3	RX ground Ch3	P	Connect to ground.
60	60	60	DVDDC	Digital core power	P	Digital core power for all channels (3.3 V).
41	41	41	DVSSC	Digital core ground	P	Digital core ground for all channels.
79	79	79	VGG	5 V/3.3 V ESD pin (1)	P	5 V supply for 5 V-tolerant, digital pad ESD diodes. No static power is drawn from pin.
73	73	73	DVDDIO	Digital I/O power	P	Connect to 3.3 V digital power.
28	28	28	DVSSIO	Digital ground	P	Digital ground.
4, 5, 20, 21	12, 13	—	VDD	Power	P	Connect to 3.3 V power.
1, 8, 17, 24	9, 16	—	VSS	Ground	P	Connect to ground.
Miscellaneous						
58	76	76	$\overline{PD}$/ $\overline{PD1}$	Power down for Ch1	I	Power down transceiver channel 0 = Power down channel (off) 1 = Channel active (on) Note: A special power-down mode exists when all three PDBs are set low. This special mode shuts off the entire chip (including biasing). This is useful for static Idd testing. (See PD pin).
—	25	58	$\overline{PD2}$	Power down for Ch2	I	
—	—	25	$\overline{PD3}$	Power down for Ch3	I	
47	65	65	REFCLK/ REFCLK1	Reference clock for Ch1	I	Reference clock from off-chip. This clock should be set to one of the following: • E3 rate (34.368 MHz) • DS3 rate (44.736 MHz) • STS-1 rate (51.84 MHz) The clock rate should correspond to the mode of operation that has been chosen for the channel.
—	36	47	REFCLK2	Reference clock for Ch2	I	
—	—	36	REFCLK3	Reference clock for Ch3	I	
80	80	80	RBIAS	Bias resistor	O	A 12.1 kΩ ±1% resistor tied from this pin to ground provides the current reference to the entire chip.(2)
78	78	78	Reset	Reset	I/O	Asynchronous reset (reset entire device).
77	77	77	GPD	Global Power Down	I/O	Power Down (device enter low power state for Static Idd testing).

Table 1-1. CN8331/CN8332/CN8333 Pin Definitions *(6 of 6)*

Pin #			Signal Name	Description	I/O/P	Notes
CN8331	CN8332	CN8333				
2, 3, 6, 7, 18, 19, 22, 23, 25, 26, 27, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 42, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 74, 75, 76	10, 11, 14, 15, 42, 44, 45, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58	—	NC	No connect	—	Not connected.

NOTE(S):
(1) This pin should be connected to 3.3 V in an all-3.3 V design.
(2) Placing a capacitor from this pin to ground may result in instabilities.
3. All digital input pins contain a 75 KΩ pull-down resistor from input to DVSS.

2.0 Functional Description

2.1 Overview

CN8333 is a triple E3/DS3/STS-1 Line Interface Unit (LIU). It is the physical layer interface between the data framer (or other terminal-side equipment) and the electrical cable used for data transmission.

The CN8333 LIU consists of three independent data transceivers that can operate over type 734/728 coaxial cable at the rates of 34.368 Mbps (E3), 44.736 Mbps (DS3), and 51.84 Mbps (STS-1). The transmit side takes an NRZ or already-encoded dual rail input and encodes it into AMI B3ZS (for DS3/STS-1) or HDB3 (for E3) analog waveforms to be transmitted over the coaxial cable. The receiver side takes in the attenuated and distorted analog receive signal and equalizes, slices, and resynchronizes the signal before decoding it to the NRZ output or sending out a non-decoded dual rail.

CN8331 and CN8332 are single- and dual-E3/DS3/STS-1 LIUs, respectively. In all respects, their performance and features are identical to the CN8333.

The architecture of the CN833x includes the following internal functions for each channel:

General:

- bias generator
- power-on reset
- loopback MUXes

Transmitter:

- B3ZS/HDB3 encoder
- Alarm Indication Signal (AIS) insertion
- pulse shaper
- line driver

Receiver:

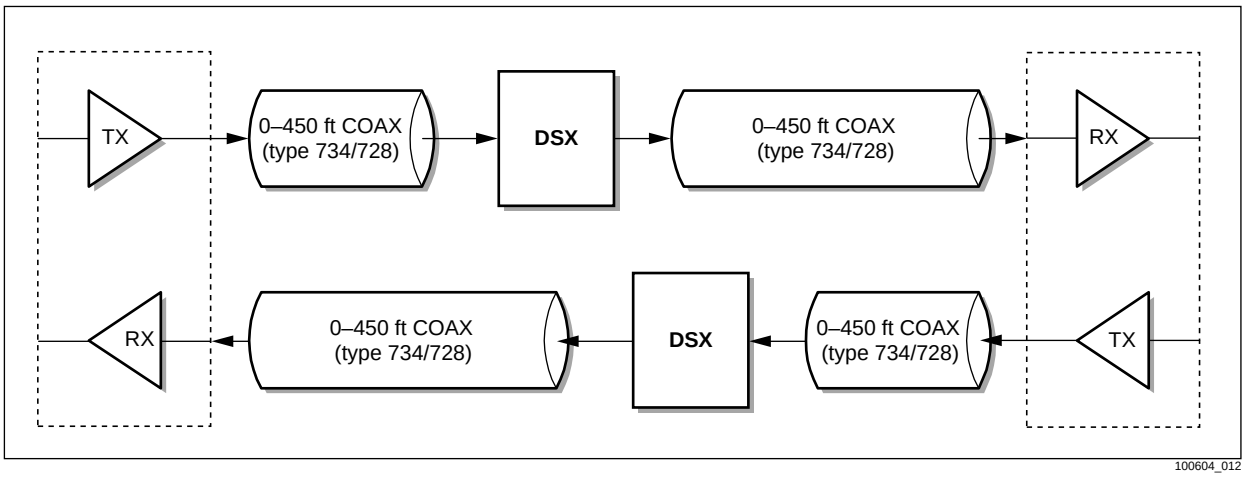
- Automatic Gain Control
- receive equalizer
- Clock Recovery Circuit
- Loss Of Signal (LOS) detector
- B3ZS/HDB3 decoder with bipolar violation detector

In addition, each channel has the ability to perform remote and local loopbacks. Figure 2-1 illustrates a typical application using the CN833x in a channel.

External pins are provided to configure the various line rates and formats for each channel.

The CN833x is used as a data transceiver over a coaxial cable that is up to 900 feet long (or up to 450 feet from the DSX) in an on-premise environment within any public or private networks which use these data rates.

Figure 2-1. Typical Application Of Single CN833x Channel



2.2 Transmitter

This section describes the detailed operation of the various blocks in the CN833x transmitter.

2.2.1 AMI B3ZS/HDB3 Encoder

ENDECDIS and the E3MODE pins configure the encoder mode.

When ENDECDIS = 0, the encoder is receiving non-encoded Nonreturn to Zero (NRZ) data on the TNRZ (TPOS) pin alone, and the NC (no connect) (TNEG) pin is ignored.

Data is encoded into a representation of a three-level B3ZS (E3MODE = 0) or HDB3 (E3MODE = 1) signal (conforming to the coding rules as specified in Appendix A) before going on to the pulse shaper in the form of two binary signals representing the positive and negative three-level pulses.

When ENDECDIS = 1, the encoder is disabled. The encoder passes already-encoded data over TPOS (TNRZ) and TNEG (NC) to the pulse shaper.

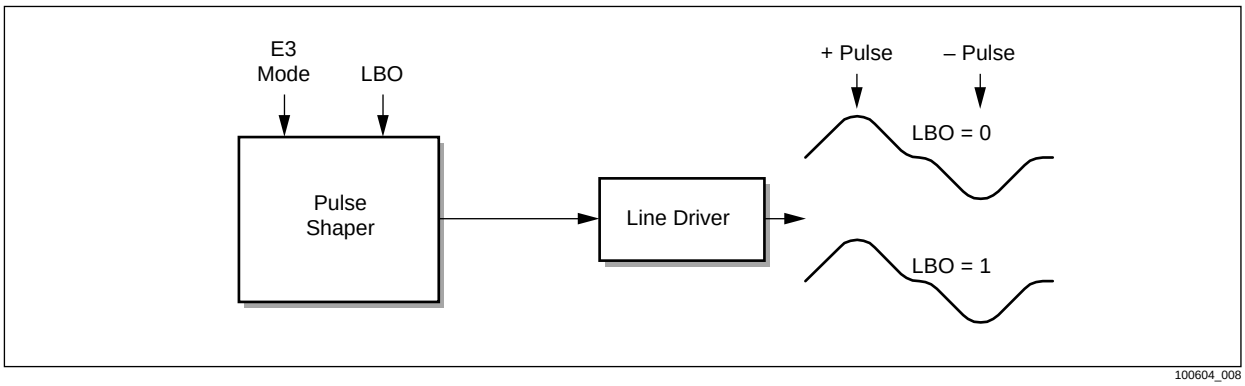
The transmit digital data is clocked into the chip via a rising TCLK edge, which must be equal to the symbol rate (line rate). A small delay added to the data provides a certain amount of negative data hold time.

2.2.2 Pulse Shaper

The pulse shaper converts the two digital (clocked) positive and negative pulses into a single analog three-level Alternate Mark Inversion (AMI) pulse. The pulses are in Return to Zero (RZ) format, meaning that all positive and negative pulses have a duration of the first half of the symbol period.

For the E3 rate (E3MODE = 1), the AMI pulse is a full-amplitude, square-shaped pulse with very little slope.

Figure 2-2. Pulse Shaper



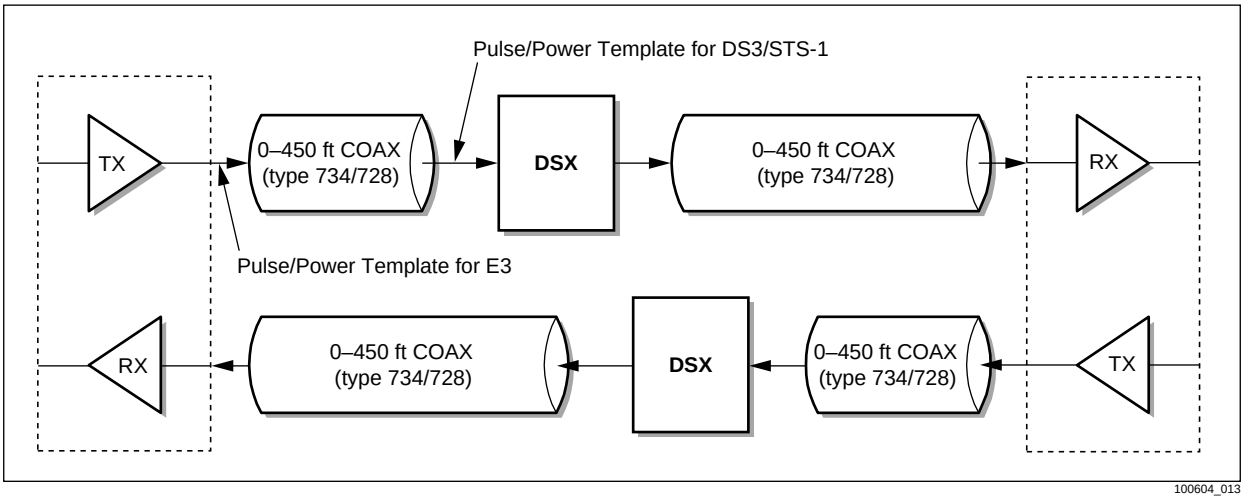
For DS3/STS-1 rates, a pulse-shaper block is used to shape the transmit waveform and reduce its high-frequency energy content. This ensures that the transmit pulse template is met at the cross-connect block, which follows 0–450 feet of transmit-side coaxial cable.

2.2.3 Line Driver

The differential line driver takes the filtered transmit waveform, increases it to the proper level, and drives it into the transmit magnetics. The two external discrete back-matching resistors (36 Ωs) aid in line matching. The driver is presented with an approximately 150 Ω differential load. Driver gain accounts for the 6 dB gain loss in the back-matching resistors.

Figure 2-3 illustrates the Pulse/Power template measurement points for the various data rates.

Figure 2-3. Pulse Measurement Points



2.2.4 Transmit Pulse Mask Templates and Power Measurements

Figure 2-4. Transmit Pulse Mask for E3 Rate

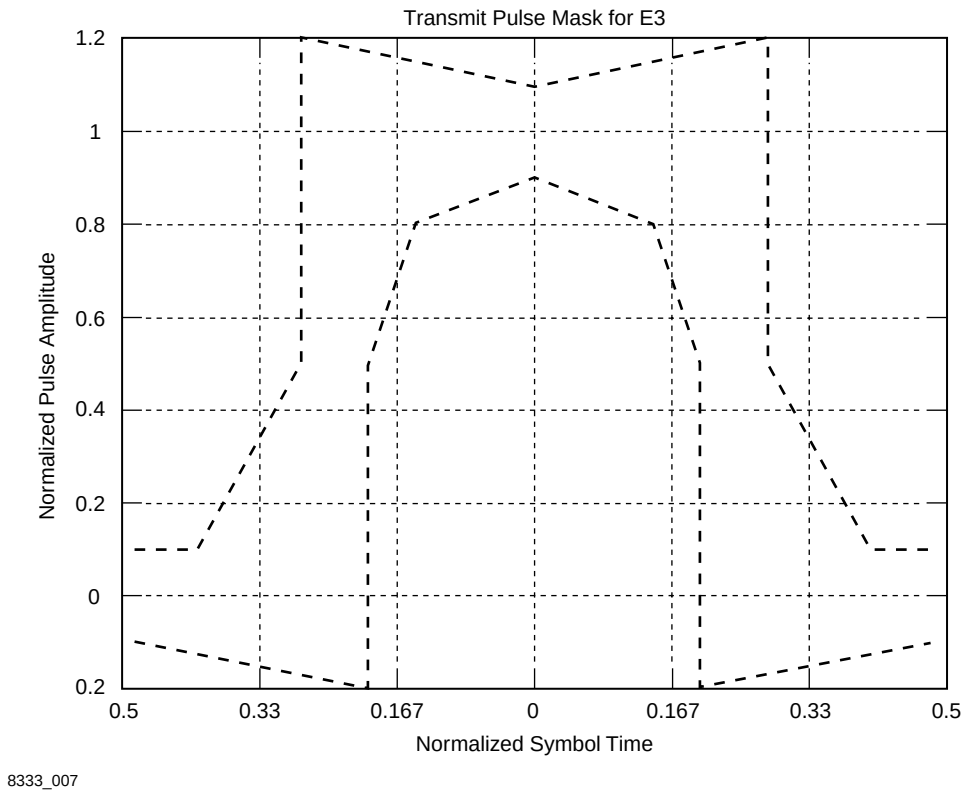
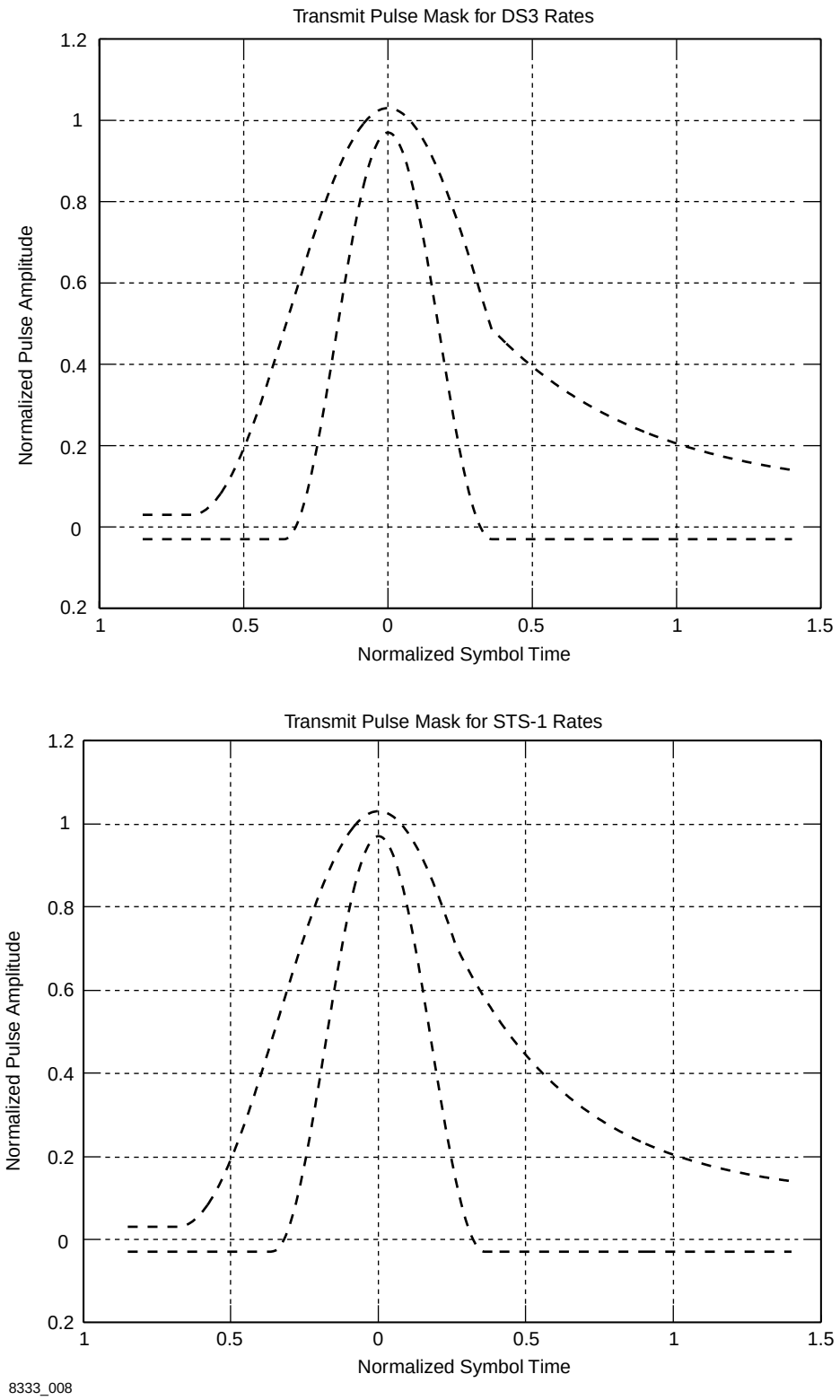


Figure 2-5. Transmit Pulse Mask for DS3 and STS-1 Rates



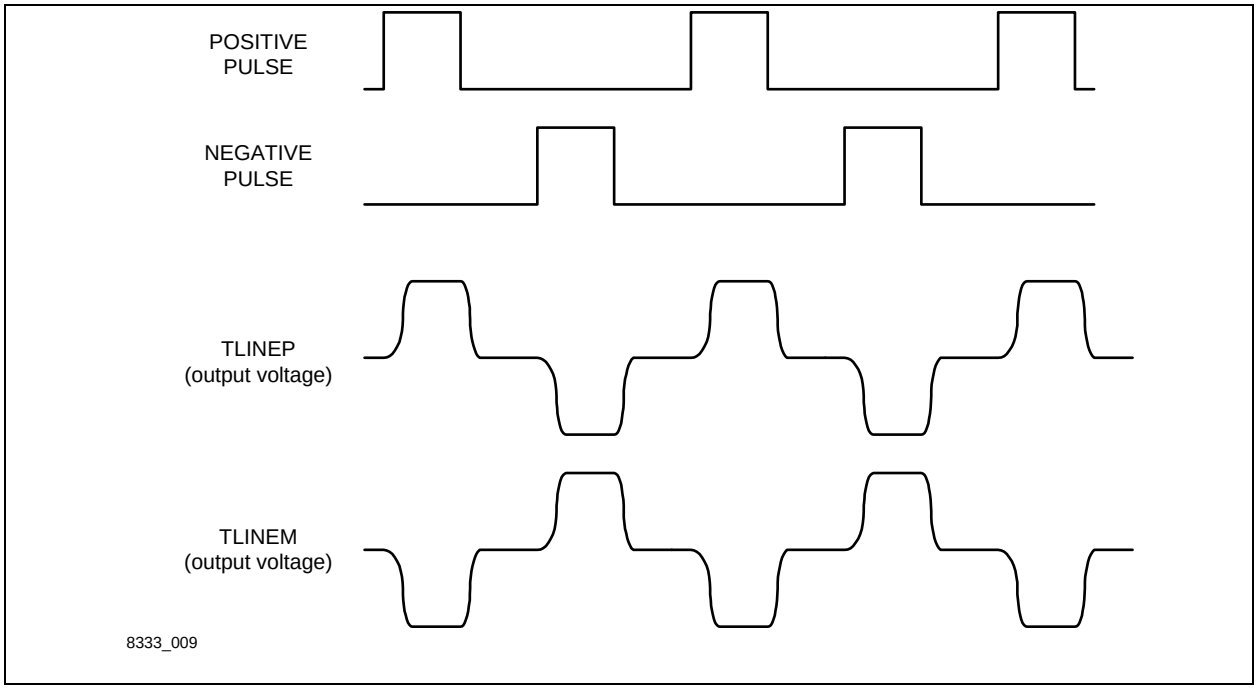
2.2.5 Alarm Indication Signal (AIS) Generator

When selected by asserting TAIS, an AIS replaces the transmit data at TPOS and TNEG. The E3 type of AIS signal (all 1s) is supported. In three-level signal form, this is a continuously alternating positive and negative pulse stream, as if the transmit data were a continuous string of logical 1s. Figure 2-6 illustrates the AIS signal.

The TAIS pin has the same data latency as the TX data pins and can be used to replace single symbols within a data stream. When the encoder is disabled (ENDECDIS = 1), the TAIS mode maintains the proper phase, based upon the polarity of the last 1 received.

The AIS signal follows the same path as the TX data during remote or local loopback.

Figure 2-6. AIS Signal



2.2.6 Jitter Generation (Intrinsic)

The CN833x device meets the jitter generation requirements for various rates with large margins, with the condition that the input transmit clock (TCLK) is jitter-free. Data rates and jitter generation requirements are defined in the following documents:

- E3 rate—*ETSI TBR24, ITU-T 9.823*
- DS3 rate—*Bellcore Telecardia GR499, AT&T Accunet TR54014, ITU-T 9.824*
- STS-1 rate—*Bellcore Telecardia GR253*

2.3 Receiver

This section describes in detail various blocks in the CN8331/CN8332/CN8333 receiver.

2.3.1 Receive Sensitivity

The receiver recovers data from the coaxial cable that is attenuated due to the frequency-dependent characteristics of the cable. In addition, the receiver compensates for the flat loss (across all frequencies) in the various electrical components and the variation in transmitted signal power.

The CN833x device is able to recover data that has been attenuated by a maximum of 900 feet of coax having characteristics and attenuation consistent with *ANSI T1.102-1993*, Annex C, Figure C.2. This approximates the characteristics of AT&T type 734/728 cable; almost the same attenuation characteristic is achieved by one-half the length of AT&T type 735 cable.

2.3.2 AGC/VGA Block

The Variable Gain Amplifier (VGA) receives the AMI input signal from the coaxial cable. The VGA supplies flat gain (independent of frequency) to make up for various flat losses in the transmission channel and for loss at one-half the symbol rate that cannot be made up by the equalizer. The VGA gain is controlled by a feedback loop which senses the amplitude of the equalizer output, acting to servo this amplitude for optimal slicing.

2.3.3 Receive Equalizer

The receive equalizer receives the differential signal from a VGA and acts to boost the high frequency content of the signal to reduce inter-symbol interference (ISI) to the point that correct decisions can be made by the slicer with a minimum of jitter in the recovered data.

The REQH pin is provided to allow lower amounts of equalization (shorter equivalent cable lengths) for cases where a square-shaped pulse (that does not meet the DS3/STS-1 standards) is transmitted to the receiver. A square-shaped input has a much larger high-frequency content and could have overshoots at the EQ output high enough to cause bit errors. Setting REQH = 0 will lower the gain and reduce the amount of overshoot.

2.3.4 The PLL Clock Recovery Circuit

The clock recovery circuit (RX PLL) extracts the embedded clock from the sliced data and provides this clock and the retimed data to the decoder (data mode). Upon startup (after the internal reset is deasserted), the RX PLL uses a reference clock (REFCLK, running at the symbol rate) and a phase-frequency detector to lock to the correct data rate (reference mode). During reference mode, the data outputs are squelched (set to 0). The RX PLL is kept in reference mode until a valid input is detected.

2.3.5 Loss Of Signal (LOS) Detector

The Receive Loss Of Signal (RLOS) is a digital function which monitors the retimed data from the clock recovery block. The AMI data is checked for a continuous run of zeroes. When a continuous run of 128 ± 1 consecutive zeroes occurs, the RLOS signal is asserted. After the RLOS signal is asserted, a 1s count is made on every block of 128 AMI symbols. The RLOS signal is deasserted when the 1s count within a block of 128 symbols is at least:

B3ZS: Minimum 1s density = 39 ± 1 count out of 128 (~30.5%)

HDB3: Minimum 1s density = 29 ± 1 count out of 128 (~22.7%)

The RLOS detector will always monitor the cable-side RX inputs. The detector is not affected by the state of remote or local looping.

2.3.6 Jitter Tolerance

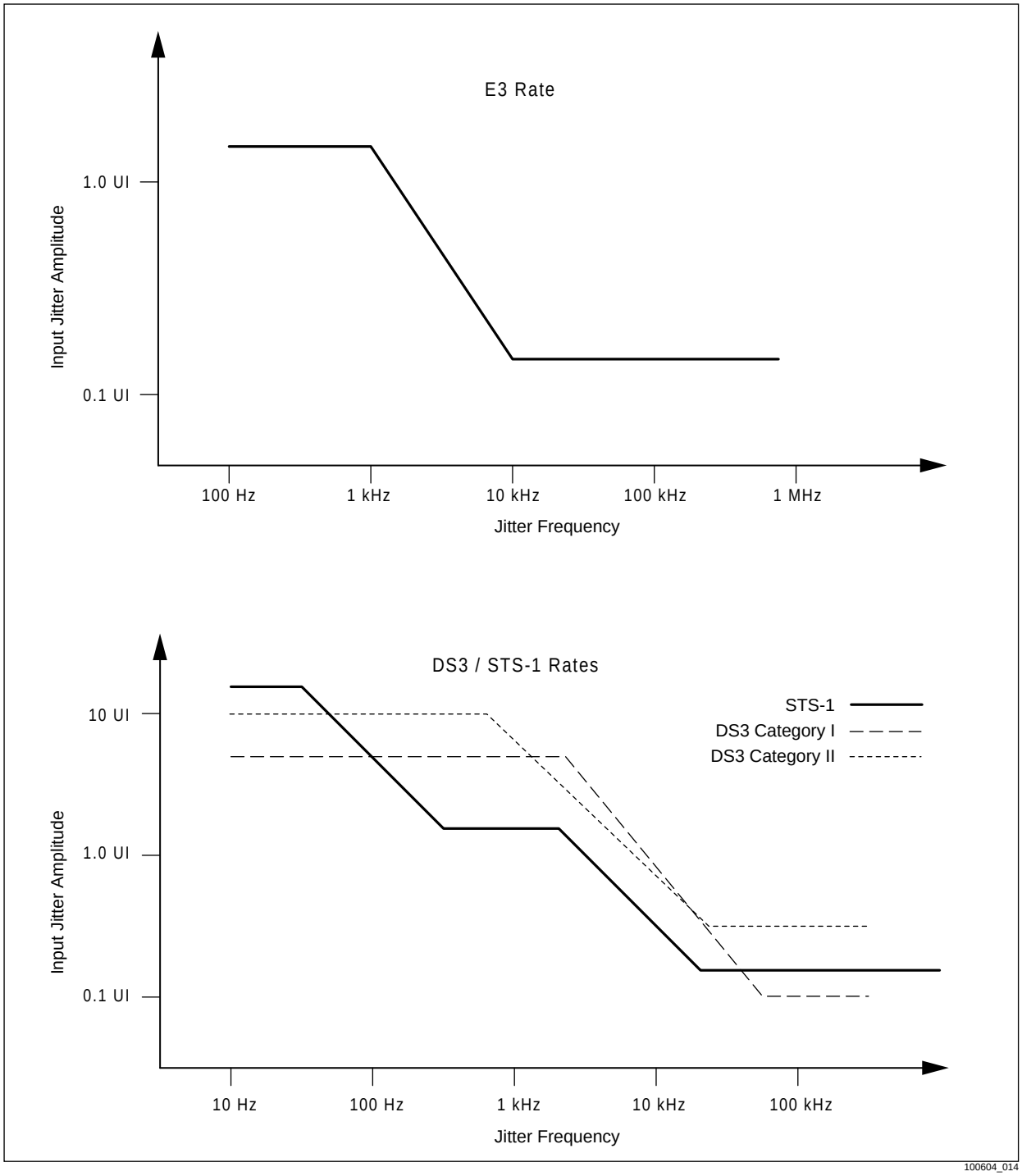
The CN833x receiver is able to tolerate a specified amount of high-frequency jitter in the received signal while providing error-free operation (generally defined as a bit error rate of less than 10^{-9}). The specifications (illustrated in Figure 2-7) for jitter tolerance are discussed in the following documents:

- E3 rate – *ITU-T G.823 and ETSI TBR24* contain frequency masks for input jitter tolerance.

NOTE: To meet jitter transfer requirements for loop-timed operation, an external jitter attenuator is required. The jitter attenuator lessens jitter from the receive clock.

- DS3 rate – *ITU-T G.823* and *Bellcore GR499* specify jitter tolerance frequency masks for Category I and Category II interfaces.
- STS-1 rate – *Bellcore GR253* specifies a jitter tolerance. It is noted that the STS-1 jitter tolerance differs from DS3 requirements only for Category II interfaces.

Figure 2-7. Minimum Input Jitter Tolerance Requirement



2.3.7 B3ZS/HDB3 Decoder With Bipolar Violation Detector

In the CN833x device, when ENDECDIS = 0 (encoder/decoder enabled), the decoder takes the output from the clock recovery circuit and decodes the data (HDB3 or B3ZS) into a single retimed NRZ data signal. The data signal is then sent out of the CN833x over the RNRZ (RPOS) pin. Any detected Line Code Violations (LCV) are sent out over the corresponding RLCV (RNEG) pin. The RLCV pin is asserted for one symbol period at the time the violation appears on the RX output pin (RNRZ).

The following shows data sequence criteria for LCV; violations are indicated in bold text. A valid bipolar pulse is indicated by a B. A bipolar violation (non-alternating positive or negative) pulse is indicated by a V.

- Excessive zeros: 0, 0, 0, **0** (HDB3) or 0, 0, **0** (B3ZS). These violations are passed on as 0 data on the RNRZ pin.
- Bipolar violation: B, 0, **V** (i.e., +1, 0, **+1** or -1, 0, **-1** for HDB3) B, **V** (B3ZS and HDB3). These violations are passed on as 1 data on the RNRZ pin.
- Coding violation: 0, 0, **V** (HDB3) or 0, **V** (B3ZS) with an even number of Bs since the last valid 0 substitution V (follows coding rule). These violations are passed on as 0 data on the RNRZ pin.

The even/odd counter (used to count the number of Bs between Vs) will count a bipolar violation as a B. A coding violation or a valid 0 substitution resets the counter.

When ENDECDIS = 1, the decoder is disabled, and the retimed slicer outputs are sent out over RPOS (RNRZ) and RNEG (RLCV) pins. These outputs are then decoded by the CN8340/CN8330 or other downstream device. Line code violations are not detected in this mode of operation. The decoder is configurable for either:

- E3 mode using HDB3 coding (E3MODE = 1)
- DS3/STS-1 mode using B3ZS coding (E3MODE = 0)

The receiver digital data outputs are centered on the rising edge of RCLK (see Section 2.8).

2.3.8 Data Squelching

A counter in the receiver keeps track of the number of consecutive symbol periods without a valid data pulse. When 128 or more 0s in a row are counted, the receiver assumes that it has lost the signal and resets itself to try and regain the signal. While the receiver is reacquiring the signal, the clock recovery block locks to the reference clock and the data squelching is achieved by forcing the data bits to zero. The data squelching is true in both NRZ and dual rail mode. When the input signal has been properly amplified and equalized, the clock recovery PLL will then switch to the incoming data.

2.4 Additional CN8331/CN8332/CN8333 Functions

2.4.1 Bias Generator

To achieve good isolation between the channels, each channel utilizes an independent power and ground to both transmit and receive. Additionally, each channel has its own band gap voltage reference. Because only one external resistor for current generation exists, only one band gap voltage can be used. The band gap from Ch1 has been chosen for this task.

The 12.1 kΩ external resistor from pin RBIAS to ground, is specified to have a tolerance of ±1%. This helps to keep tighter control on power dissipation and circuit performance.

NOTE: Capacitance should be kept to a minimum on the RBIAS pin.

2.4.2 Power-On Reset (POR)

A POR function is provided in the CN833x device to ensure all of the resettable digital logic and analog control lines are starting from a known state. This circuit uses a fixed RC timer (~1µs); additionally, 128 clocks from REFCLK are counted (after the RC timer has timed-out) before reset is deasserted, which begins timing after a minimum supply voltage is reached (see Table 2-2).

2.4.3 Loopback Multiplexers (MUXes)

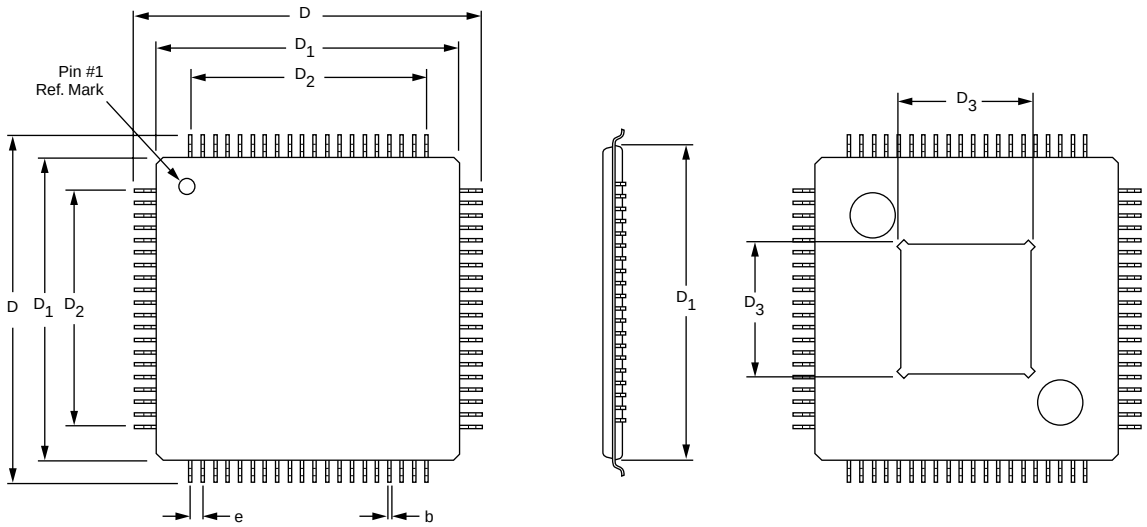
Two loopback MUXes per channel in the CN833x allow for local loopback (terminal or framer side), remote loopback (cable side), or both (the AIS signal follows the same path as the transmit data during loopback). The RLOS signal monitors the RX cable inputs irrespective of any loopback.

In remote loopback, set by asserting pin RLOOP high, the receive data (retimed after clock recovery but not decoded) loops back into the pulse shaper in place of the transmit data. Additionally, this data sent out the RPOS, RNEG, and RCLK pins.

In local loopback, set by asserting pin LLOOP, the transmit data loops back immediately from the encoder output to the decoder input in place of the received data. Additionally, this data is sent out the TLINEP and TLINEM pins.

2.5 Mechanical Specifications

Figure 2-8. Mechanical Drawing—Dimensions



	Millimeters		Inches	
Dim.	Min.	Max.	Min.	Max.
A	1.20 MAX.		0.047 MAX.	
A_1	0.05	0.15	0.002	0.006
A_2	0.95	1.05	0.040	0.041
D	15.75	16.25	0.620	0.640
D_1	13.90	14.10	0.547	0.555
D_2	12.35 REF.		0.486 REF.	
D_3	6.50 REF.		0.256 REF.	
L	0.45	0.75	0.018	0.030
L_1	1.00 REF.		0.039 REF.	
b	0.32 REF.		0.026 REF.	
c	0.09	0.20	0.013 REF.	
e	0.65 REF.		0.004	0.008
Coplanarity	0.10 MAX.		0.004 MAX.	
Ref. 80-Pin ETQFP (GP00-D537)				

100604_015

2.6 Electrical Characteristics

2.6.1 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
DVDDC RVDD TVDD VDD	Power Supply Voltage	–0.3	6	V
V_I	Voltage on Any Signal Pin	–1.0	VGG + 0.3 V	V
T_{ST}	Storage Temperature	–40	125	°C
T_{VSOL}	Vapor Phase Soldering Temperature (1 min.)	—	220	°C
θ_{JA}	Thermal Resistance (Still air, socketed)	—	40	$^{\circ}C/_{W}$
θ_{JA}	Thermal Resistance (Still air, soldered)	—	24	$^{\circ}C/_{W}$
θ_{Jc}	—	—	7.40	$^{\circ}C/_{W}$
FIT	Failures in time @ 89,000 device hours, temperature of 55 °C, 0 failures.	—	313	fits

NOTE(S):

1. Stresses above those listed as absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.6.2 Recommended Operating Conditions

Table 2-2 specifies various operating conditions, power supplies, and the bias resistor.

Table 2-2. Recommended Operating Conditions

Parameter	Conditions	Min	Nom	Max	Unit
Power supply voltage	DVDDC, RVDD, TVDD, VDD	3.135	3.3	3.465	V
ESD voltage(1)	VGG	3.135	5	5.5	V
Power dissipation (CN8333)	Total chip	—	0.83	1.0	W
Power dissipation (CN8332)	Total chip	—	—	0.8	W
Power dissipation (CN8331)	Total chip	—	—	.450	W
External bias resistor	Pin RBIAS to GND; ±1%	11.98	12.1	12.22	kΩ

NOTE(S):
(1) With 5 V logic input, VGG should be tied to 5 V. With 3.3 V logic input, VGG should be tied to 3.3 V.

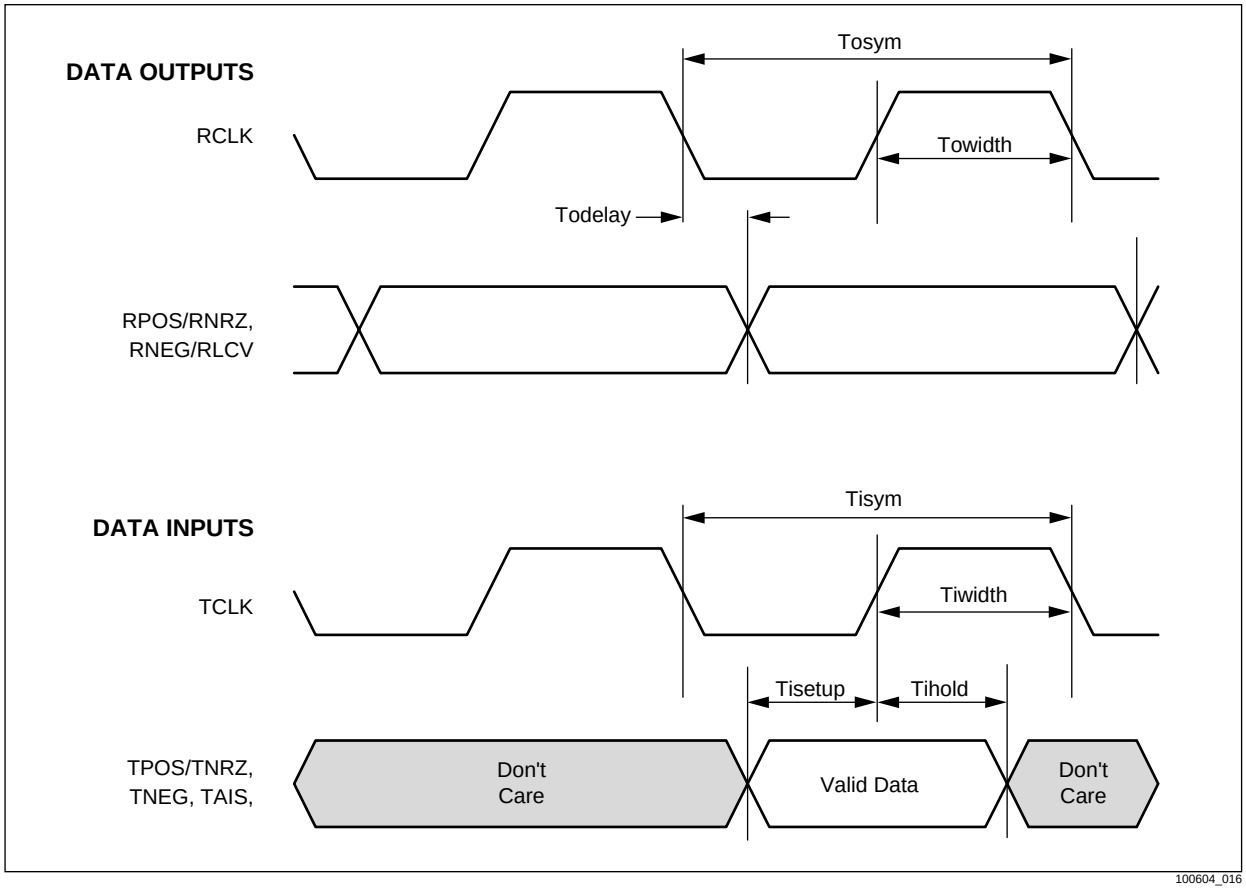
2.8 AC Characteristics

Table 2-4. AC Characteristics (Logic Timing)

Parameter	Conditions	Min	Nom	Max	Unit
Tosym, Tisym RCLK and TCLK	E3 DS-3 STS-1	—	29.10 22.35 19.29	—	ns ns ns
Clock Duty Cycle	Towidth/Tosym, RCLK Tiwidth/Tisym, TCLK Tiwidth/Tisym, REFCLK	45 40 40	—	55 60 60	% % %
Todelay				5	ns
Tisetup	TPOS/TNRZ, TNEG, TAIS	4	—	—	ns
Tihold	TPOS/TNRZ, TNEG, TAIS	0	—	—	ns

NOTE(S):
1. The description applies to the DS3, E3, and STS-1 clock rates and other parameters such as pulse width, set-up time, hold time, and duty cycle.
2. The timing diagram, illustrated in Figure 2-9, describes the logical relationship between various clock and data signals, and parameter values.

Figure 2-9. Timing Diagram



3.0 Applications

The CN8331/CN8332/CN8333 can be used in a variety of applications.

Figure 3-1 illustrates an example of three DS3 lines being terminated by the CN8333. The data and clock are extracted and passed on to the framer chip for further data manipulation and user interface.

It is important to employ high-frequency design techniques for the printed board layout.

3.1 PCB Design Considerations for CN8331/CN8332/CN8333

The CN8333 device is a triple LIU operating at frequencies up to 52 MHz. The high-speed nature of the device calls for a careful design of the PCB using this part. Some design considerations are outlined below.

3.1.1 Power Supply and Ground Plane

A unified power plane with properly placed capacitors of the correct size will mitigate most power rail-related voltage transients. A properly placed bulk capacitor, where the power enters the board, with noise-bypassing capacitors at the power pins on the integrated circuits should be adequate. The noise-bypassing capacitors must be able to supply all the switching current.

Ferrite beads are used with power rails to filter the high-frequency noise. For every design, noise frequencies and levels are different. Therefore, whether beads are necessary, and the effective frequency where they should operate, is difficult to determine. It is a good idea to provision for ferrite beads on the boards.

The board trace from the CN8333 power supply pin to the noise-bypassing capacitor should be minimized. Additionally, ground connections from the ground plane to the CN8333 ground pins and the noise-bypassing capacitor ground pins should be minimized.

A unified ground plane is the best way to minimize ground impedance. Most of the ground noise is produced by the return currents and power supply transients during switching. This effect is minimized by reducing the ground plane impedance.

3.1.2 Impedance Matching

It is critical that traces around the transformers and matching resistors be kept to a minimum length and, in the following cases, the trace impedance be matched to 75 Ω:

- The impedance from the BNC connector to the transformer
- The impedance from the transformer to the matching resistors

3.1.3 Other Passive Parts

The reference design uses the Pulse T3001 extended temperature range 1:1 transformer for the coupling of the BNC connector to the device.

The ferrite beads used to decouple the receive- and transmit-VDD pins and the ferrite beads on all analog input VDD pins are type 2508056017Y0 from Fair-Rite. The bulk capacitor used for where the power enters the board can be a electrolytic or tantulum type capacitor, the recommended value and type is a 220µf tantulum capacitor.

3.1.4 IBIS Models

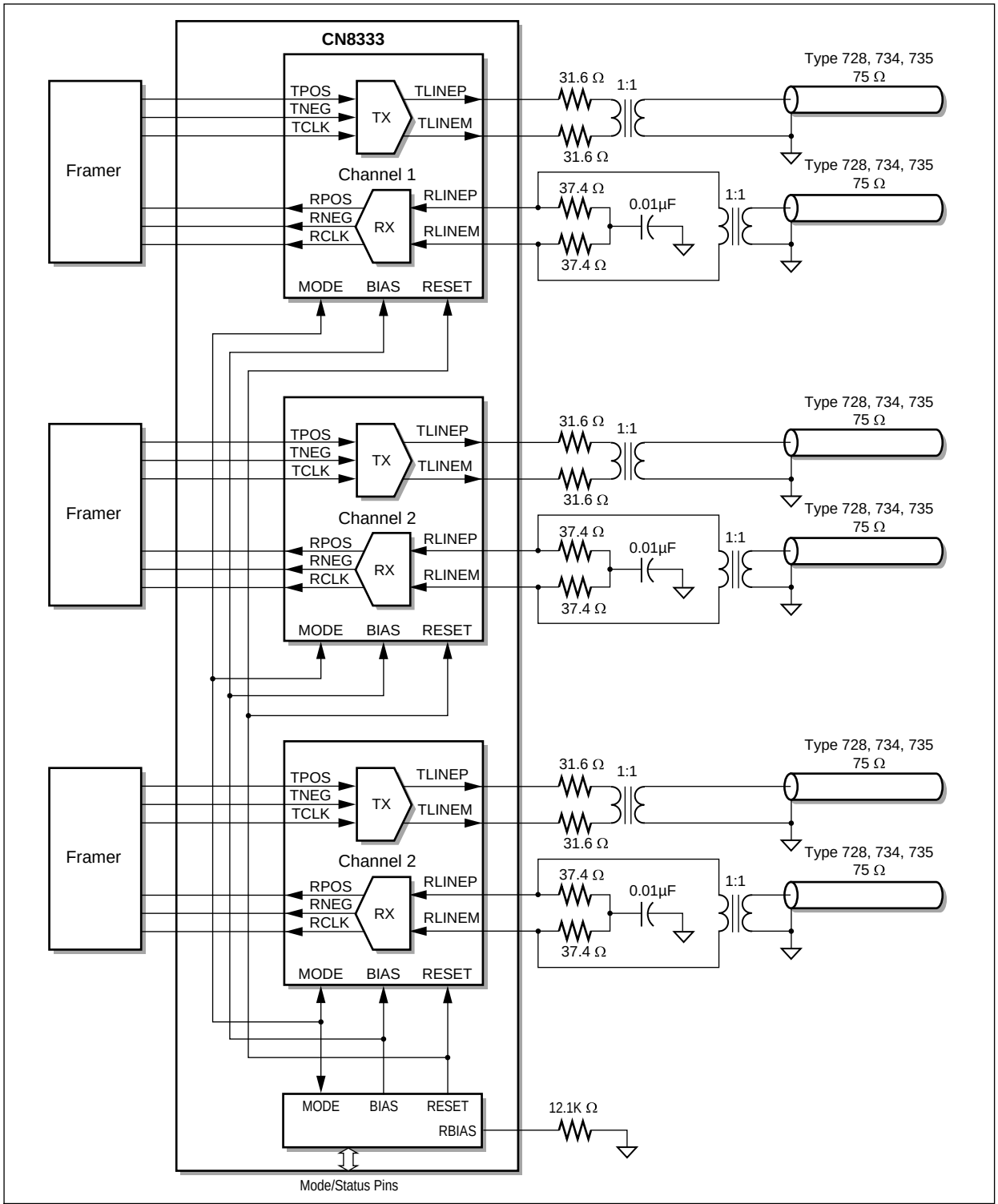
IBIS (Input/Output Buffer Interface Specification) models for the CN8331/CN8332/CN8333 are available from Conexant.

3.1.5 Recommended Vendors

Part #
T3001, Data Sheet - T619

America	Pulse		**Fair-Rite Products Corp.**
Address:	Corporate Office 12220 World Trade Drive San Diego, CA 92128		P.O. Box J One Commercial Row Wallkill, NY 12589
Telo:	858-674-8100	Telo:	914-895-2055
Fax:	858-674-8262		
Northern Asia	Pulse 3F-4, No. 81, Sec. 1 Hsin Tai Wu Road Hsi-Chih Tapei Hsien, Taiwan R.O.C.		
Telo:	886-2-26980228 886-2-26980948		
Northern Europe	Pulse 1S2 Huxley Road The Surrey Research Park Guildford, Surrey GU2 5RE United Kingdom		
Telo:	44-1483-401700		
Fax:	44-1483-401701		

Figure 3-1. Typical Connection of CN8333



NOTE(S): All transformers are part number T3001 from Pulse Technology. (See Recommended Vendors, page 3.2.)

100604_004

Appendix A

A.1 Applicable Standards

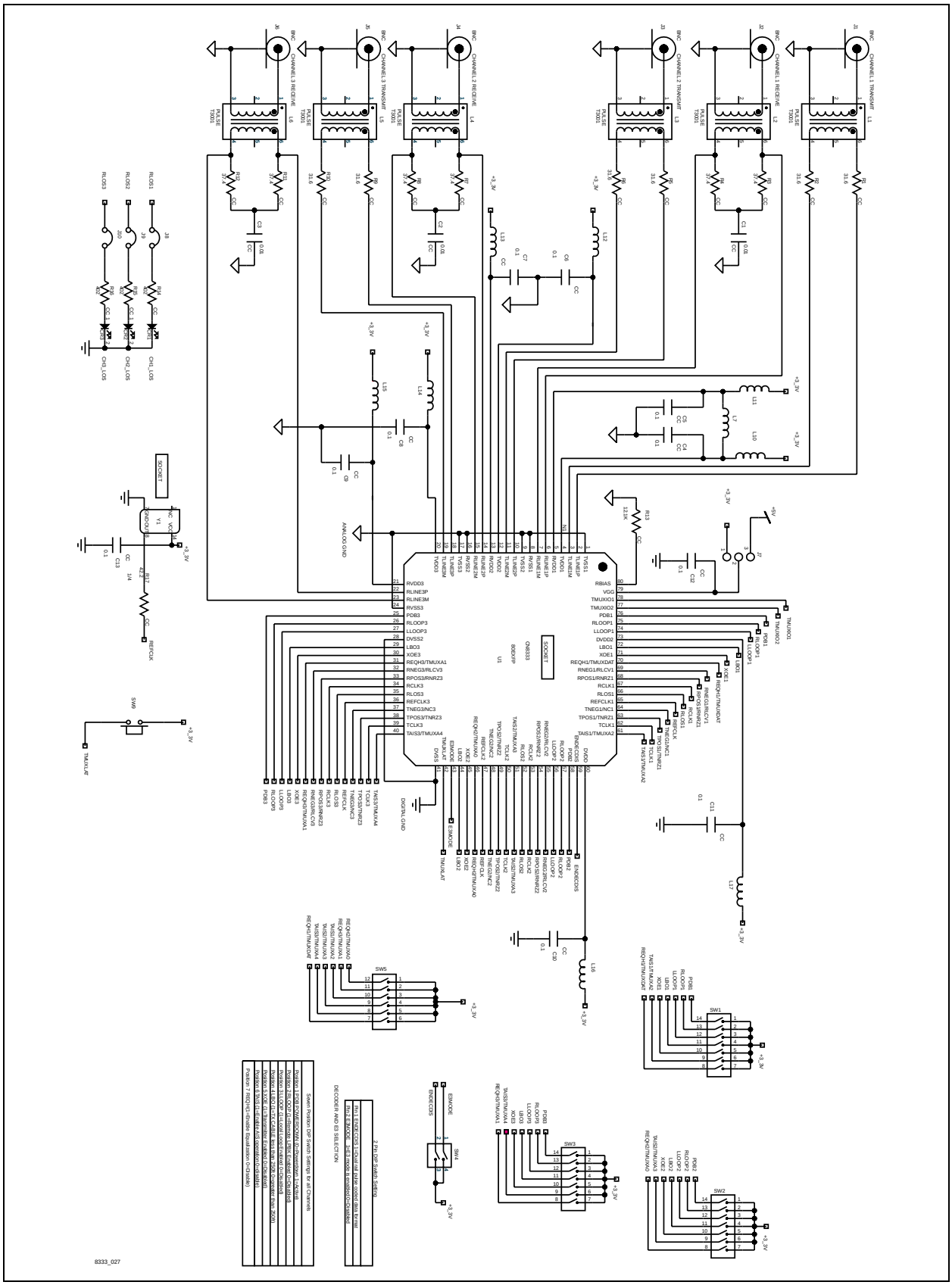
The applicable standards documents are as follows:

- *ANSI T1.102-1993* (DS3 and STS-1 standard)
- *ANSI T1.404a-1996* (DS3 metallic interface)
- *ITU Recommendation G.703* (DS3 and E3 standard)
- *ITU Recommendation G.823* and G.824 (jitter and wander)
- *Bellcore GR499*, Issue 1, 12/89 (formerly *TR-TSY-000499*) (DS3 and STS-1 requirements)
- *Bellcore GR253*, Issue 2, 12/91 (formerly *TA-NWT-000253*) (STS-1 requirements and jitter)
- *Bellcore TR-TSY-000191*, Issue 1, 5/86 (AIS and LOS)
- *ETSI TBR24* and *TBR25* (E3 terminal equipment interface)
- *ETSI ETS 300 686* and *ETS 300 687* (E3 standard)
- *AT&T Technical Reference TR54014*, May 1992 (Accunet Interface Specification for DS-3 jitter only)

Appendix B

B.1 Evaluation Module Schematic

Figure B-1. Recommended Schematic for the CN833x Device



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