VG-100A
CMOS V40™ MULTI-FUNCTION PERIPHERAL CHIP

February 1988

Features

- ☐ Dynamic RAM controller
- ☐ Refresh logic
- ☐ Peripheral I/O address decoder
- ☐ Memory address decoder (RAM and ROM)
- ☐ NMI control register
- ☐ Speaker clock generator
- ☐ 1.5 micron CMOS technology
- ☐ 64-pin shrink DIP package (optional flatpack)

Description

The VG-100A integrates the DRAM control and refresh functions, NMI control register, and address decoding functions. When used with the companion VG-200A and NEC's V40 microprocessor, a functionally compatible PC can be integrated by using just these three chips plus minimum glue logic.

Pin Description

Symbol	Function
BUFOFF	This active high output should be connected to the BUFOFF input of the VG-200A. Signal goes high when any of the following I/O hex address are accessed: 00-0F, 20-2F, 40-4F, 60-6F, 72, 73, 80-8F, A0-AF, C0-CF, or E0-EF. A CPU access to F0000-FFFFF will also force BUFOFF high.
AD0-AD7	V40 address/data lines 0-7. CMOS inputs.
A8-A15	V40 addresses 8-15. CMOS inputs.
A16-A19	V40 address/status lines 16-19. CMOS inputs.
MA0-MA7 (Note 1)	Multiplexed $\overline{RAS}$/$\overline{CAS}$ and refresh addresses for DRAM. During $\overline{RAS}$, CPU addresses A0-A7 are sent out; during $\overline{CAS}$, addresses A9-A16 are transmitted; during a refresh, addresses A0-A7 are sent. These outputs must be buffered.
$\overline{REFRQ}$	Refresh request from V40. CMOS input.
MERROR	Parity error output from VG-200A. Includes error results for both on-board and expansion RAMs. CMOS input.
GND	System ground.
CPUCLK	V40 CMOS clock output; actually system clock divided by 2.
EXTRDY	Ready line from expansion boards. A low indicates not ready. TTL input with internal pull-up.
$\overline{RAS}$	Active low row select. Goes low during memory cycles and refresh cycles. Active from 0 to 1 Mbyte. Should be connected to all RAMs directly without decoding, although buffering is required.
$\overline{CAS}$ (Note 2)	Active low column select. Goes low during memory cycles and high during refresh. Active from 0 to 1 Mbyte. External bank decoding and buffering required.
RD73	Goes high when I/O 73_H is read. I/O 73_H is the internal read/write register of the VG-100A used by the BIOS during emulation. This output should be OR'd with $\overline{BUFEN}$ of the V40 to control the transceiver between the AD and local data bus.
$\overline{RD72}$	Goes low when I/O 72_H is read. This address is provided for a system configuration register. If a basic system is designed as shown in the App Note, this register is not needed, and DB7 should be pulled up. A high on DB7 when I/O 72_H is read indicates to the BIOS that there is no register. If the register is present, DB7 should be low.
SW2	A high indicates that the 8087 co-processor chip is installed; a low indicates that it is not. CMOS input.
NMI	Sent to V40 NMI input pin. This is an OR'ing of RAM parity results, 8087 interrupt, EXTNMI, and other proprietary logic. A high indicates an NMI, and the output will be 6 clock pulses wide regardless of the input pulse width.
$\overline{IORD}$	Active low. CMOS I/O read control from the V40.
$\overline{IOWR}$	Active low. CMOS I/O write control from the V40.
MA8	Multiplexed $\overline{RAS}$/$\overline{CAS}$ and refresh address for DRAM. During $\overline{RAS}$, CPU address A8 is sent out; during $\overline{CAS}$, address A17 is transmitted; during a refresh, refresh address A8 is sent. This output must be buffered.
MA9	Multiplexed $\overline{RAS}$/$\overline{CAS}$ and refresh address for DRAM. During $\overline{RAS}$, CPU address A18 is sent out; during $\overline{CAS}$, address A19 is transmitted; during a refresh, MA9 is a don't care. This output must be buffered.
PPSEL	This directs one of two internally-decoded printer port addresses to appear on PRTCS. When low, I/O addresses $3BC_H$-$3BF_H$ will appear, and when high, addresses 378_H-$37F_H$. CMOS input with internal pull-up resistor.
INT87	8087 interrupt; enabled by SW2. A high on this TTL input will cause an NMI.
$\overline{EXTNMI}$	Extra NMI input: TTL with internal pullup. OR'd with other NMI inputs , and not controlled by NMI register. Must be qualified with V40 control signal ($\overline{IORD}$, $\overline{IOWR}$, $\overline{MRD}$, $\overline{MWR}$).
BS1	V40 CMOS bus status input. High = write; low = read.
BS2	V40 CMOS bus status input. High = memory; low = I/O.
$\overline{LOROM}$	Active low. Decoded memory address from F0000 to F7FFF. Intended for OEM ROM.
$\overline{HIROM}$	Active low. Decoded memory address from F8000 to FFFFF. Intended for BIOS ROM.
$\overline{PRTCS}$	Active low; Decoded I/O address for printer. See PPSEL.
RDY	Ready output to V40

Pin Description (cont)

Symbol	Function
$\overline{PPICS}$	Active low; Decoded I/O address (60_H-62_H — same as IBM) for 8255 controller or equivalent (VG-200A)
RESET	Active high, TTL input. Low = run; high = reset.
SYSASTB	Active high, TTL. The result of the OR'ing of the V40 ASTB and the 8087 ASTB.
TCLK	The CPUCLK divided by 6. Used by the V40 as TCU input clock. Output is 1.1913 MHz required for IBM compatibility.
$\overline{MRD}$	Active low, CMOS. Memory read control from V40.
$\overline{MWR}$	Active low, CMOS. Memory write control from V40.
SA16-SA19	System addresses. The result of input pins A16-A19 being latched internally by SYSASTB.
V_{CC}	+5 V power supply.

Notes:

(1) Address multiplexer is designed to use either 256K x 1 or 1M x 1 DRAMS

(2) If three banks of 256K or 1M DRAMs are located on the local bus, caution must be used when decoding for CAS. The standard PC display adapter resides in B0000-BFFFF and the EGA adapter starts at A0000. Therefore, decoding for CAS must insure that the DRAM is disabled when the display adapter is addressed. If 1M DRAMs are used, care must be taken to avoid bus conflicts above C0000 as well.

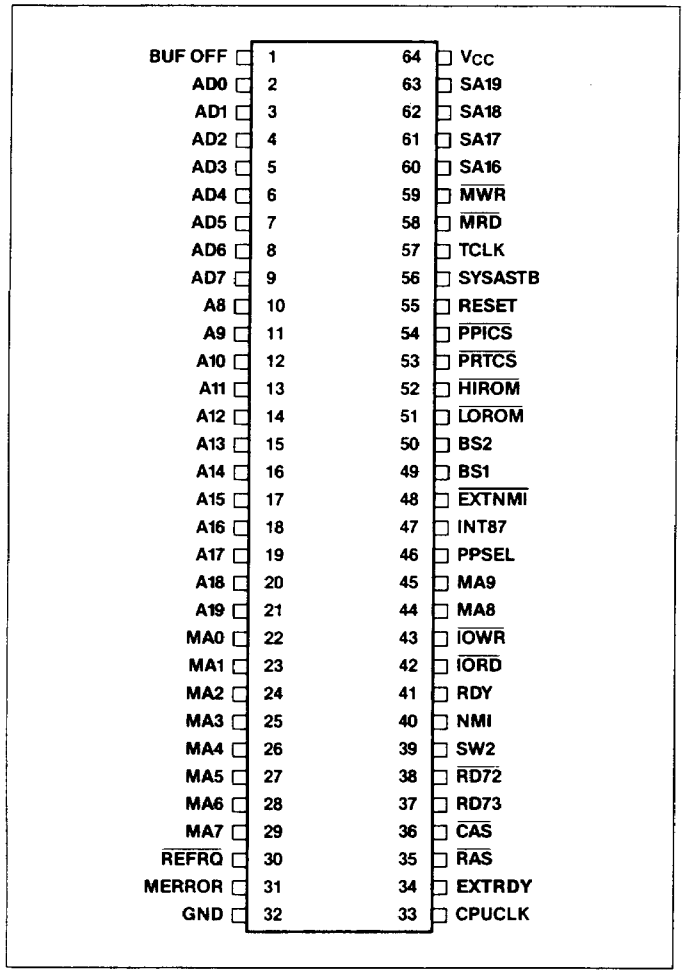
Absolute Maximum Ratings

$T_A = 25°C$

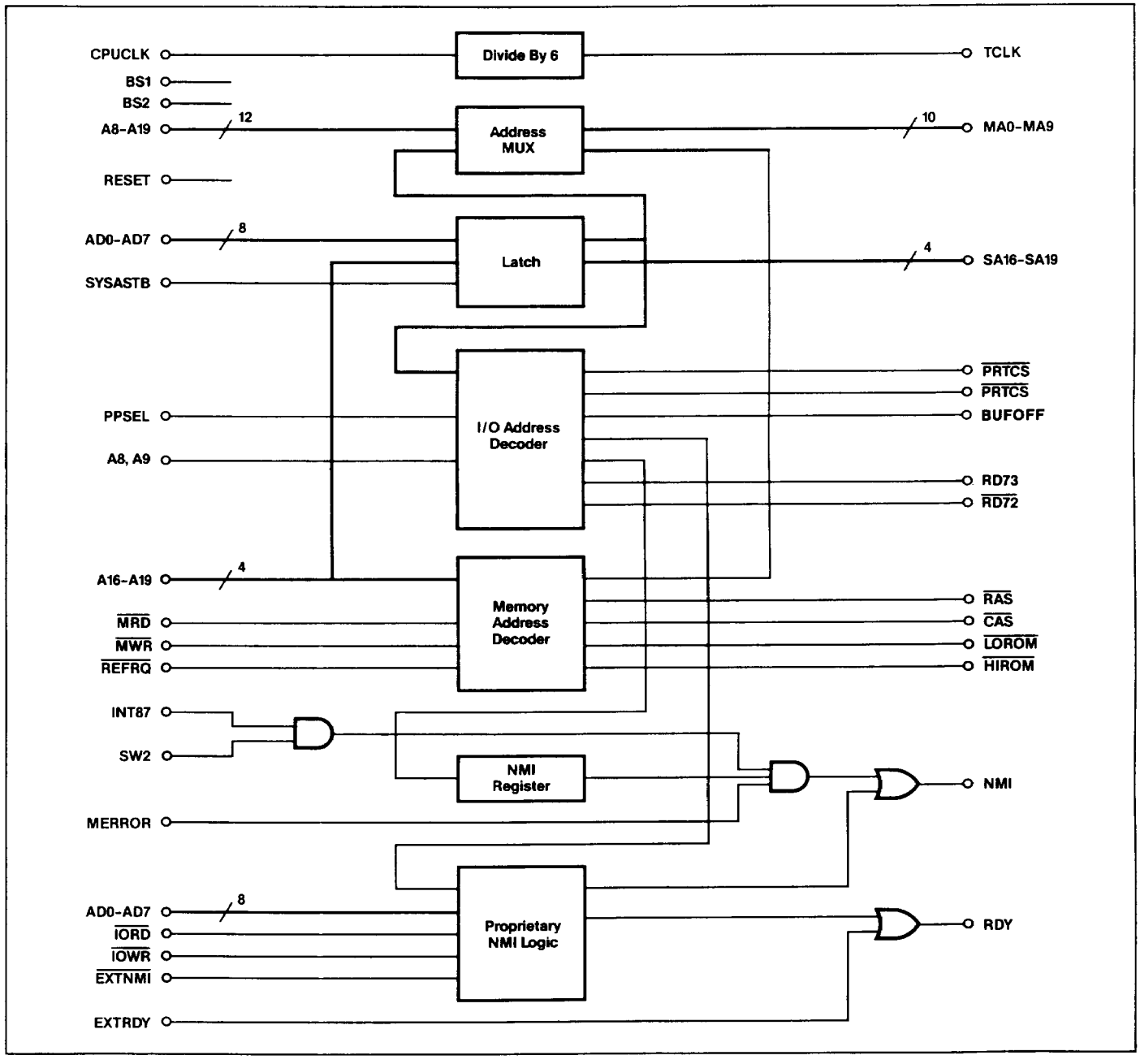
Power supply voltage	−0.5 to +7 V
Input voltage	−0.5 to (V_{CC} + 0.5) V
Output current	20 mA
Operating temperature range	−40 to +85°C
Storage temperature range	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Pin Configuration



Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Limits When interfacing with CMOS: Min	Max	When interfacing with TTL: Min	Max	Unit
Power supply voltage	V_{CC}	4.5	5.5	4.75	5.25	V
Operating temperature	T_{opt}	−40	+85	0	+70	°C
Low-level input voltage	V_{IL}	0	0.3 V_{CC}	0	0.8	V
High-level input voltage	V_{IH}	0.7 V_{CC}	V_{CC}	2.0	V_{CC}	V
Positive Schmitt trigger voltage	V_P	2.2	3.6	1.3	2.2	V
Negative Schmitt trigger voltage	V_N	0.9	2.8	0.7	1.7	V
Hysteresis	V_H	0.3	1.5	0.3	1.5	V
Rise/fall time	t_r/t_f	0	10	0	10	ns

DC Characteristics

CMOS interface levels: V_{CC} = 5.0 V ± 10%; T_{opt} = −40 to +85 °C
TTL interface levels: V_{CC} = 5.0 V ±5%; T_{opt} = 0 to +70 °C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Quiescent current	I_Q		0.1	200	μA	$V_{IN} = V_{CC}$ or GND
Off-state output leakage current	I_{OLK}			10	μA	$V_O = V_{CC}$ or GND
Operating current	I_{CC}		3		μA	1 MHz/cell
Input current	I_{IN}		10^{-5}	10	μA	$V_{IN} = V_{CC}$ or GND
Low-level output current (Note 1)	I_{OL}	4 4.3	11		mA mA	CMOS TTL
High-level output current (Note 2)	I_{OH}	4 4.3	7		mA mA	CMOS TTL
Low-level output voltage	V_{OL}			0.1	V	I_O = 0 mA
High-level output voltage	V_{OH}	V_{CC} − 0.1			V	I_O = 0 mA

Notes:

(1) V_{OL} = 0.4 V.

(2) $V_{OH} = V_{CC}$ − 0.4 V.

AC Characteristics

CMOS interface levels: V_{CC} = 5.0 V ± 10%; T_{opt} = −40 to +85 °C
TTL interface levels: V_{CC} = 5.0 V ± 5%; T_{opt} = 0 to +70 °C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Toggle frequency	f_{clk}	70 75			MHz MHz	CMOS TTL
Internal gate delay time	t_{PD}		1.4		ns	F/O = 3; L = 3 mm
Input buffer delay time	t_{PD}		2.0		ns	F/O = 3; L = 3 mm
Output buffer delay time	t_{PD}		4.5		ns	C_L = 15 pF
Output rise time	t_r		3.5		ns	C_L = 15 pF
Output fall time	t_f		2.5		ns	C_L = 15 pF

Timing Characteristics

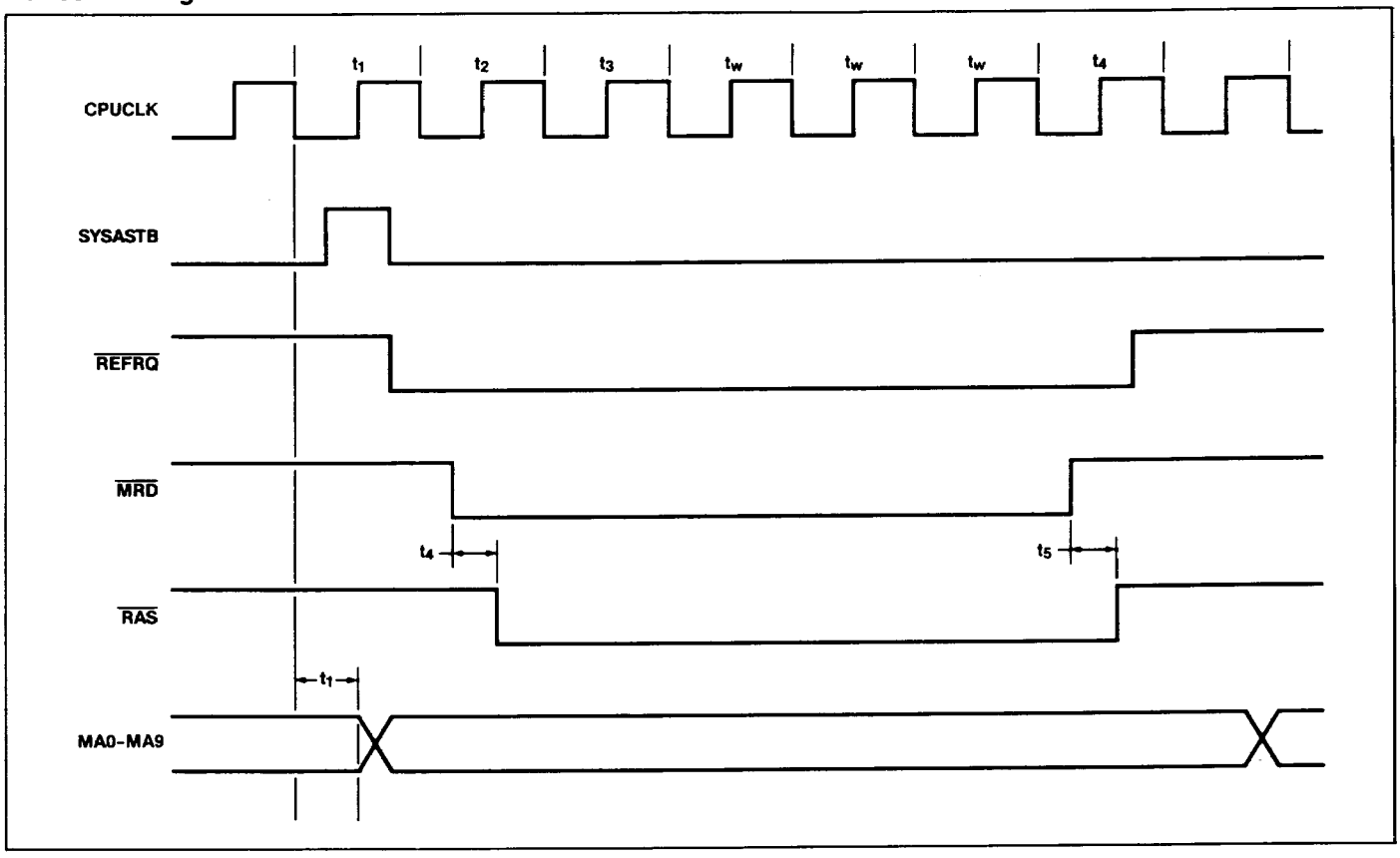
Parameter	Symbol	Limits Min	Max	Unit
MA0-MA9 (RAS) from $t_4\downarrow$	t_1	14	87	ns
MA0-MA9 (CAS) from $t_2\downarrow$	t_2	7	34	ns
MA0-MA9 hold from $\overline{MRD}/\overline{MWR}\uparrow$	t_3	7	40	ns
$\overline{RAS}\downarrow$ from $\overline{MRD}/\overline{MWR}\downarrow$	t_4	3	19	ns
$\overline{RAS}\uparrow$ from $\overline{MRD}/\overline{MWR}\uparrow$	t_5	3	19	ns
$\overline{CAS}\downarrow$ from $t_3\uparrow$	t_6	6	26	ns
$\overline{CAS}\uparrow$ from $\overline{MRD}/\overline{MWR}$	t_7	6	31	ns
SA16-SA19 from $t_4\downarrow$	t_8	17	84	ns
$\overline{LOROM}/\overline{HIROM}$ from $t_4\downarrow$	t_9	17	99	ns
BUFOFF$\uparrow$ from $t_4\downarrow$	t_{10}	16	96	ns
BUFOFF$\downarrow$ from $t_4\downarrow$	t_{11}	16	96	ns
$\overline{PPICS}/\overline{PRTCS}\downarrow$ from $t_4\downarrow$	t_{12}	19	100	ns
$\overline{PPICS}/\overline{PRTCS}\uparrow$ from $t_4\uparrow$	t_{13}	19	100	ns
$\overline{RD72}\downarrow$ from CPUCLK$\uparrow$	t_{14}	9	43	ns
$\overline{RD72}\uparrow$ from $\overline{IORD}/\overline{IOWR}\uparrow$	t_{15}	7	32	ns
RD73$\uparrow$ from CPUCLK$\uparrow$	t_{16}	10	48	ns
RD73$\downarrow$ from $\overline{IORD}/\overline{IOWR}\uparrow$	t_{17}	8	37	ns
BUFOFF$\uparrow$ from CPUCLK$\uparrow$	t_{18}	8	42	ns
BUFOFF$\downarrow$ from $\overline{IORD}/\overline{IOWR}$	t_{19}	7	31	ns
RDY$\downarrow$ from $\overline{IORD}/\overline{IOWR}$	t_{20}	5	29	ns
RDY$\uparrow$ from CPUCLK$\downarrow$	t_{21}	7	35	ns
NMI$\uparrow$ from $\overline{IORD}/\overline{IOWR}$	t_{22}	6	30	ns
NMI from $\overline{IORD}/\overline{IOWR}\uparrow$	t_{23}	6	30	ns
RDY$\downarrow$ from EXTRDY$\downarrow$	t_{24}	5	25	ns
RDY$\uparrow$ from EXTRDY$\uparrow$	t_{25}	5	25	ns
MERROR$\uparrow$ setup to CPUCLK$\uparrow$	t_{26}	24		ns
MERROR minimum pulse width	t_{27}	20		ns

Timing Characteristics

Parameter	Symbol	Limits Min	Limits Max	Unit
INT87↑ setup to CPUCLK↑	t_{28}	28		ns
INT87 minimum pulse width	t_{29}	20		ns
NMI↑ from MERROR, INT87	t_{30}	6	29	ns
NMI↓ from CPUCLK	t_{31}	7	34	ns
SYSASTB delay, V40 out to VG-100A in	t_{32}		20	ns

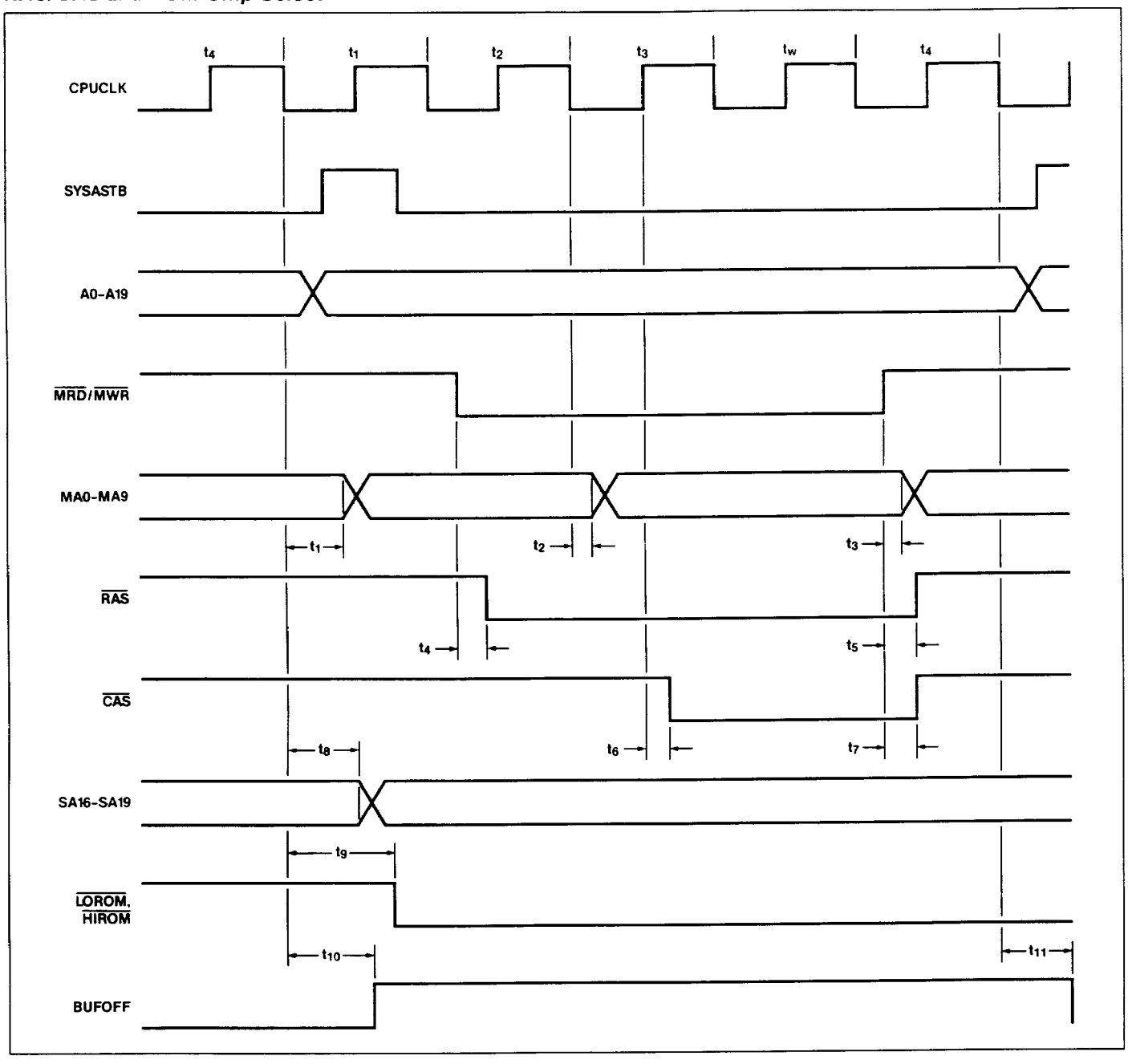
Timing Waveforms

Refresh Timing



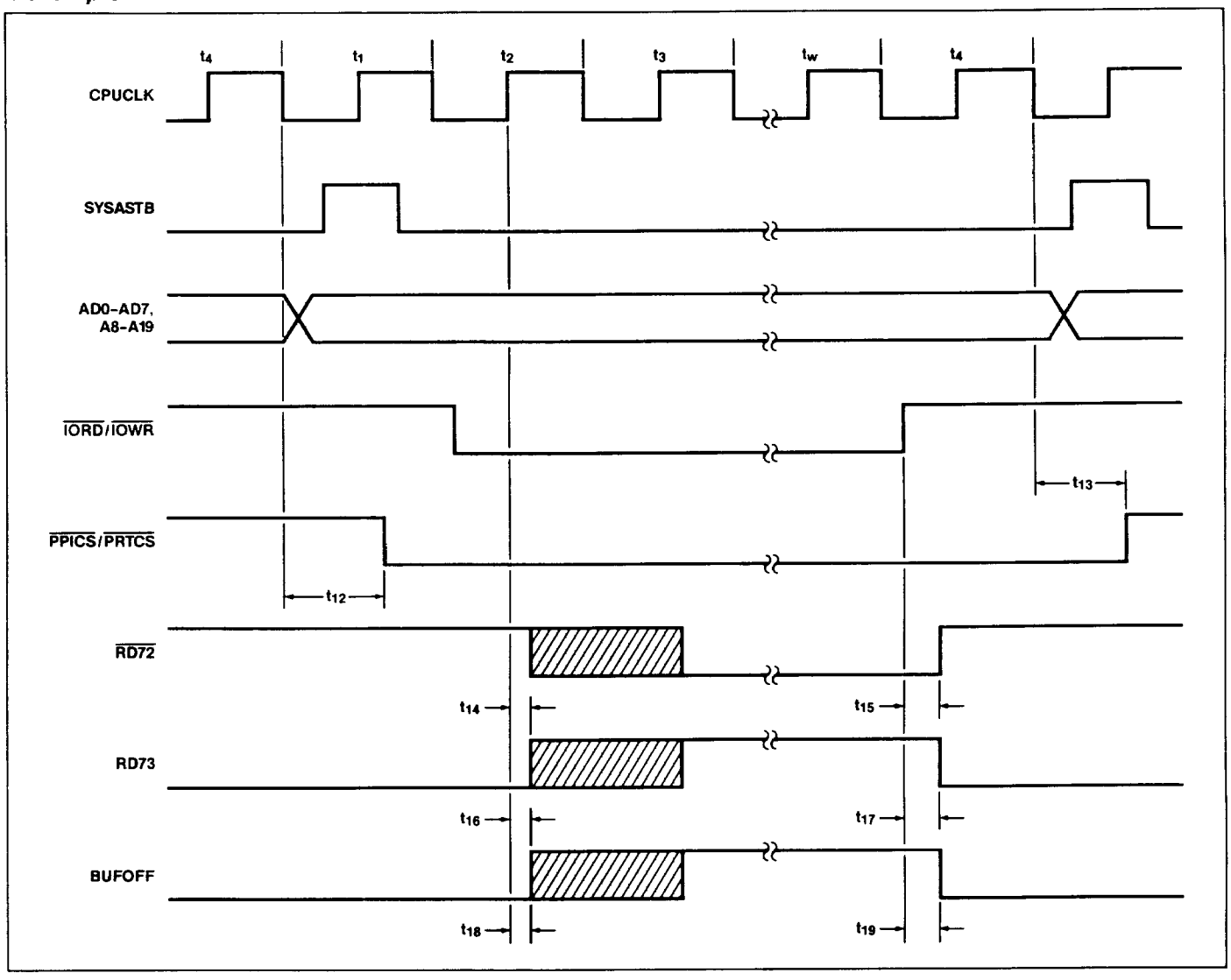
Timing Waveforms (cont)

RAS/CAS and ROM Chip Select



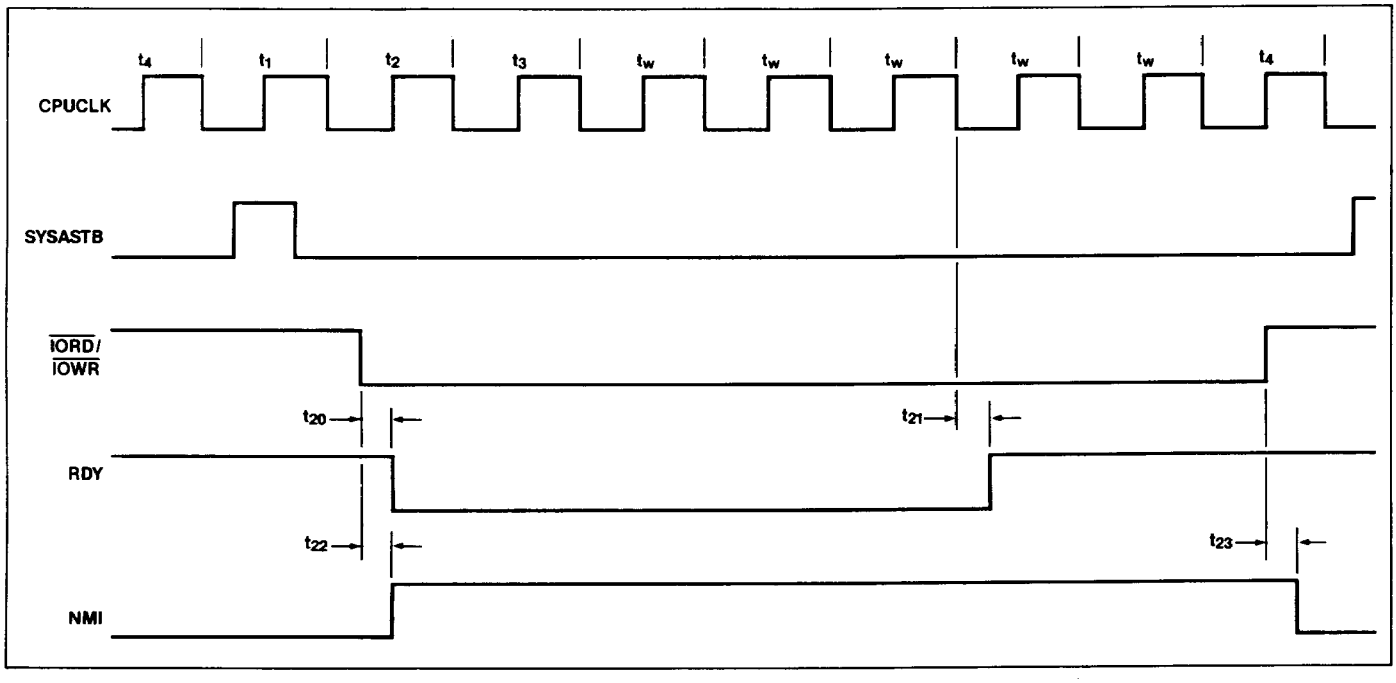
Timing Waveforms (cont)

I/O Chip Selects

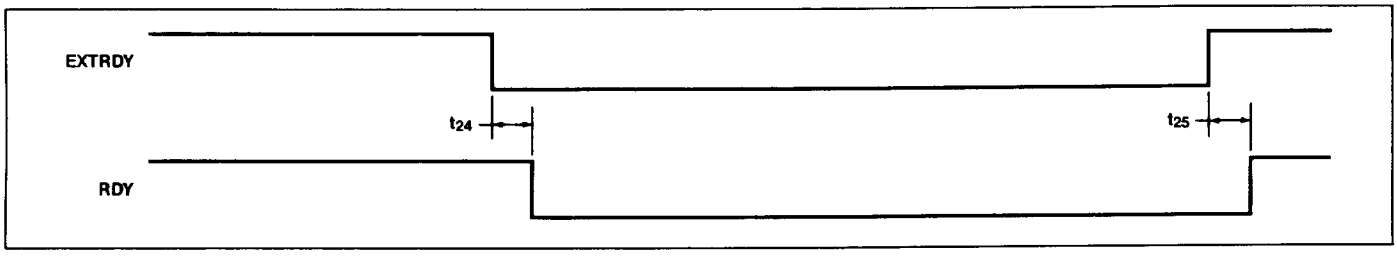


Timing Waveforms (cont)

I/O Trapping

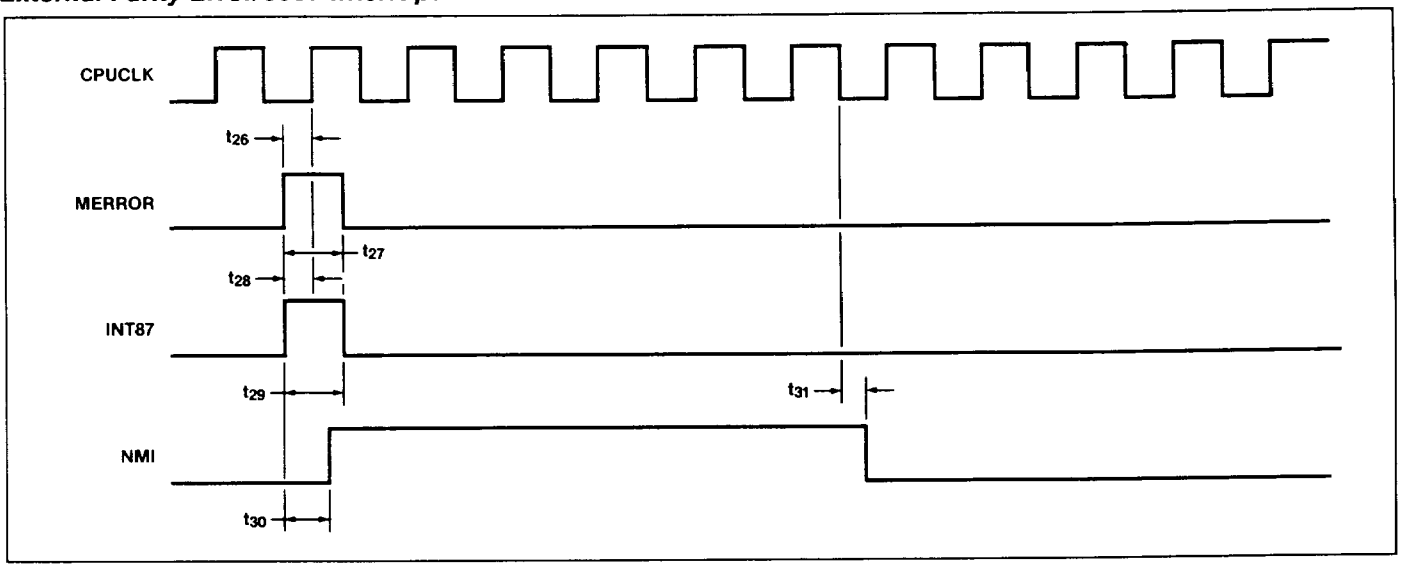


External Ready Timing

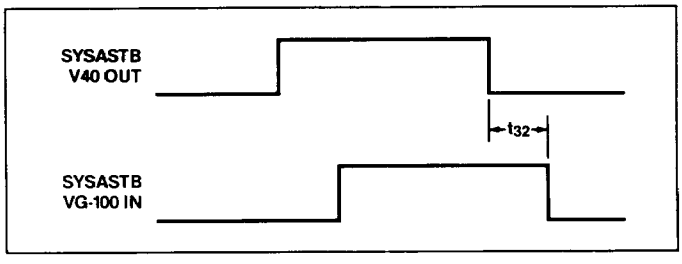


Timing Waveforms (cont)

External Parity Error/8087 Interrupt



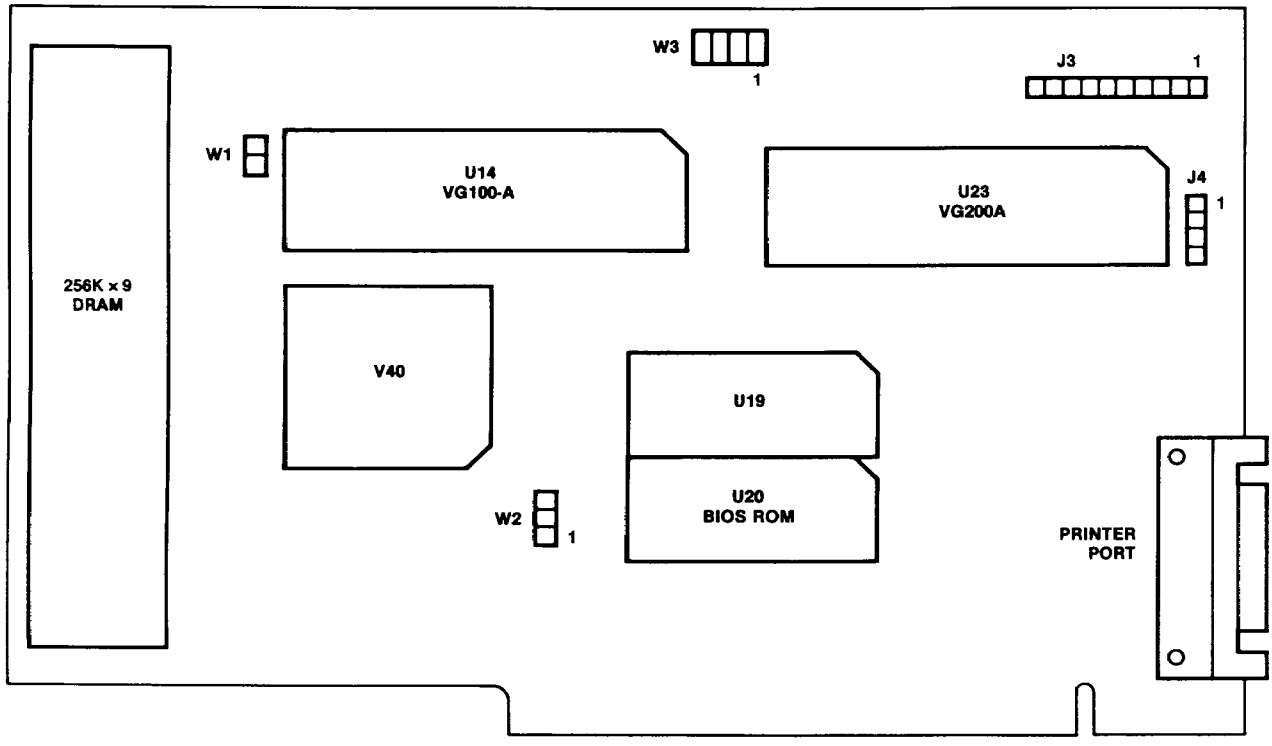
SYSASTB Timing



Applications Information

The following figure is an actual size representation of a fully functional IBM PC-compatible computer, built using the NEC V40 microprocessor and the Vadem VG-100A and VG-200A.

Typical Application



W1
short = printer port at 3BC-3BF
open = printer port at 378-37F

W2
1-2 32K byte EPROM
2-3 128K byte page mode EPROM

J4

1	SIO output
2	N.C.
3	SIO input
4	Ground

W3-1	W3-2	Display Adapter
short	short	= reserved (EGA)
open	short	= CGA 320 x 200
short	open	= CGA 640 x 200
open	open	= monochrome 80 x 25

W3-3	W3-4	No. of floppies
short	short	1
open	short	2
short	open	3
open	open	4

J3

1	Speaker
2	Speaker
3	Keyboard clock
4	Keyboard data
5	Reset
6	Ground
7	V_{CC}
8	External NMI
9	N.C.
10	N.C.

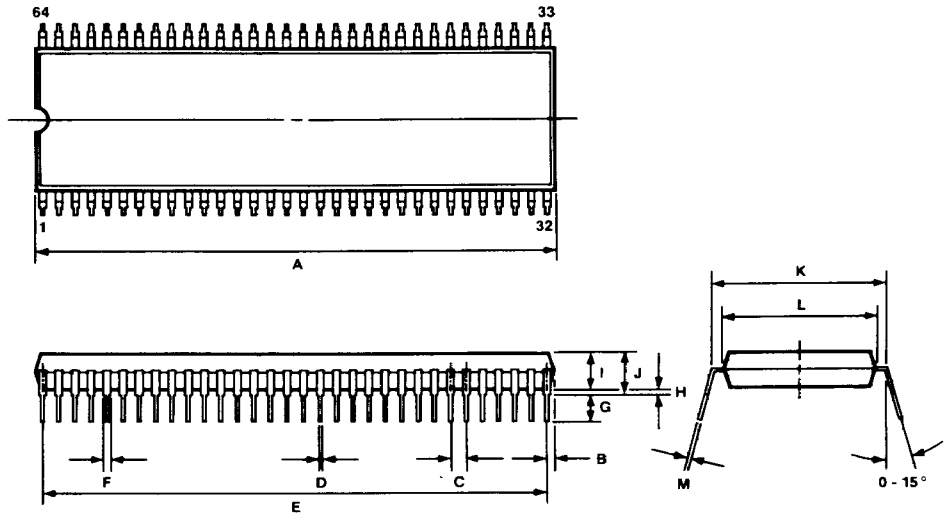
Physical Dimensions

64-Pin Plastic Shrink DIP (750 mil)

Item	Millimeters	Inches
A	58.68 max	2.311 max
B	1.78 max	.07 max
C	1.778 [TP]	.07 [TP]
D	.5 ±.10	.02 $^{+.004}_{-.005}$
E	55.12	2.17
F	.9 min	.035 min
G	3.2 ±.3	.126 ±.012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	19.05 [TP]	.75 [TP]
L	17	.669
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:

1. Each lead centerline is located within .17 mm [.0007 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



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