VG-200A
CMOS V40™ MULTI-FUNCTION PERIPHERAL CHIP

February 1988

Features

- ☐ Keyboard logic
- ☐ Printer port
- ☐ Bus controller logic
- ☐ Speaker logic
- ☐ IBM configuration registers (8255)
- ☐ Parity logic including parity generator for on-board RAM
- ☐ 1.5 micron CMOS technology
- ☐ 64-pin shrink DIP package (optional flatpack)

Description

The VG-200A integrates the printer port, keyboard controller, speaker logic, IBM configuration registers, and both CPU and DMA bus controller logic. When used with the companion VG-100A and NEC's V40 microprocessor, a functionally compatible PC can be integrated by using just these three chips plus minimal glue logic.

Pin Description

Symbol	Function
TGATE	Active high enable signal to V40 timer channel 2.
SD0-SD7	System data bus inputs. CMOS.
SA0, SA1	System address inputs. TTL.
IRQ1	Keyboard interrupt; should be connected to Interrupt Channel 1 of V40. A high on this pin causes an interrupt.
IRQ7	Printer interrupt; should be connected to Interrupt Channel 7 of V40. Output is through a three-state driver. A high on this pin causes an interrupt.
SPEAKER	Active high speaker outputs. Must be buffered.
$\overline{\text{IOCHK}}$	Input to the parity logic from the expansion memory. TTL input with internal pull-up. A low on this pin indicates a parity error.
PARIN	TTL output signal from the parity RAM. If parity is not being used this pin should be tied to PAROUT.
$\overline{\text{IORD}}$	Active low. CMOS I/O read control from the V40.
$\overline{\text{IOWR}}$	Active low. CMOS I/O write control from the V40.
MERROR	Parity error output to VG-100A. A high indicates a parity error in either the on-board or expansion RAM.
PAROUT	Parity RAM input signal. During a memory write cycle, PAROUT will be written into the parity RAM on the falling edge of $\overline{\text{CAS}}$. Output level is generated by the internal parity generator.
INTD/$\overline{\text{EXTD}}$	Indicates the position of the floppy disk controller; a low means the FDC is on the expansion bus, while a high (or open) indicates the local bus. This is a CMOS input with an internal pull-up.
$\overline{\text{FDCCS}}$	Used in conjunction with INTD/$\overline{\text{EXTD}}$ pin. When INTD/$\overline{\text{EXTD}}$ is low, this pin should be tied high or left open. When INTD/$\overline{\text{EXTD}}$ is high, this input should be driven by the result of an AND'ing between FDC Chip Select (low true) and FDC DACK (low true). FDCCS is used by the buffer control logic, and qualified internally with AEN, $\overline{\text{IORD}}$, and $\overline{\text{IOWR}}$. It is a TTL input with an internal pull-up.
$\overline{\text{BOFF}}$	This is an extra input to the buffer control logic. Except when AEN is high, a low on this pin produces a high on $\overline{\text{BUFON}}$. This input can be used if additional hardware, such as a real-time clock, is added to the local bus, and if unused it can be left open. It is a TTL input with internal pull-up.
$\overline{\text{MEM}}$ (Note 1)	This is a TTL input to the buffer control logic, and should be decoded to act as an on-board memory chip select, going low only when the DRAM present on the local bus is accessed.
BUFDIR	This signal controls the direction for both CPU and DMA data cycles, and should be connected to the direction pin on the expansion bus data buffer. The control logic will adapt to the amount of memory on the local bus and the location of the floppy disk controller.
BUFOFF	This active high input should be connected to the BUFOFF output of the VG-100A. Signal goes high when any of the following I/O hex address are accessed: 00-0F, 20-2F, 40-4F, 60-6F, 72, 73, 80-8F, A0-AF, C0-CF, or E0-EF. A CPU access to F0000-FFFFF will also force BUFOFF high.
SW2	A high indicates that the 8087 co-processor chip is installed; a low indicates that it is not. CMOS input with internal pull-up.
SYSASTB	Active high TTL input. The result of the OR'ing of the V40 ASTB and the 8087 ASTB.
AEN	A high on this TTL input indicates that there is a DMA address on the bus. Signal can be created by NAND'ing the V40 $\overline{\text{DACK}}$ signals together with the $\overline{\text{REFRQ}}$.
SW5, SW6	Indicates the type of display adapter being used. CMOS inputs with internal pull-ups. SW6 / SW5 / Type L / L / Reserved L / H / CGA 320 x 200 H / L / CGA 640 x 200 H / H / Monochrome 80 x 25
RESET	Active high TTL input. Low = run; high = reset.

Note:

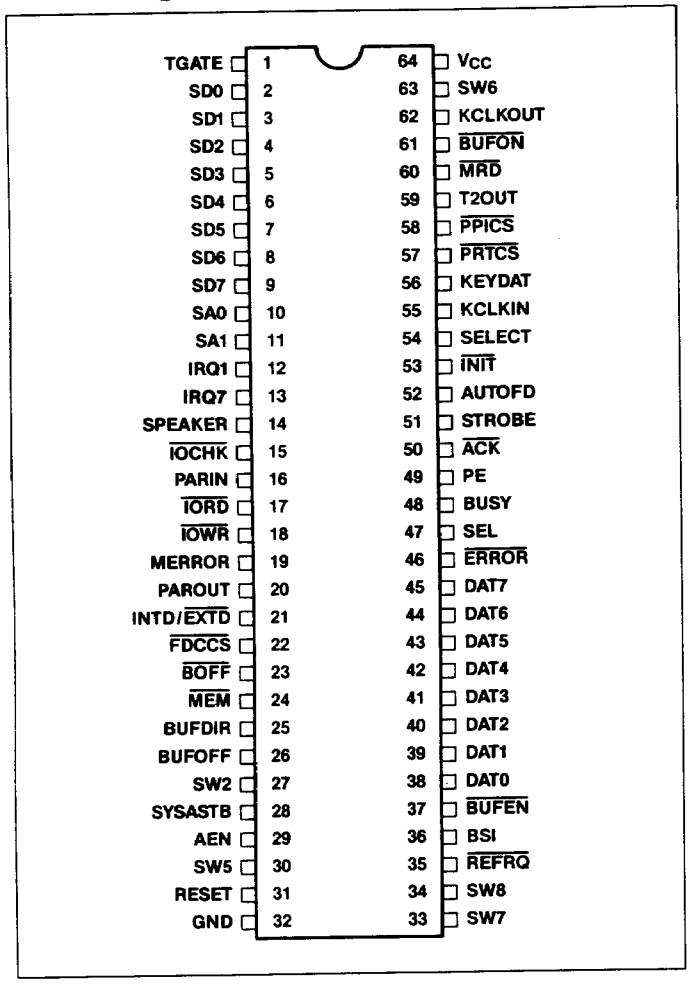
(1) If three banks of 256K (or one bank of 1M) DRAMs are located on the local bus, caution must be used when decoding $\overline{\text{MEM}}$. The standard PC display adapter resides in B0000-BFFFF and the EGA adapter starts at A0000. Therefore, decoding for $\overline{\text{MEM}}$ must insure that it is high when the display adapter is addressed. If 1M DRAMs are used, care must be taken to avoid bus conflicts above C0000 as well. If less than 640K of memory is present on the local bus, MEM must be active for only the amount of memory present.

Symbol	Function
GND	System ground.
SW7, SW8	Sets the number of floppy disk drives installed. CMOS inputs with internal pull-ups. SW8 SW7 Number L L 1 L H 2 H L 3 H H 4
$\overline{\text{REFRQ}}$	Refresh request from V40. CMOS input.
BS1	Bus status from V40. CMOS input.
$\overline{\text{BUFEN}}$	Buffer enable control from the V40. CMOS input.
DAT0-DAT7	Printer port data outputs.
$\overline{\text{ERROR}}$ (Note 2)	A low on this pin indicates a printer error.
SEL (Note 2)	A high means that the printer has been selected.
BUSY (Note 2)	A high indicates that the printer is busy and not ready for data.
PE (Note 2)	A high means that the printer is out of paper.
$\overline{\text{ACK}}$ (Note 2)	A low indicates that the character has been received.
STROBE	Positive going pulse which strobes data into the printer. Should be inverted once.
AUTOFD	A high enables a line feed after each line of data is printed. Should be inverted once.
INIT	A high resets the printer. Should be inverted once.
SELECT	A high selects the printer. Should be inverted once.
KEYCLKIN	Keyboard clock signal used to clock data into the internal shift register of the VG-200A. This TTL input should be buffered with a Schmitt-triggered input device; if an XX14 is used, an additional inverter must follow the XX14 to maintain proper polarity.
KEYDAT	Keyboard bidirectional serial data. TTL input with internal pull-up.
$\overline{\text{PRTCS}}$	Printer port chip select input. Active low TTL input with internal pull-up.
$\overline{\text{PPICS}}$	Chip select input for 8255 logic, including keyboard controller and configuration register. Active low TTL input with internal pull-up.
T2OUT	V40 timer channel 2 clock output.
$\overline{\text{MRD}}$	V40 memory read control. CMOS input.
$\overline{\text{BUFON}}$	This output should be connected to the enable pin of the expansion bus data buffer. It will disable the buffer when BUFOFF (VG-100A) goes high; when $\overline{\text{FDCCS}}$, $\overline{\text{PRTCS}}$, $\overline{\text{PPICS}}$, or $\overline{\text{BOFF}}$ inputs go low; or whenever the local RAM is accessed. This control logic adapts to the amount of memory on the system bus and the location of the floppy disk controller, and functions the same whether during a CPU or a DMA cycle.
KCLKOUT	Output control for keyboard clock. Should be connected to the keyboard connector through an XX05 (open collector).
V_{CC}	+5 V power supply.

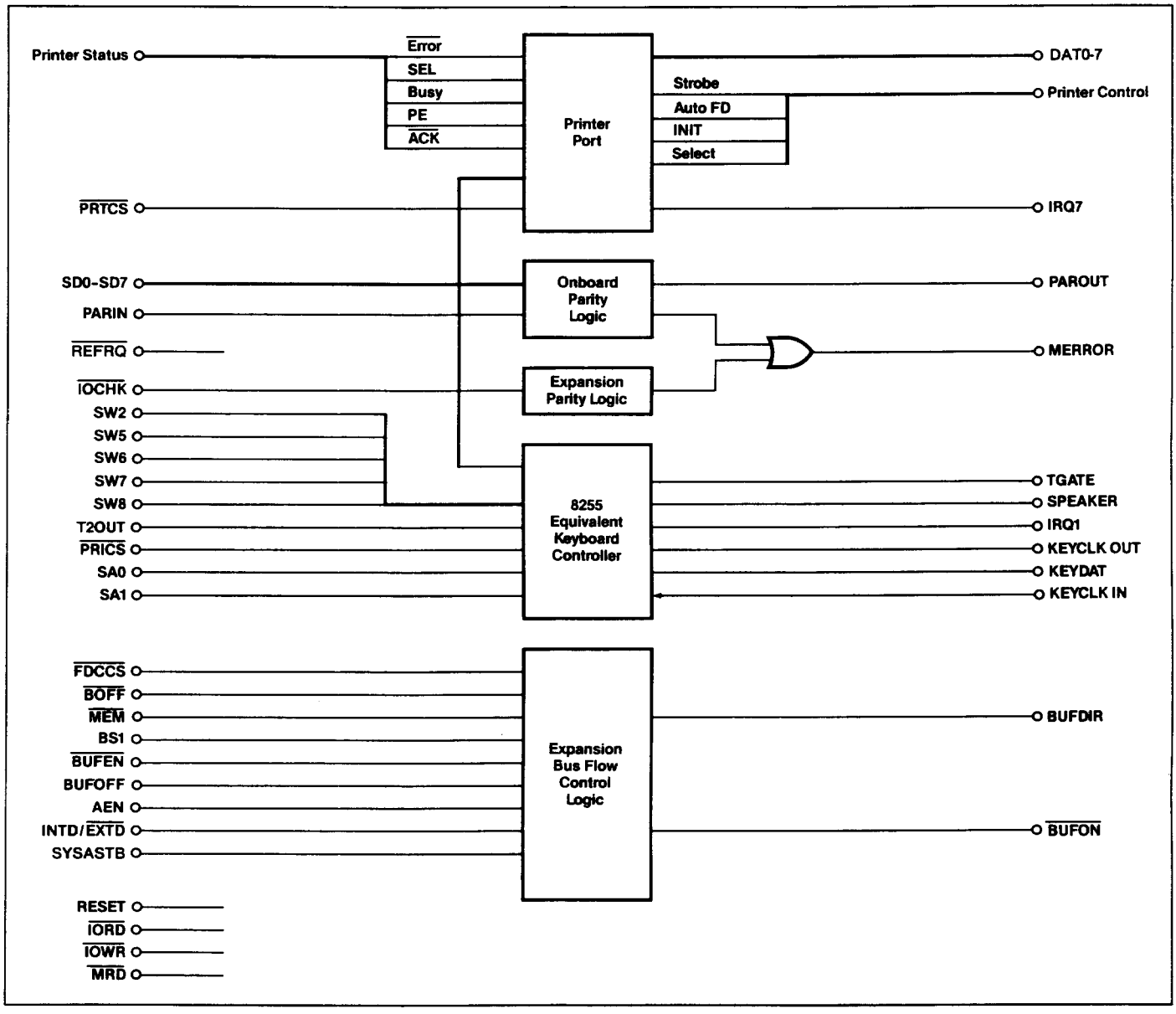
Note:

(2) These five signals are printer status inputs. All are TTL inputs with internal pull-up resistors.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage	−0.5 to +7 V
Input voltage	−0.5 to (V_{CC} + 0.5) V
Output current	20 mA
Operating temperature range	−40 to +85°C
Storage temperature range	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

DC Characteristics

CMOS interface levels: $V_{CC} = 5.0$ V ±10%; $T_{opt} = -40$ to +85°C
TTL interface levels: $V_{CC} = 5.0$ V ± 5%; $T_{opt} = 0$ to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Quiescent current	I_Q		0.1	200	µA	$V_{IN} = V_{CC}$ or GND
Off-state output leakage current	I_{OLK}			10	µA	$V_O = V_{CC}$ or GND
Operating current	I_{CC}		3		µA	1 MHz/cell
Input current	I_{IN}		10^{-5}	10	µA	$V_{IN} = V_{CC}$ or GND
Low-level output current (Note 1)	I_{OL}	4 4.3	11		mA mA	CMOS TTL
High-level output current (Note 2)	I_{OH}	4 4.3	7		mA mA	CMOS TTL
Low-level output voltage	V_{OL}			0.1	V	$I_O = 0$ mA
High-level output voltage	V_{OH}	V_{CC} − 0.1			V	$I_O = 0$ mA

Notes:

(1) $V_{OL} = 0.4$ V.

(2) $V_{OL} = V_{CC} - 0.4$ V.

AC Characteristics

CMOS interface levels: $V_{CC} = 5.0$ V ±10%; $T_{opt} = -40$ to +85°C
TTL interface levels: $V_{CC} = 5.0$ V ±5%; $T_{opt} = 0$ to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Toggle frequency	f_{clk}	70 75			MHz MHz	CMOS TTL
Internal gate delay time	t_{PD}		1.4		ns	F/O = 3; L = 3 mm
Input buffer delay time	t_{PD}		2.0		ns	F/O = 3; L = 3 mm
Output buffer delay time	t_{PD}		4.5		ns	$C_L = 15$ pF
Output rise time	t_r		3.5		ns	$C_L = 15$ pF
Output fall time	t_f		2.5		ns	$C_L = 15$ pF

Recommended Operating Conditions

Parameter	Symbol	Limits When interfacing with CMOS: Min	Max	When interfacing with TTL: Min	Max	Unit
Power supply voltage	V_{CC}	4.5	5.5	4.75	5.25	V
Operating temperature	T_{opt}	−40	+85	0	+70	°C
Low-level input voltage	V_{IL}	0	0.3 V_{CC}	0	0.8	V
High-level input voltage	V_{IH}	0.7 V_{CC}	V_{CC}	2.0	V_{CC}	V
Positive Schmitt trigger voltage	V_P	2.2	3.6	1.3	2.2	V
Negative Schmitt trigger voltage	V_N	0.9	2.8	0.7	1.7	V
Hysteresis	V_H	0.3	1.5	0.3	1.5	V
Rise/fall time	t_r/t_f	0	10	0	10	ns

Timing Characteristics

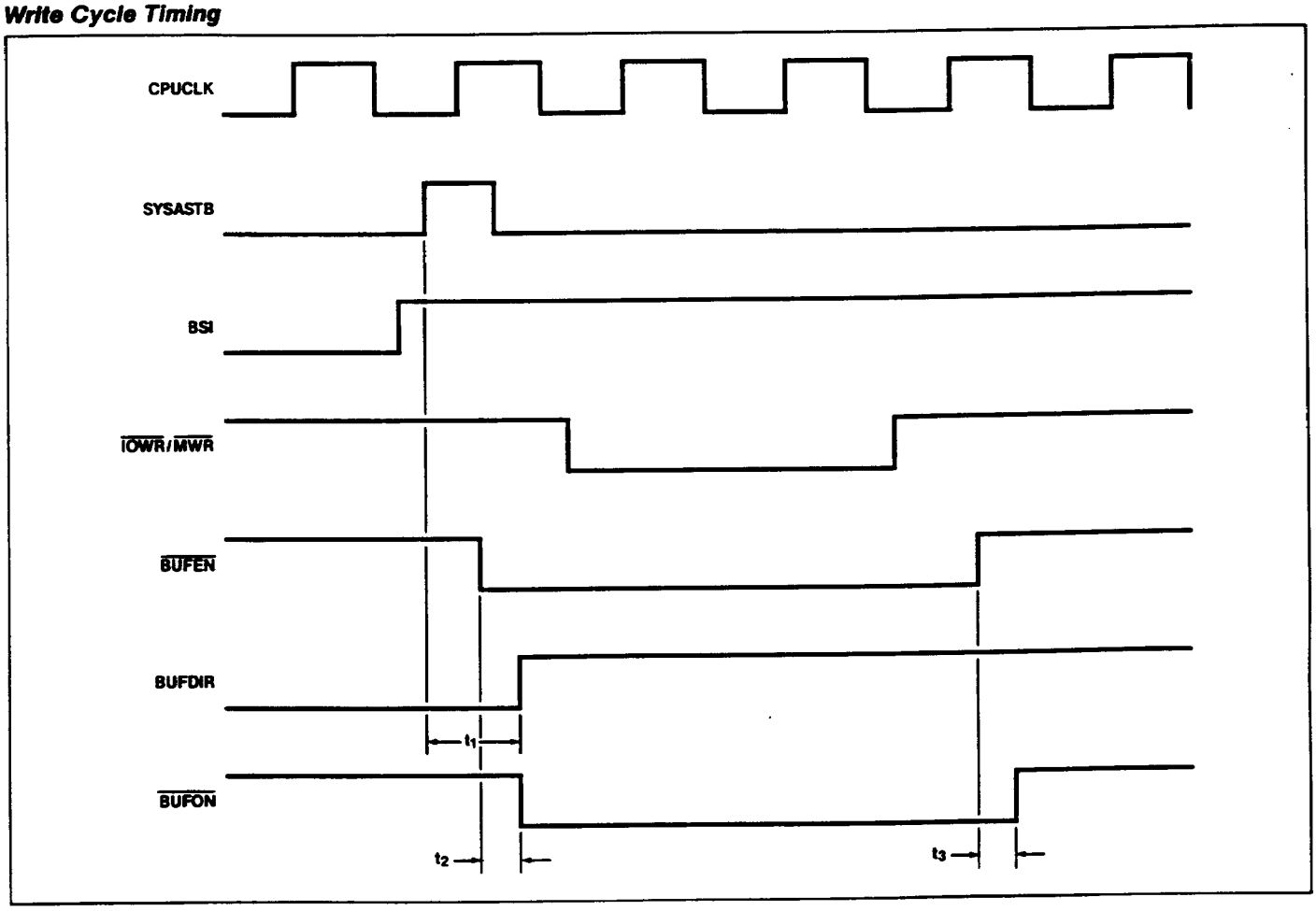
Parameter	Symbol	Limits Min	Max	Unit
SYSASTB↑ to BUFDIR	t_1	12	29	ns
$\overline{\text{BUFEN}}$↓ to $\overline{\text{BUFON}}$↓	t_2	4	24	ns
$\overline{\text{BUFEN}}$↑ to $\overline{\text{BUFON}}$↑	t_3	4	24	ns
$\overline{\text{PPICS}}/\overline{\text{PRTCS}}$ setup to $\overline{\text{IOWR}}$↓	t_4		25	ns
$\overline{\text{PPICS}}/\overline{\text{PRTCS}}$ hold from $\overline{\text{IOWR}}$↑	t_5		25	ns
SD0-SD7 setup to $\overline{\text{IOWR}}$↑	t_6	20		ns
SD0-SD7 hold from $\overline{\text{IOWR}}$↑	t_7	20		ns
$\overline{\text{IOWR}}$↑ to outputs	t_8	9	39	ns
$\overline{\text{IOWR}}$↑ to IRQ1↓	t_9	7	42	ns
KCLKOUT cleared from $\overline{\text{IOWR}}$↑	t_{10}	9	39	ns
KEYDAT cleared from $\overline{\text{IOWR}}$↑	t_{11}	8	46	ns
$\overline{\text{PPICS}}/\overline{\text{PRTCS}}$↓ to SD0-SD7	t_{12}	6	35	ns
$\overline{\text{PPICS}}/\overline{\text{PRTCS}}$↓ setup to $\overline{\text{IORD}}$↓	t_{13}	15		ns
$\overline{\text{IORD}}$↓ to SD0-SD7	t_{14}	5	24	ns
Printer status to SD0-SD7	t_{15}	6	32	ns
SD0-SD7 hold from $\overline{\text{IORD}}$↑	t_{16}	6	26	ns
Setup↓ to $\overline{\text{BUFEN}}$↓	t_{17}	25		ns
Hold↑ from $\overline{\text{BUFEN}}$↑	t_{18}	10		ns
$\overline{\text{BUFON}}$↓ from $\overline{\text{IORD}}/\overline{\text{IOWR}}$↓	t_{19}	9	46	ns
$\overline{\text{BOFF}}$↑ setup to $\overline{\text{BUFEN}}$↓	t_{20}	20		ns
$\overline{\text{BOFF}}$ hold from $\overline{\text{BUFEN}}$↑	t_{21}	10		ns
BS1 setup to SYSASTB↓	t_{22}	15		ns
BS1 hold from SYSASTB↓	t_{23}	10		ns
BUFDIR from SYSASTB↑	t_{24}	12	29	ns
BUFDIR from AEN↑	t_{25}	11	31	ns
BUFDIR from AEN↓	t_{26}	11	31	ns

Timing Characteristics (cont)

Parameter	Symbol	Limits Min	Limits Max	Unit
AEN↑ to $\overline{\text{BUFON}}$↓	t_{27}	4	25	ns
SD0-SD7 setup to $\overline{\text{MRD}}$/$\overline{\text{MWR}}$	t_{28}	35		ns
SD0-SD7 hold from $\overline{\text{MRD}}$/$\overline{\text{MWR}}$	t_{29}	10		ns
PIN setup to $\overline{\text{MRD}}$↑	t_{30}	35		ns
PIN hold from $\overline{\text{MRD}}$/$\overline{\text{MWR}}$	t_{31}	10		ns
SD-SD7 to PAROUT	t_{32}	5	26	ns
MERROR from $\overline{\text{MRD}}$↑	t_{33}	6	30	ns
$\overline{\text{IOCHK}}$↓ to MERROR↑	t_{34}	4	24	ns
KEYDAT setup to KCLKIN↑	t_{35}	25		ns
KEYDAT hold from KCLKIN↑	t_{36}	25		ns
IRQ1 from KCLKIN↑	t_{37}	5	28	ns
Delay SYSASTB	t_{38}		20	ns

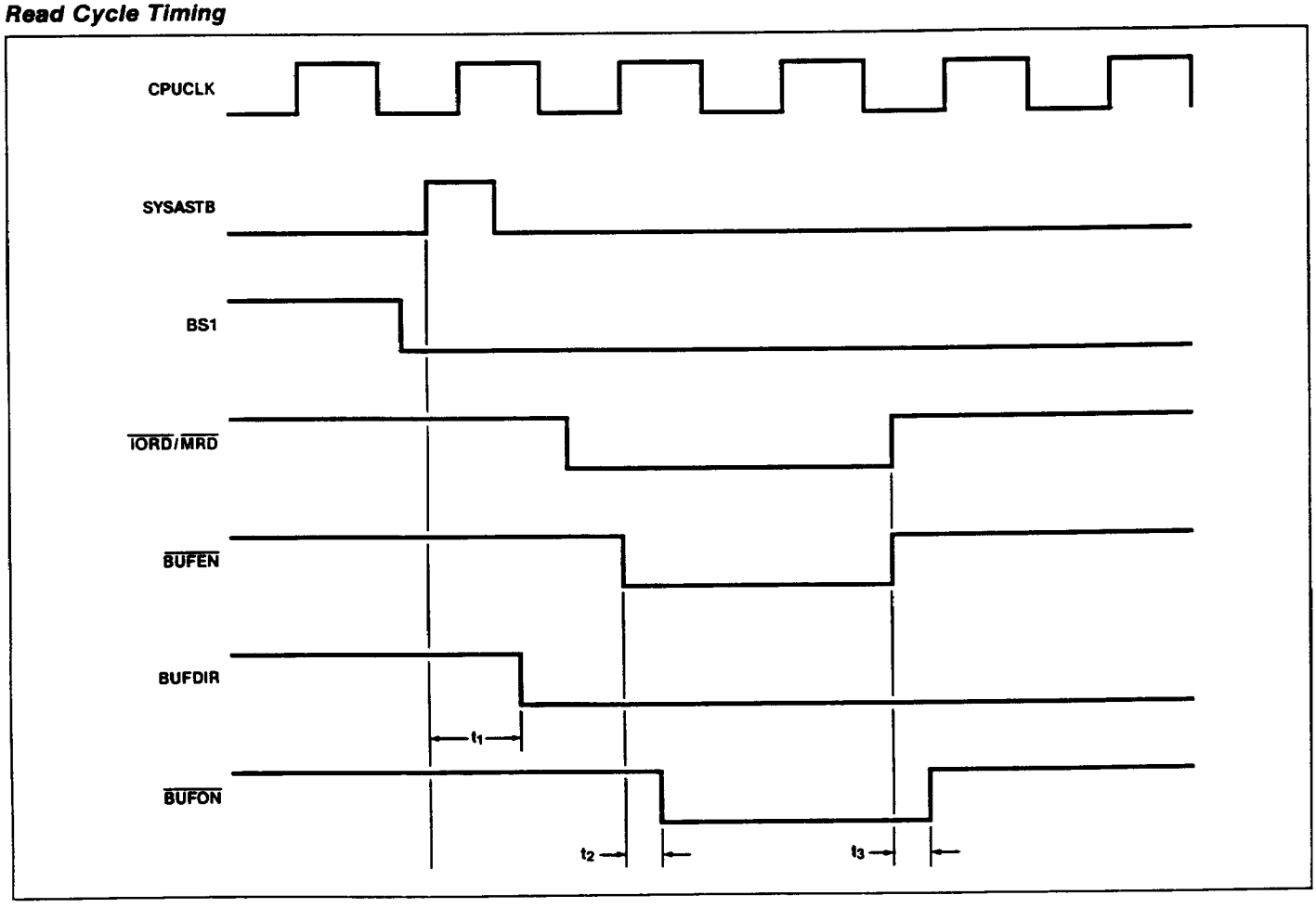
Timing Waveforms

Write Cycle Timing



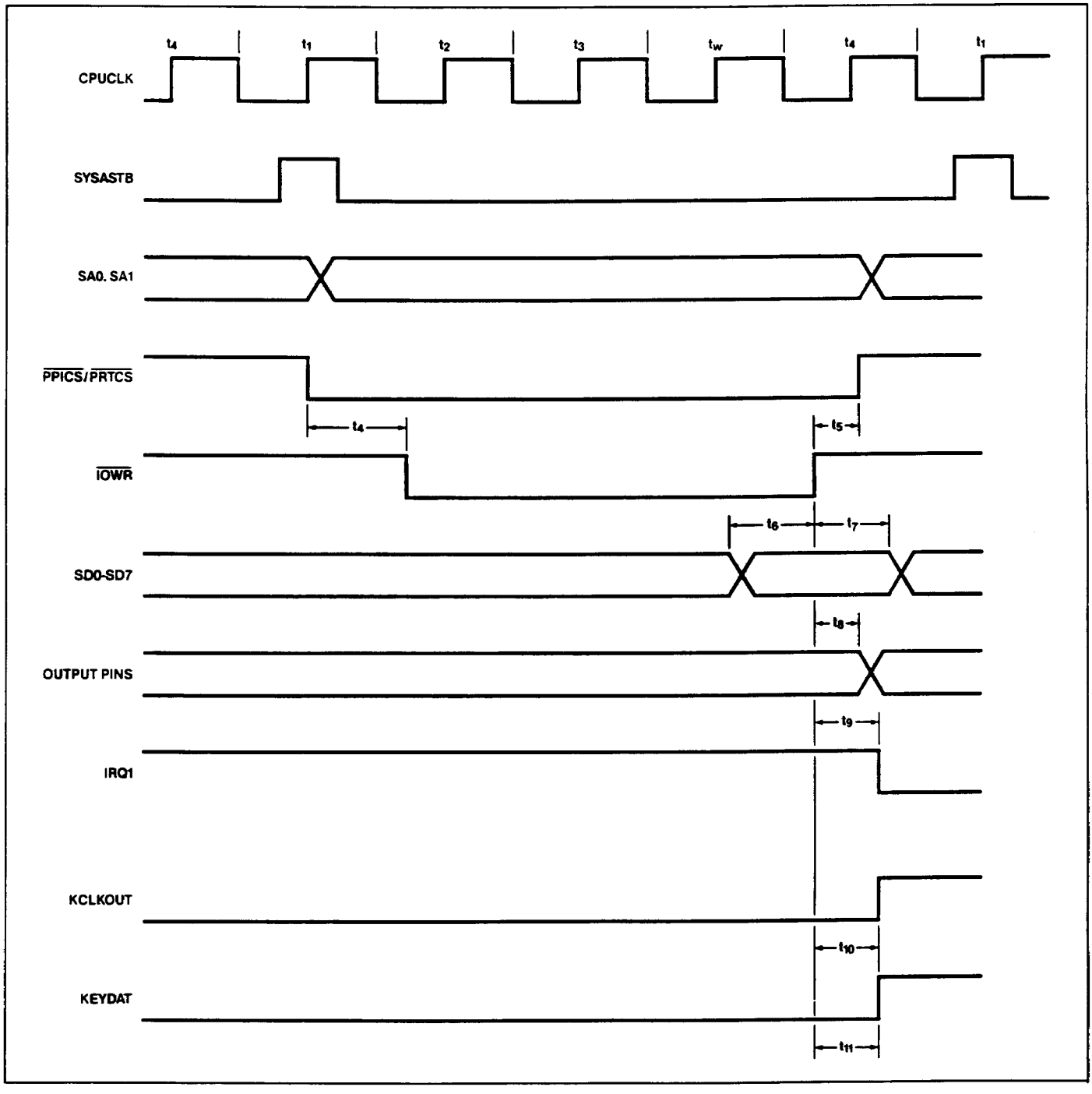
Timing Waveforms (cont)

Read Cycle Timing



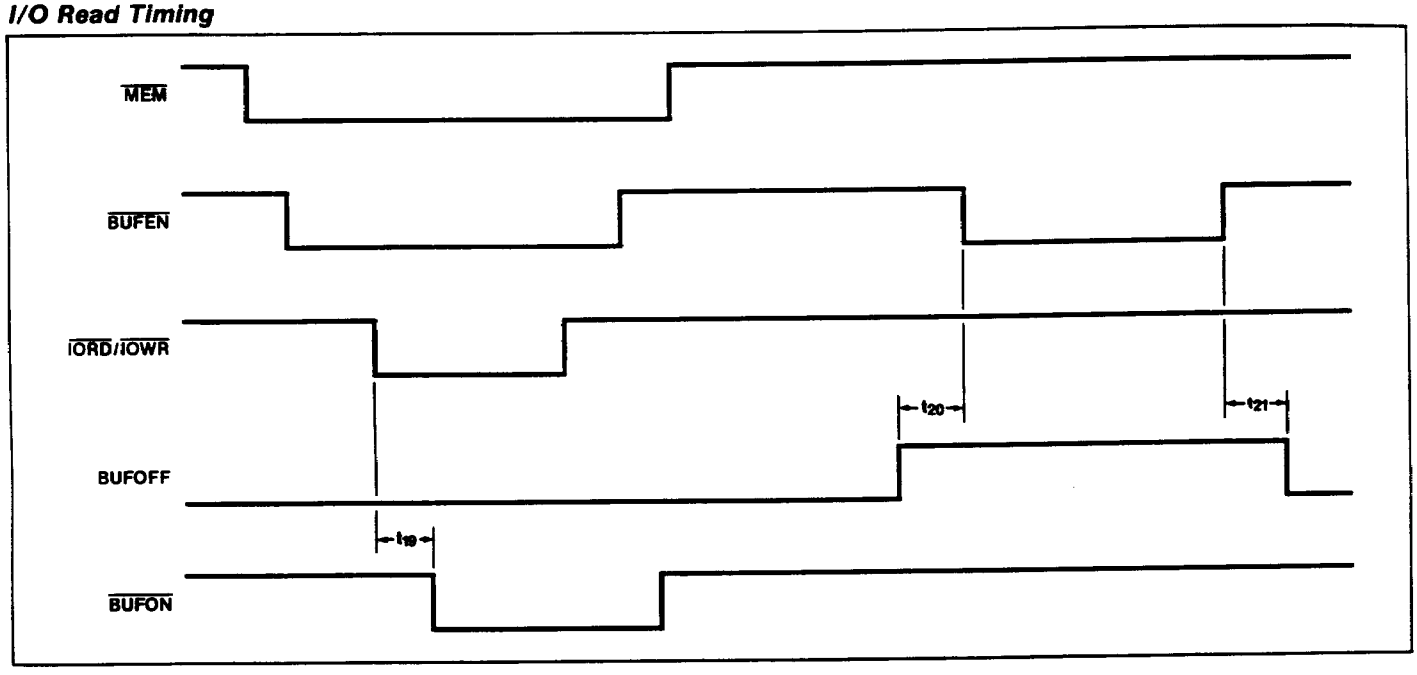
Timing Waveforms (cont)

Outputs from I/O Write

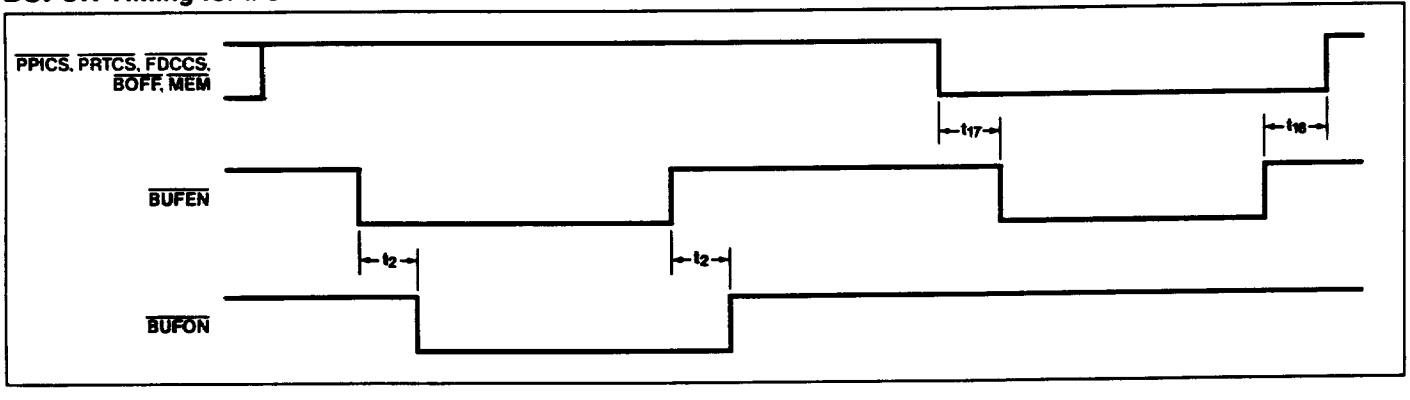


Timing Waveforms (cont)

I/O Read Timing

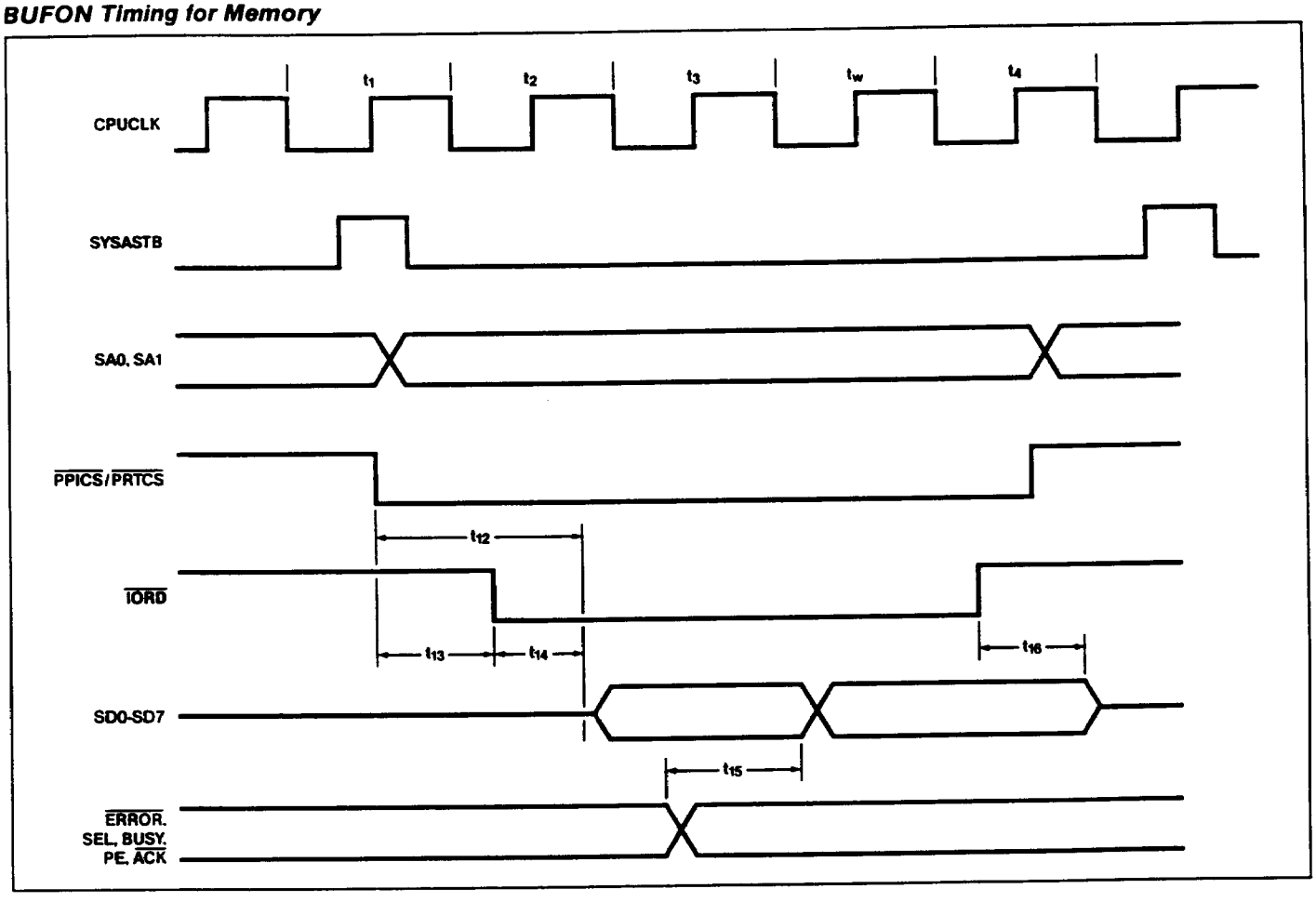


BUFON Timing for I/O



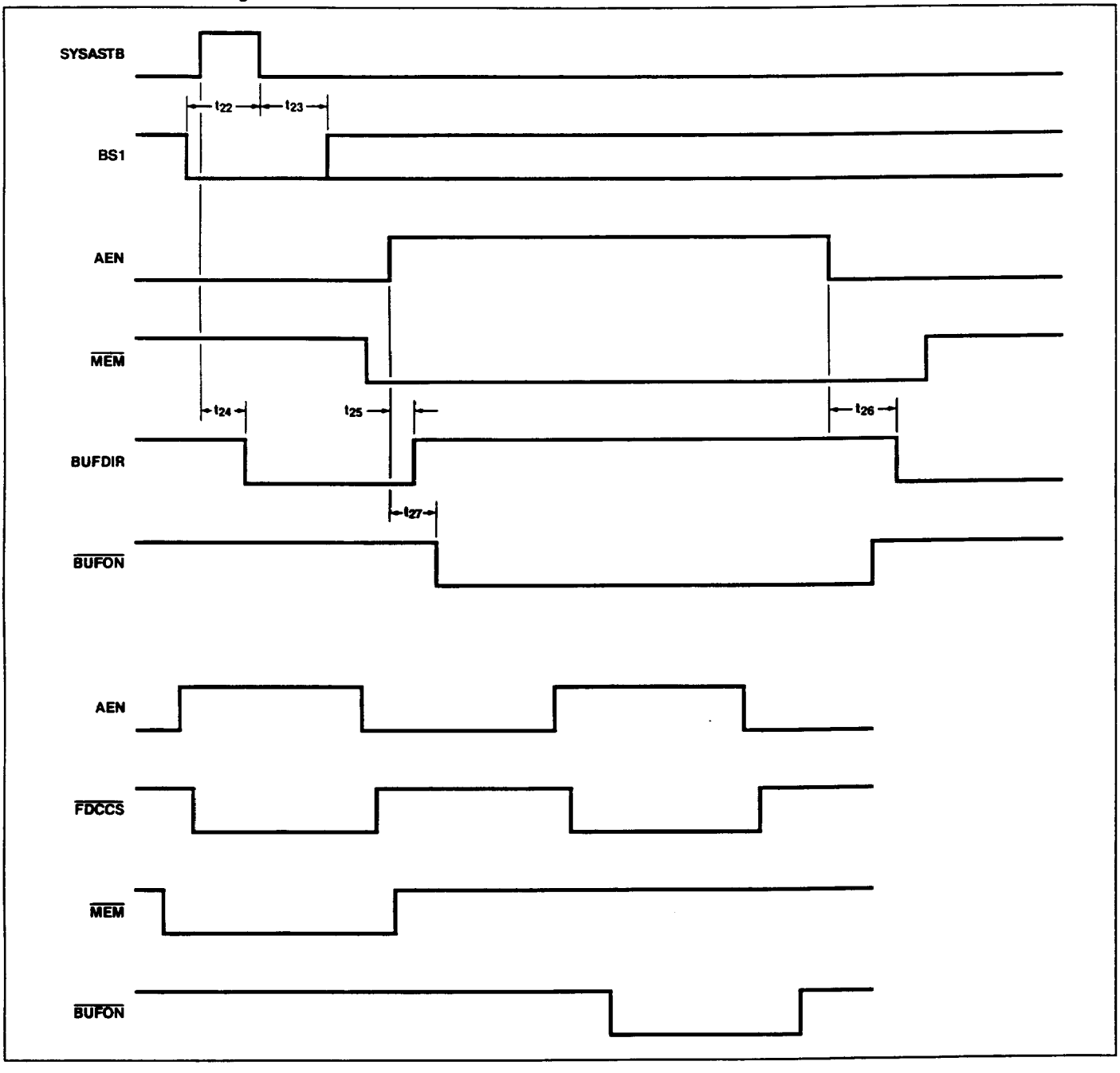
Timing Waveforms (cont)

BUFON Timing for Memory



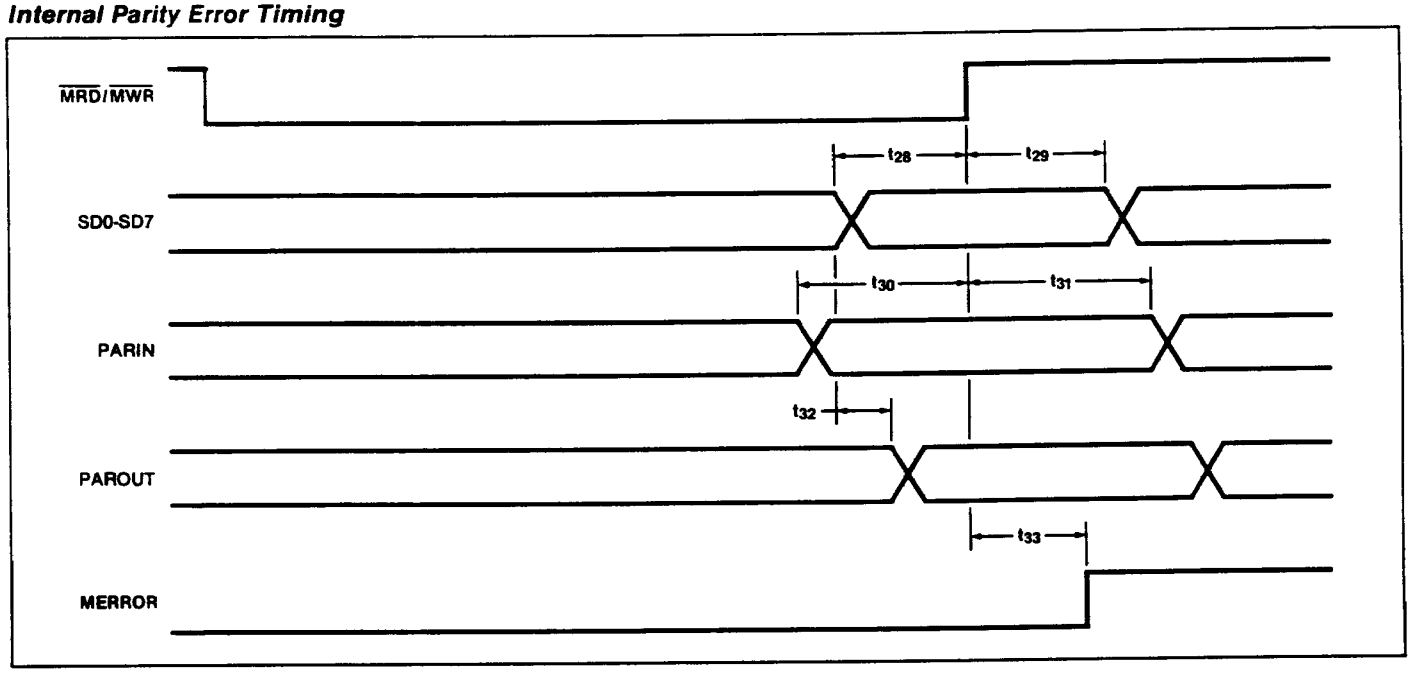
Timing Waveforms (cont)

AEN and FDCCS Timing

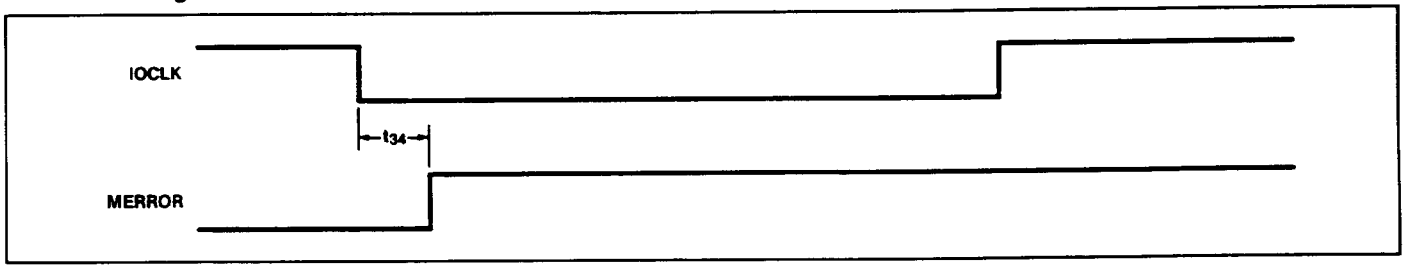


Timing Waveforms (cont)

Internal Parity Error Timing

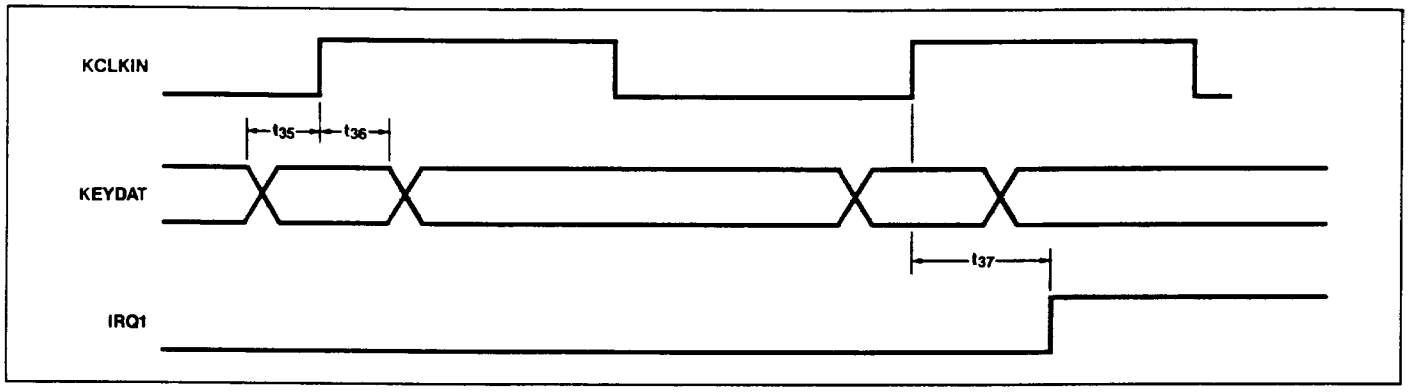


IO CLK Timing

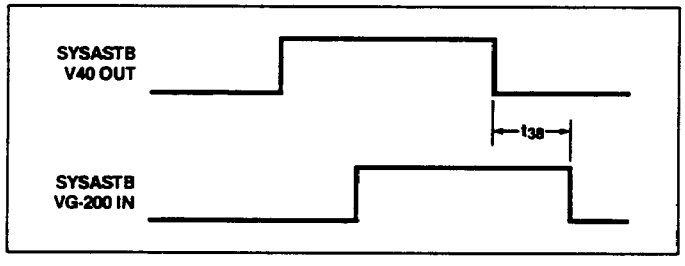


Timing Waveforms (cont)

Keyboard Port Timing



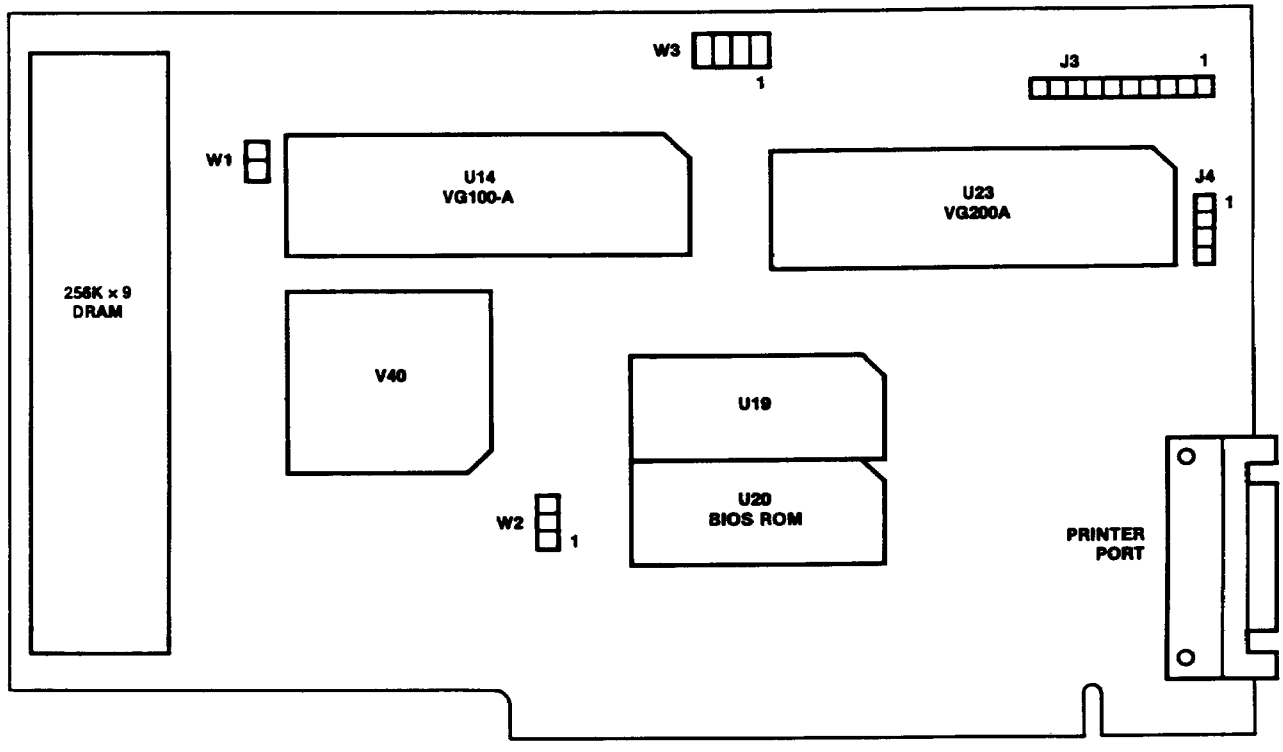
SYSASTB Timing



Applications Information

The following figure is an actual size representation of a fully functional IBM PC-compatible computer, built using the NEC V40 microprocessor and the Vadem VG-100A and VG-200A.

Typical Application



W1
short = printer port at 3BC-3BF
open = printer port at 378-37F

W2
1-2 32K byte EPROM
2-3 128K byte page mode EPROM

J4

1	SIO output
2	N.C.
3	SIO input
4	Ground

W3-1	W3-2	Display Adapter
short	short	reserved (EGA)
open	short	CGA 320 x 200
short	open	CGA 640 x 200
open	open	monochrome 80 x 25

W3-3	W3-4	No. of floppies
short	short	1
open	short	2
short	open	3
open	open	4

J3

1	Speaker
2	Speaker
3	Keyboard clock
4	Keyboard data
5	Reset
6	Ground
7	Vcc
8	External NMI
9	N.C.
10	N.C.

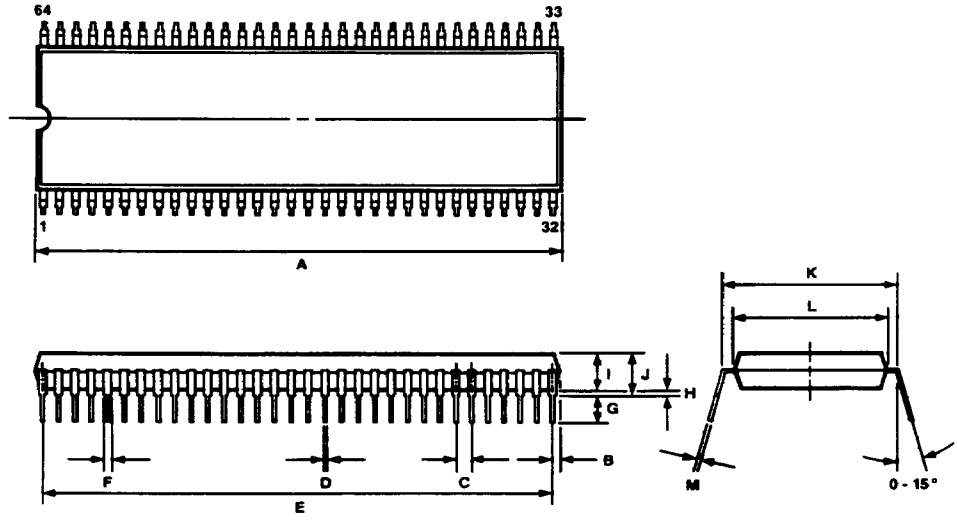
Physical Dimensions

64-Pin Plastic Shrink DIP (750 mil)

Item	Millimeters	Inches
A	58.68 max	2.311 max
B	1.78 max	.07 max
C	1.778 [TP]	.07 [TP]
D	.5 ±.10	.02 $^{+.004}_{-.005}$
E	55.12	2.17
F	.9 min	.035 min
G	3.2 ±.3	.126 ±.012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	19.05 [TP]	.75 [TP]
L	17	.669
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:

1. Each lead centerline is located within .17 mm (.0007 inch) of its true position (TP) at maximum material condition.
2. Item "K" to center of leads when formed parallel.



Notes:

Notice

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VADEM

1885 Lundy Avenue, Suite 201
San Jose, CA 95131 U.S.A.
Telephone (408) 943-9301
Telex: 887-591 (VADEM SNTA UD)
Fax: (408) 943-9735

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