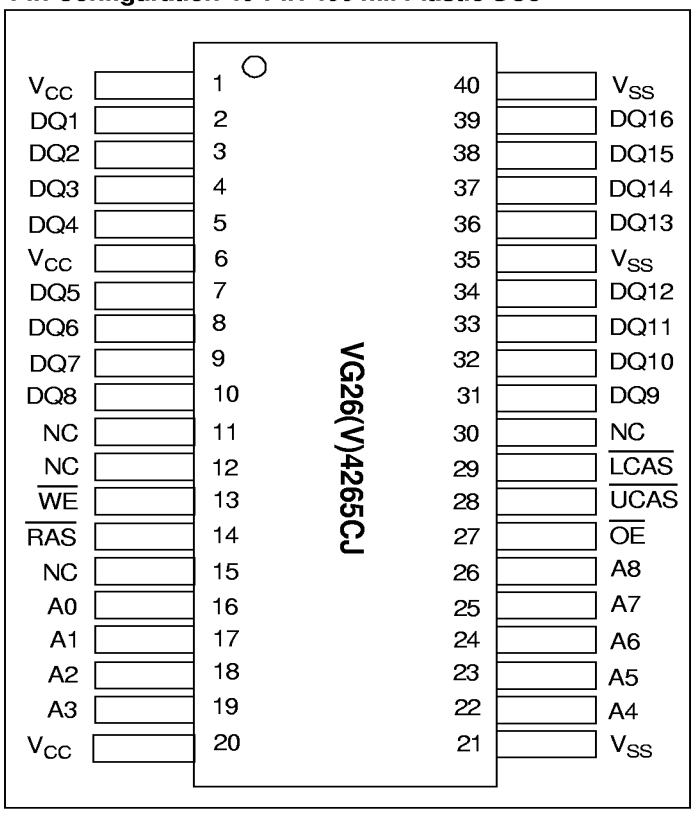
Description

The device is CMOS Dynamic RAM organized as 262,144 words x 16 bits with extended data out access mode. It is fabricated with an advanced submicron CMOS technology and advanced CMOS circuit design technologies. It is packaged in JEDEC standard 40-pin plastic SOJ package.

Features

- Single 5V (±10%) or 3.3V (±10%) power supply
- High speed t_{RAC} access time :
  - 5V: 25/28/30/35/40ns
  - 3.3V: 40/50/60ns
- Low power dissipation
- Extended-data-out (EDO) page mode access
- I/O level: TTL compatible
  - 5V: TTL compatible
  - 3.3V: LVTTL compatible
- 512 refresh cycles in 8 ms
- 2 $\overline{CAS}$ byte control
- 3 refresh modes :
  - $\overline{RAS}$ only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh

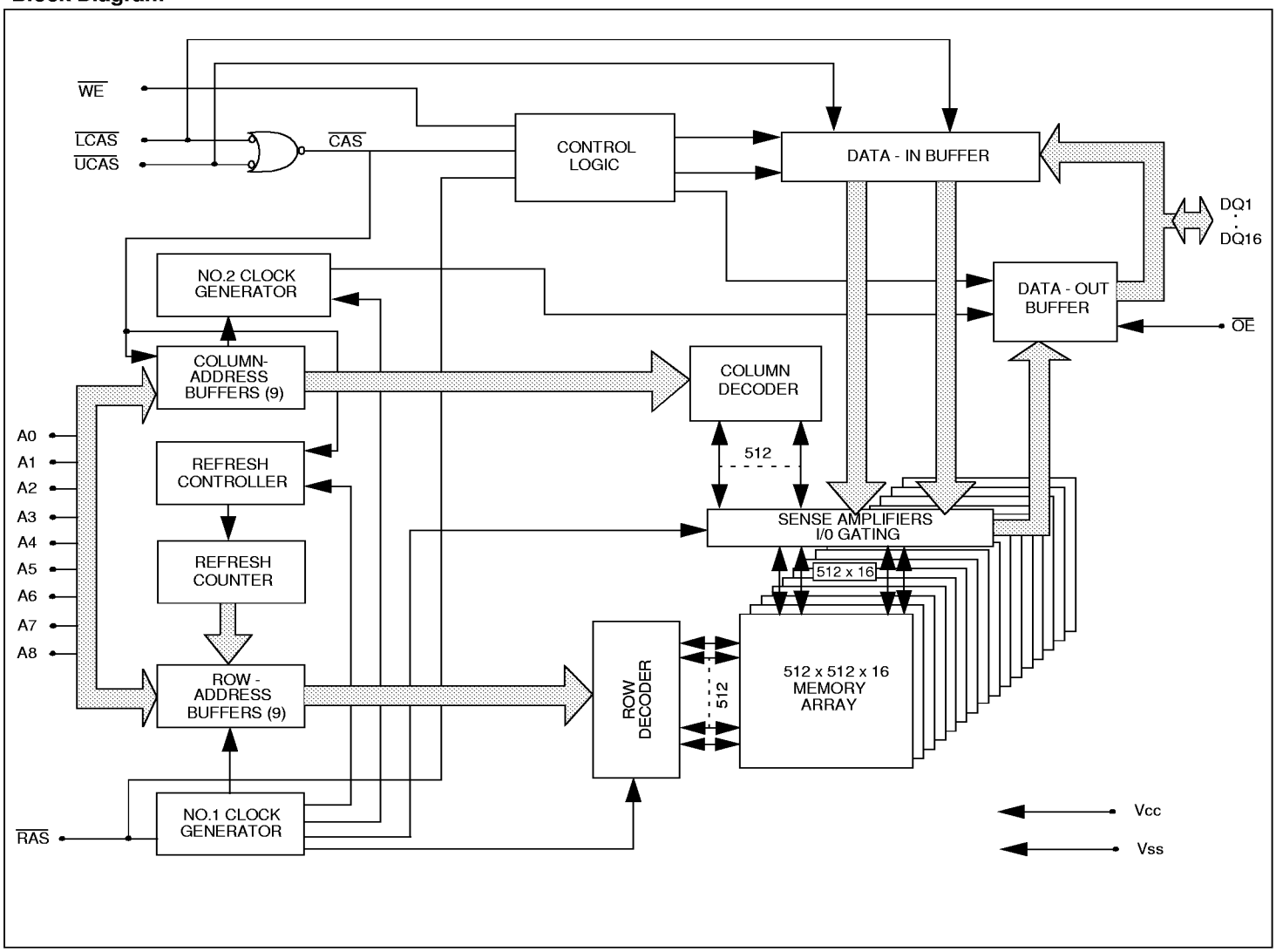
Pin Configuration 40-PIN 400 mil Plastic SOJ



Pin Description

Pin Name	Function
A0 - A8	Address inputs - Row address A0 - A8 - Column address A0 - A8 - Refresh address A0 - A8
DQ1~ DQ16	Data-in/data-out
$\overline{RAS}$	Row address strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{cc}	Power (+5V or +3.3V)
V_{ss}	Ground

Block Diagram



TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ROW	ADDRESSES COL	DQ_S	Notes
STANDBY		H	H → X	H → X	X	X	X	X	High-Z	
READ : WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ : LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte: Data-Out Upper Byte: High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte: High-Z Upper Byte: Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte: Data-In Upper Byte: High-Z	
WRITE : UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte: High-Z Upper Byte: Data-In	
READ WRITE		L	L	L	H → L	L → H	ROW	COL	Data-Out, Data-In	1,2
PAGE-MODE READ	1st Cycle	L	H → L	H → L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H → L	H → L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H → L	H → L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H → L	H → L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H → L	H → L	H → L	L → H	ROW	COL	Data-Out, Data-In	1,2
	2nd Cycle	L	H → L	H → L	H → L	L → H	n/a	COL	Data-Out, Data-In	1,2
HIDDEN REFRESH	READ	L → H → L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L → H → L	L	L	L	X	ROW	COL	Data-In	1,3
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H → L	L	L	H	X	X	X	High-Z	4

Notes: 1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).

2. These READ cycles may also be BYTE READ cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).

3. EARLY WRITE only.

4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{LCAS}$ or $\overline{UCAS}$).

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to Vs.	5V	V_T	- 0.5 to +7.0	V
	3.3V		- 0.5 to +4.6	
Supply voltage relative to Vs.	5V	V_{CC}	- 0.5 to +7.0	V
	3.3V		- 0.5 to +4.6	
Short circuit output current		I_{OUT}	50	mA
Power dissipation		P_D	1.0	W
Operating temperature		T_{OPT}	0 to +70	℃
Storage temperature		T_{STG}	- 55 to +125	℃

Recommended DC Operating Conditions

Parameter/Condition	Symbol	5V Version			3.3V Version			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{cc}	4.5	5.0	5.5	3.0	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.4	-	V_{CC}+0.3	2.0	-	V_{CC}+0.3	V
Input Low Voltage, all inputs	V_{IL}	-1.0	-	0.8	-0.3	-	0.8	V

Capacitance

Ta = 25°C, V_{CC} = 5V±10% or 3V±10 %, f = 1MHz

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{11}	-	5	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WE}$)	C_{I2}	-	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	-	7	pF	1,2

Note : 1. Capacitance measured with effective capacitance measuring method.

2. $\overline{RAS}$, $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH} to disable Dout.

DC Characteristics: 5V Version
(T_a = 0 to 70°C, V_{CC} = + 5V±10%, V_{ss} = 0V)

Parameter	Symbol	Test Conditions	VG264265CJ										Unit	Notes
			-25		-28		-3		-35		-4			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	$\overline{RAS}$ cycling $\overline{LCAS}$,$\overline{UCAS}$ cycling t_{RC} = min.	-	230	-	210	-	200	-	180	-	170	mA	1,2
Standby Current (TTL Interface)	I_{CC2}	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ = V_{IH} Dout = High-Z	-	2	-	2	-	2	-	2	-	2	mA	
Standby current (CMOS Interface)		$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{OE}$ = VCC-0.2V Dout = High-Z	-	1	-	1	-	1	-	1	-	1	mA	
$\overline{RAS}$-only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min.	-	230	-	210	-	200	-	180		170	mA	2
EDO page mode current	I_{CC4}	t_{RC} = min.	-	230	-	210	-	200	-	180		170	mA	1,3
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling	-	230	-	210	-	200	-	180		170	mA	2
Input leakage current	I_{LI}	0V < Vin < Vcc	-10	10	-10	10	-10	10	-10	10	-10	10	µA	
Output leakage current	I_{LO}	0V < Vout < Vcc Dout = Disable	-10	10	-10	10	-10	10	-10	10	-10	10	µA	
Output high voltage	V_{OH}	I_{OH} = -5mA	2.4	-	2.4	-	2.4	-	2.4	-	2.4	-	v	
Output low voltage	V_{OL}	I_{OL} = + 4.2mA	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	v	

Note :

1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.

DC Characteristics: 3.3V Version

(T_a = 0 to + 70°C, V_{cc} = +3.3V±10%, V_{ss} = 0V)

Parameter	Symbol	Test Conditions	VG26V265BJ						Unit	Notes
			-4		-5		-6			
			Min	Max	Min	Max	Min	Max		
Operating current	I_{cc1}	$\overline{RAS}$ cycling $\overline{LCAS}$, $\overline{UCAS}$ cycling t_{RC} = min	-	210	-	180	-	150	mA	1,2
Standby Current (TTL Interface)	I_{cc2}	$\overline{RA S}$, $\overline{LCAS}$, $\overline{UCAS}$ = V_{IH} Dout = High-Z	-	2	-	2	-	2	mA	
Standby current (CMOS Interface)		$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ $\overline{OE}$ = V_{cc}-0.2V Dout = High-z	-	1	-	1	-	1	mA	
$\overline{RAS}$-only refresh current	I_{cc3}	$\overline{RA}$cling, $\overline{CAS}$ = V_{IH} t_{RC} = min.	-	210	-	180	-	150	mA	2
Hyper page mode current	I_{cc4}	t_{PC} = min.	-	210	-	180	-	150	mA	1,3
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{cc5}	t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling	-	210	-	180	-	150	mA	2
Input leakage curent	I_{LI}	OV <V_{in}<V_{cc}	-10	10	-10	10	-10	10	µA	
Output leakage current	I_{LO}	0V <V_{OUT} <V_{CC} D_{OUT} = Disable	-10	10	-10	10	-10	10	µA	
Output high voltage	V_{OH}	I_{OH} = -5mA	2.4	-	2.4	-	2.4	-	V	
Output low Voltage	V_{OL}	I_{OL} = +4.2mA	-	0.4	-	0.4	-	0.4	V	

Note:

1. I_{CC} depends on output load condition when the device is selected. I_{CC}max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.
4. All the V_{CC} pins shall be shanged with the same voltage. And all the V_{SS} pins shall be supplied with the same vvoltage.

AC Characteristics: 5V Version

(Ta = 0 to + 70°C, V_{CC} = 5V±10%, V_{SS} = 0V) * 1, * 2, * 3, * 4, * 5

- Input rise and fal times : 5ns
- Input pulse level : 0~3V
- Input timing reference levels : V_{IL} = 0.8, V_{IH} = 2.4V
- Oututload : one TTL load and 50pF
- Output reference levels : V_{OL} = 0.8V, V_{OH} = 2.0V

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	50	-	55	-	60	-	70	-	80	-	ns	
$\overline{RAS}$ precharge time	t_{RP}	15	-	18	-	20	-	25	-	30	-	ns	
$\overline{LCAS}$/$\overline{UCAS}$ precharge time in normal mode	t_{CPN}	10	-	10	-	10	-	10	-	10	-	ns	22
$\overline{RAS}$ pulse width	t_{RAS}	25	10^5	28	10^5	30	10^5	35	10^5	40	10^5	ns	6
$\overline{LCAS}$/$\overline{UCAS}$ pulse width	t_{CAS}	5	10^5	5	10^5	5	10^5	6	10^5	6	10^5	ns	7
Row address setup time	t_{ASR}	0	-	0	-	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	5	-	5	-	5	-	6	-	6	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	0	-	0	-	0	-	ns	8
Column address hold time	t_{CAH}	5	-	5	-	5	-	6	-	6	-	ns	
$\overline{RAS}$ to $\overline{LCAS}$/$\overline{UCAS}$ delay time	t_{RCD}	11	17	11	19	11	21	12	25	12	29	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	8	13	8	14	8	14	9	17	9	20	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	15	-	16	-	17	-	18	-	20	-	ns	
$\overline{RAS}$ hold time	t_{RSH}	6	-	6	-	6	-	6	-	6	-	ns	
$\overline{LCAS}$/$\overline{UCAS}$ hold time	t_{CSH}	25	-	28	-	30	-	35	-	40	-	ns	
$\overline{LCAS}$/$\overline{UCAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	4	-	4	-	4	-	4	-	4	-	ns	11
$\overline{OE}$ to Din delay time	t_{OED}	6	-	6	-	7	-	7	-	8	-	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	1	50	1	50	ns	12
Refresh period	t_{REF}	-	8	-	8	-	8	-	8	-	8	ns	
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0	-	0	-	0	-	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	-	25	-	28	-	30	-	35	-	40	ns	13
Access time from $\overline{LCAS}$/$\overline{UCAS}$	t_{CAC}	-	8	-	9	-	9	-	10	-	11	ns	14,15
Access time from column address	t_{AA}	-	13	-	14	-	15	-	18	-	20	ns	15,16
Access time from $\overline{OE}$	t_{OEA}	-	8	-	8	-	8	-	9	-	9	ns	
Read command setup time	t_{RCS}	0	-	0	-	0	-	0	-	0	-	ns	8
Read command hold time to $\overline{LCAS}$/$\overline{UCAS}$	t_{RCH}	0	-	0	-	0	-	0	-	0	-	ns	11,17
Read command hold time to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	0	-	0	-	ns	17
Output buffer turn-off time	t_{OFF}	0	6	0	6	0	7	0	7	-	8	ns	18
Output buffer turn-off time from $\overline{OE}$	t_{OEZ}	0	6	0	6	0	7	0	7	-	8	ns	18

Write Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	-	0	-	0	-	0	-	0	-	ns	8,19
Write command hold time	t_{WCH}	5	-	5	-	5	-	6	-	6	-	ns	
Write command pulse width	t_{WP}	5	-	5	-	5	-	6	-	6	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	-	10	-	10	-	10	-	10	-	ns	
Write command to $\overline{LCAS}$/$\overline{UCAS}$ lead time	t_{CWL}	6	-	6	-	6	-	7	-	7	-	ns	20
Data-in setup time	t_{DS}	0	-	0	-	0	-	0	-	0	-	ns	21
Data-in hold time	t_{DH}	4	-	4	-	5	-	6	-	7	-	ns	21
$\overline{WE}$ to Data-in delay	t_{WED}	6	-	6	-	6	-	6	-	7	-	ns	

Read-Modify-Write Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	85	-	90	-	94	-	100	-	110	-	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	43	-	46	-	48	-	53	-	58	-	ns	19
$\overline{LCAS}$/$\overline{UCAS}$ to $\overline{WE}$ dealy time	t_{CWD}	25	-	26	-	27	-	28	-	29	-	ns	19
Column address to $\overline{WE}$ dealy time	t_{AWD}	32	-	33	-	34	-	36	-	38	-	ns	19
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	6	-	6	-	6	-	6	-	7	-	ns	

Refresh Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{LCAS}$/$\overline{UCAS}$ setup time (CBR refrsh)	t_{CSR}	5	-	5	-	5	-	5	-	5	-	ns	
$\overline{LCAS}$/$\overline{UCAS}$ hold time (CBR refrsh)	t_{CHR}	10	-	10	-	10	-	10	-	10	-	ns	11
$\overline{RAS}$ precharge to $\overline{LCAS}$/$\overline{UCAS}$ hold time	t_{RPC}	5	-	5	-	5	-	5	-	5	-	ns	8

EDO Page Mode Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t_{PC}	10	-	11	-	12	-	15	-	16	-	ns	
EDO page mode $\overline{LCAS}/\overline{UCAS}$ precharge time	t_{CP}	4	-	4	-	4	-	5	-	6	-	ns	22
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	25	10^5	28	10^5	30	10^5	35	10^5	40	10^5	ns	23
Access time from $\overline{LCAS}/\overline{UCAS}$ precharge	t_{CPA}	-	17	-	18	-	19	-	22	-	25	ns	11,15
$\overline{RAS}$ hold time from $\overline{LCAS}/\overline{UCAS}$ precharge	t_{CPRH}	25	-	25	-	25	-	25	-	28	-	ns	
$\overline{OE}$ high hold time from $\overline{CAS}$ high	t_{OEHC}	5	-	5	-	5	-	7	-	7	-	ns	
$\overline{OE}$ high pulse width	t_{OEP}	5	-	5	-	5	-	7	-	7	-	ns	
Data output hold after $\overline{CAS}$ low	t_{COH}	3	-	3	-	3	-	3	-	3	-	ns	
Output disable delay from $\overline{WE}$	t_{WHZ}	0	12	0	12	0	13	0	13	0	13	ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ high	t_{WPZ}	7	-	7	-	7	-	7	-	7	-	ns	
$\overline{OE}$ low to $\overline{CAS}$ high setup time	t_{OES}	5	-	5	-	5	-	5	-	5	-	ns	

EDO Page Mode Read Modify Write Cycle

Parameter	Symbol	VG264265CJ										Unit	Notes
		-25		-28		-3		-35		-4			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
EDO page mode read-modify-write cycle $\overline{LCAS}/\overline{UCAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	44	-	44	-	44	-	46	-	46	-	ns	11
EDO page mode read-modify-write cycle time	t_{PRWC}	40	-	43	-	45	-	50	-	56	-	ns	

AC Characteristics: 3.3V Version

(Ta = 0 to +70¢J, V_{CC} = 3.3V± 10%, V_{SS} = 0V)*1, *2, *3, *4, *5

Test conditions

- Input rise and fal times : 5ns
- Input pulse level : 0~3V
- Input timing reference levels : V_{IL} = 0.8, V_{IH} = 2.0V
- Output load : one TTL load and 50pF
- Output reference levels : V_{OL} = 0.8V, V_{OH} = 2.0V

Read, Write, Read - Modify - Write and Refresh Cycles

(Common Parameters)

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	80	-	95	-	110	-	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	-	40	-	50	-	ns	
$\overline{LCAS}$/$\overline{UCAS}$ precharge time in normal mode	t_{CPN}	10	-	10	-	10	-	ns	22
$\overline{RAS}$ pulse width	t_{RAS}	40	10^5	50	10^5	60	10^5	ns	6
$\overline{LCAS}$/$\overline{UCAS}$ pulse width	t_{CAS}	6	10^5	8	10^5	10	10^5	ns	7
Row adress setup time	t_{ASR}	0	-	0	-	0	-	ns	
Row adress hold time	t_{RAH}	6	-	8	-	10	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	0	-	ns	8
Column address hold time	t_{CAH}	6	-	8	-	10	-	ns	
$\overline{RAS}$ to $\overline{LCAS}$/$\overline{UCAS}$ delay time	t_{RCD}	12	29	13	36	14	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	9	20	11	25	12	30	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	20	-	24	-	30	-	ns	
$\overline{RAS}$ hold time	t_{RSH}	6	-	8	-	10	-	ns	
$\overline{LCAS}$/$\overline{UCAS}$ hold time	t_{CSH}	30	-	35	-	40	-	ns	
$\overline{LCAS}$/$\overline{UCAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	4	-	5	-	5	-	ns	11
$\overline{OE}$ to Din delay time	t_{OED}	8	-	8	-	10	-	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	12
Refresh period	t_{REF}	-	8	-	8	-	8	ms	
$\overline{CAS}$ to output in Low - Z	t_{CLZ}	0	-	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	-	40	-	50	-	60	ns	13
Access time from $\overline{LCAS}$/$\overline{UCAS}$	t_{CAC}	-	13	-	14	-	15	ns	14,15
Access time from column/address	t_{AA}	-	20	-	25	-	30	ns	15,16
Access time from $\overline{OE}$	t_{OEA}	-	10	-	12	-	15	ns	
Read command setup time	t_{RCS}	0	-	0	-	0	-	ns	8
Read command hold time to $\overline{LCAS}$/$\overline{UCAS}$	t_{RCH}	0	-	0	-	0	-	ns	11,17
Read command hold time to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	ns	17
Output buffer turn-off time	t_{OFF}	-	8	0	8	0	10	ns	18
Output buffer turn-off time from $\overline{OE}$	t_{OEZ}	-	8	0	8	0	10	ns	18

Write Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	-	0	-	0	-	ns	8,19
Write command hold time	t_{WCH}	6	-	7	-	10	-	ns	
Write command pulse width	t_{WP}	6	-	7	-	10	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	-	12	-	15	-	ns	
Write command to $\overline{LCAS}$/$\overline{UCAS}$ lead time	t_{CWL}	7	-	8	-	10	-	ns	20
Data-in setup time	t_{DS}	0	-	0	-	0	-	ns	21
Data-in hold time	t_{DH}	7	-	8	-	10	-	ns	21
$\overline{WE}$ to Data-in delay	t_{WED}	7	-	8	-	8	-	ns	

Read - Modify - Write Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	110	-	126	-	140	-	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	58	-	68	-	77	-	ns	19
$\overline{LCAS}$/$\overline{UCAS}$ to $\overline{WE}$ dealy time	t_{CWD}	29	-	30	-	32	-	ns	19
Column address to $\overline{WE}$ dealy time	t_{AWD}	38	-	43	-	47	-	ns	19
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	7	-	8	-	10	-	ns	

Refresh Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
$\overline{LCAS}$/$\overline{UCAS}$ setup time (CBR refresh)	t_{CSR}	5	-	5	-	5	-	ns	
$\overline{LCAS}$/$\overline{UCAS}$ hold time (CBR refresh)	t_{CHR}	10	-	10	-	10	-	ns	11
$\overline{RAS}$ precharge to $\overline{LCAS}$/$\overline{UCAS}$ hold time	t_{RPC}	5	-	5	-	5	-	ns	8

EDO Page Mode Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t_{PC}	16	-	20	-	25	-	ns	
EDO page mode $\overline{LCAS}/\overline{UCAS}$ precharge time	t_{CP}	6	-	8	-	10	-	ns	22
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	40	10^5	50	10^5	60	10^5	ns	23
Access time from $\overline{LCAS}/\overline{UCAS}$ precharge	t_{CPA}	-	25	-	30	-	35	ns	11,15
$\overline{RAS}$ hold time from $\overline{LCAS}/\overline{UCAS}$ pre-charge	t_{CPRH}	28	-	30	-	35	-	ns	
$\overline{OE}$ high hold time from $\overline{CAS}$ high	t_{OEHC}	7	-	8	-	10	-	ns	
$\overline{OE}$ high pulse width	t_{OEP}	7	-	7	-	10	-	ns	
Data output hold after $\overline{CAS}$ low	t_{COH}	3	-	3	-	3	-	ns	
Output disable delay from $\overline{WE}$	t_{WHZ}	0	13	0	13	0	13	ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ high	t_{WPZ}	7	-	7	-	7	-	ns	
$\overline{OE}$ low to $\overline{CAS}$ high setup time	t_{OES}	5	-	5	-	5	-	ns	

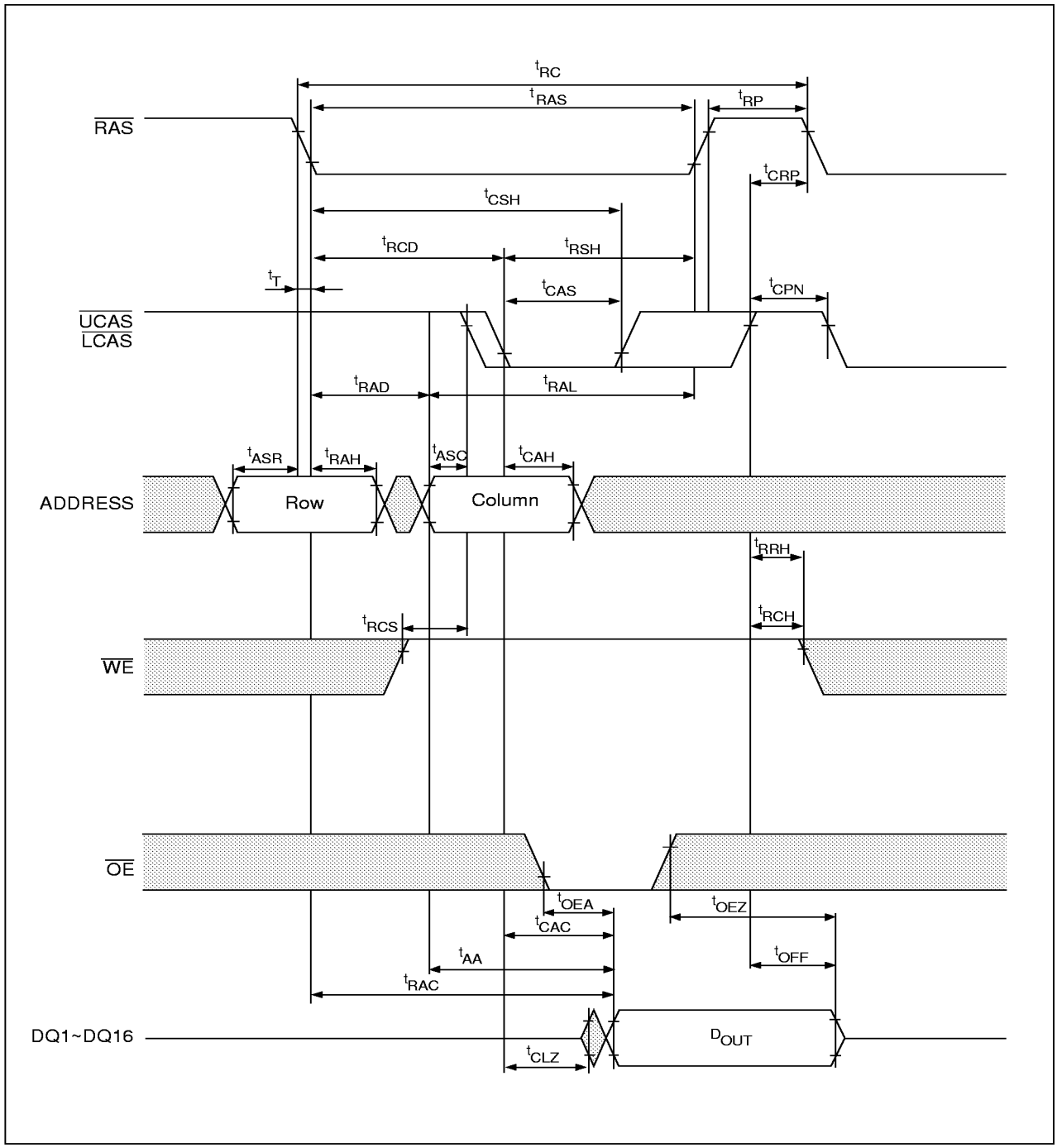
EDO Page Mode Read Modify Write Cycle

Parameter	Symbol	VG26V4265CJ						Unit	Notes
		-4		-5		-6			
		Min	Max	Min	Max	Min	Max		
EDO page mode read-modify-write cycle $\overline{LCAS}$ / $\overline{UCAS}$ precharge to $\overline{WE}$ delaycle time	t_{CPW}	46	-	48	-	55	-	ns	11
EDO page mode read-modify-write cycle time	t_{PRWC}	56	-	64	-	66	-	ns	

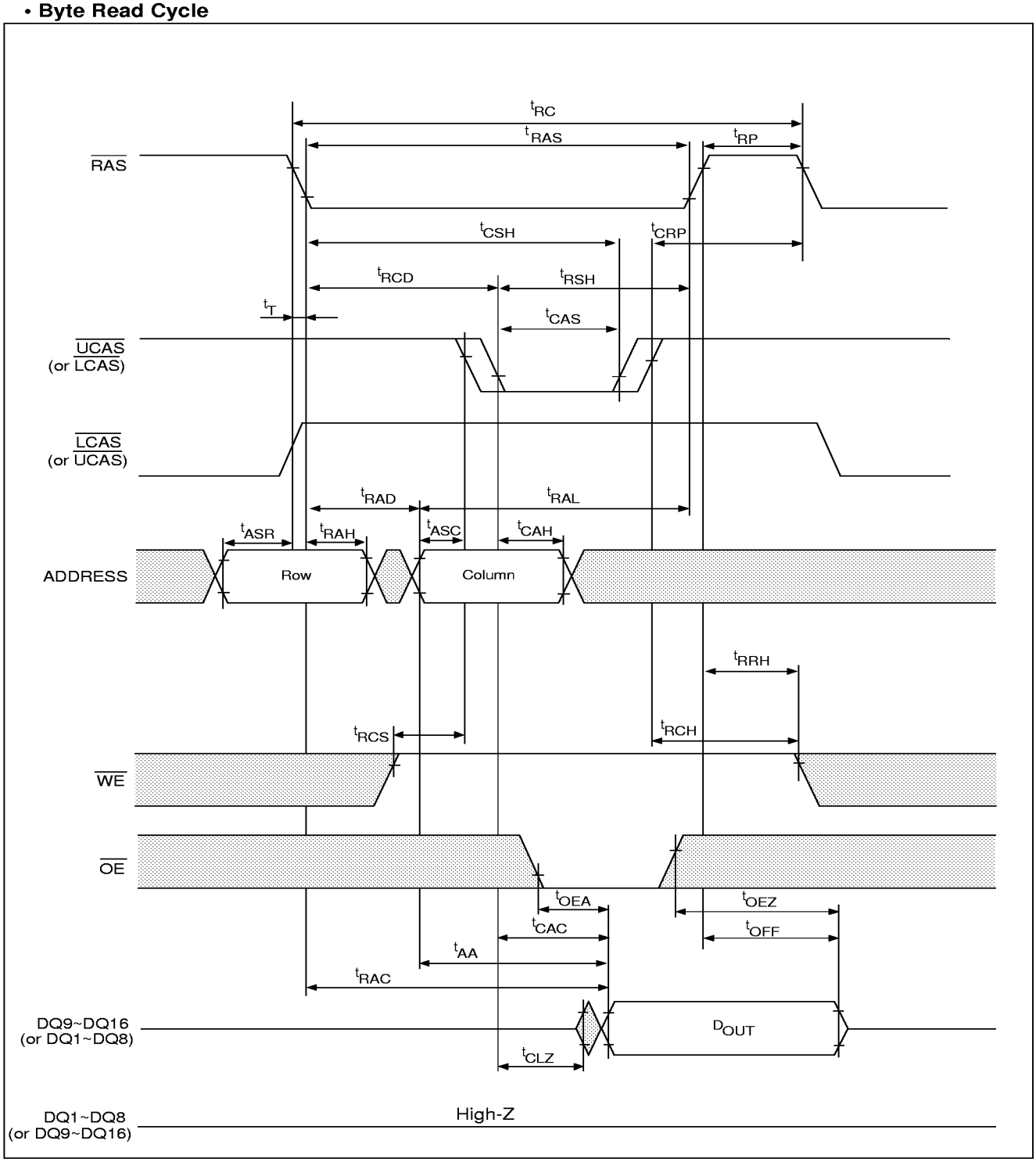
Notes :

1. AC measurements assume t_T = 5ns.
2. An initial pause of 100 µS is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycles or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
3. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
4. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16-bits data are witten into the device. $\overline{LCAS}$ and $\overline{UCAS}$ cannot be staggered within the same write/read cycles.
5. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
6. $t_{RAS}(min) = t_{RWD}(min) + t_{RWL}(min) + t_T$ in read-modify-write cycle.
7. $t_{CAS}(min) = t_{CWD}(min) + t_{CWL}(min) + t_T$ in read-modify-write cycle.
8. $t_{ASC}(min)$, $t_{RCS}(min)$, $t_{WCS}(min)$ and t_{RPC} are determined by the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$.
9. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a refer ence point only, if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
10. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a refer- ence point only, if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
11. t_{CRP}, t_{CHR}, t_{RCH}, t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{LCAS}$ or $\overline{UCAS}$.
12. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing or input signals. Also, transition times are measured between V_{IH} and V_{IL}.
13. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
14. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
15. Access time is determined by the longer of t_{AA}, t_{CAC} and t_{CPA}. t_{CAC} is guaranteed for one TTL and 50pF load.
16. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
17. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
18. $t_{OFF}(max)$ and $t_{OEZ}(max)$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. t_{OFF} is determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.
19. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
20. t_{CWL} shall be satisfied by both $\overline{LCAS}$ and $\overline{UCAS}$.
21. These parameters are referenced to $\overline{LCAS}$ or $\overline{UCAS}$ separately in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
22. t_{CPN} and t_{CP} are determined by the time that both $\overline{LCAS}$ and $\overline{UCAS}$ are high.
23. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.

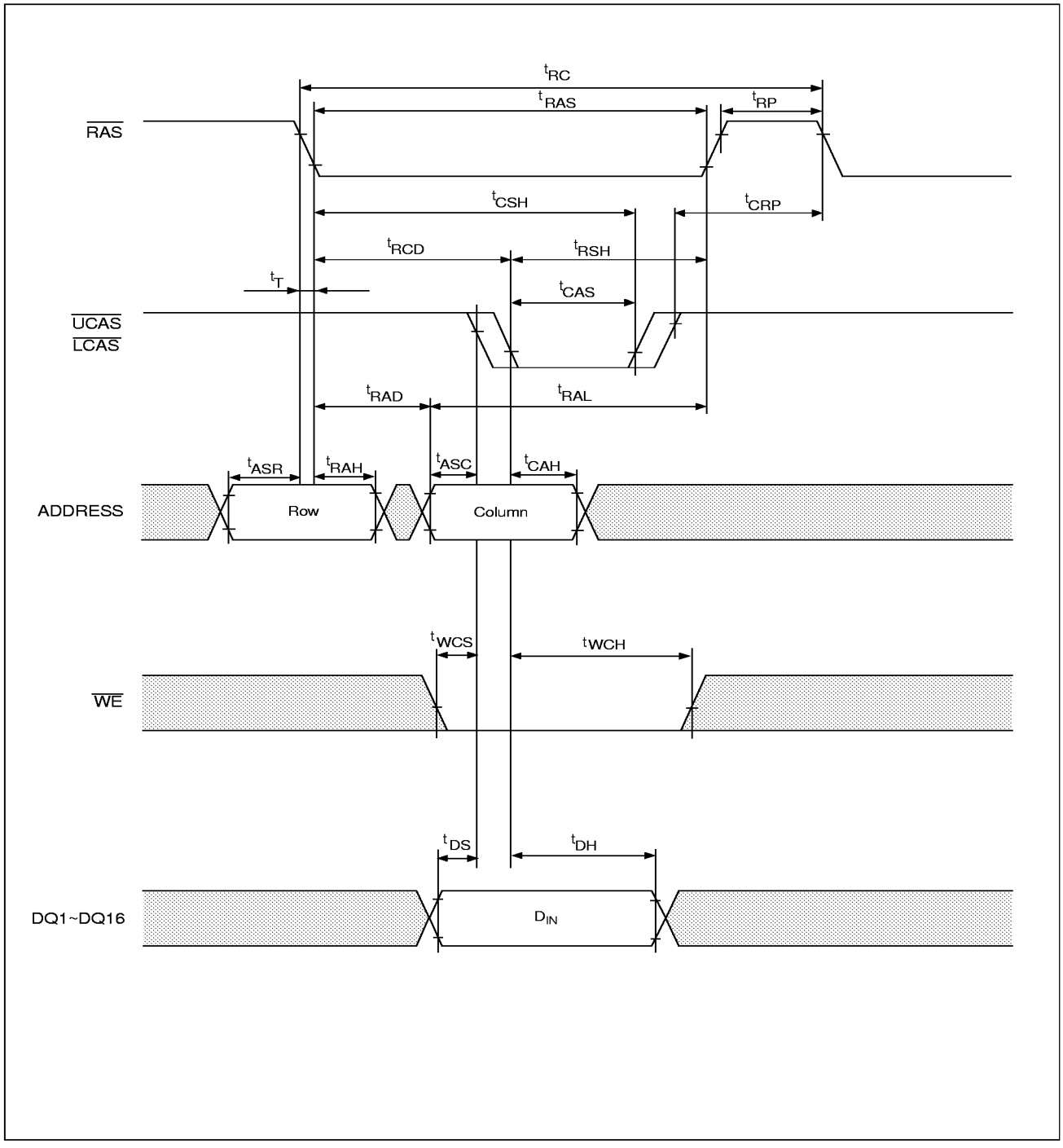
Timing Waveforms
• Word Read Cycle



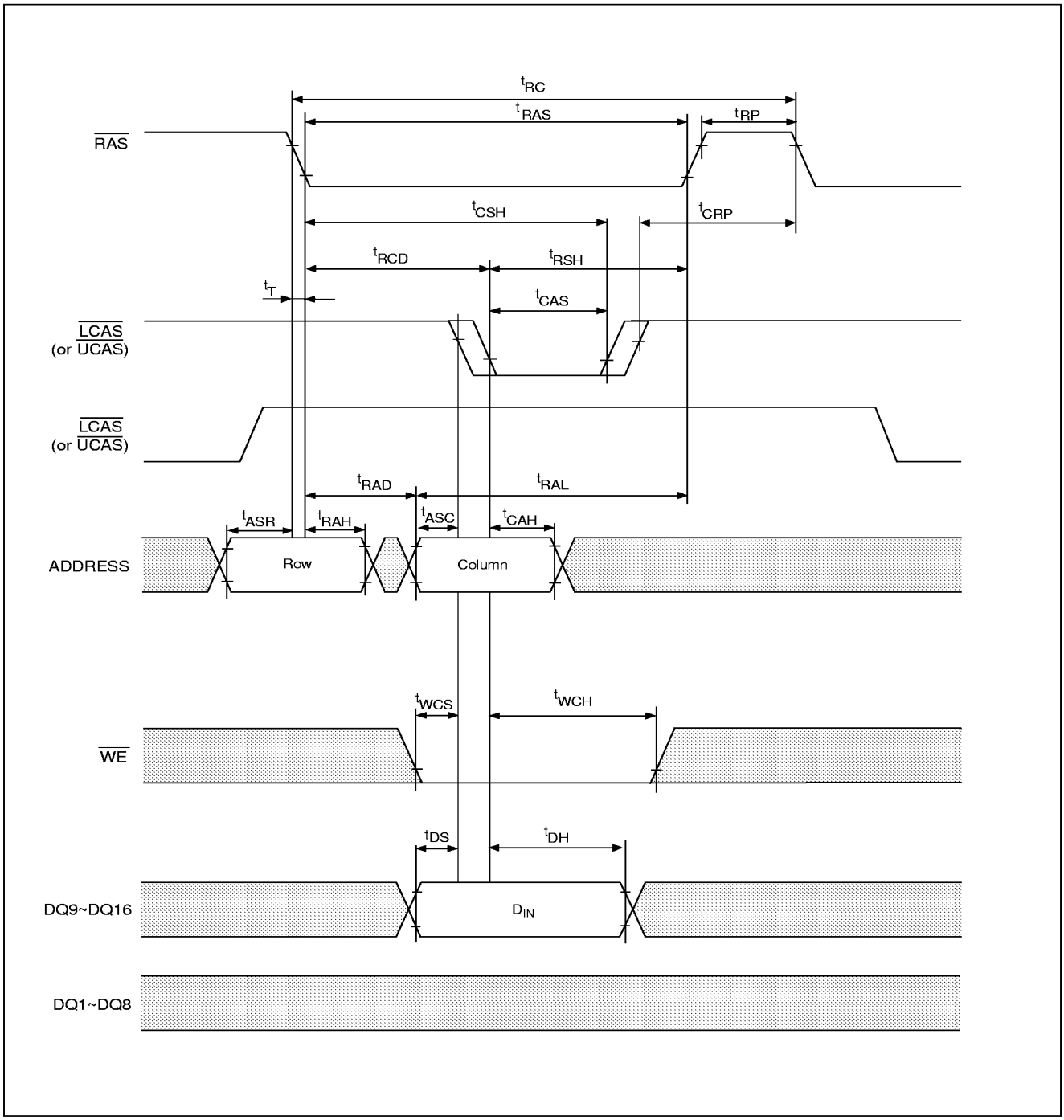
• **Byte Read Cycle**



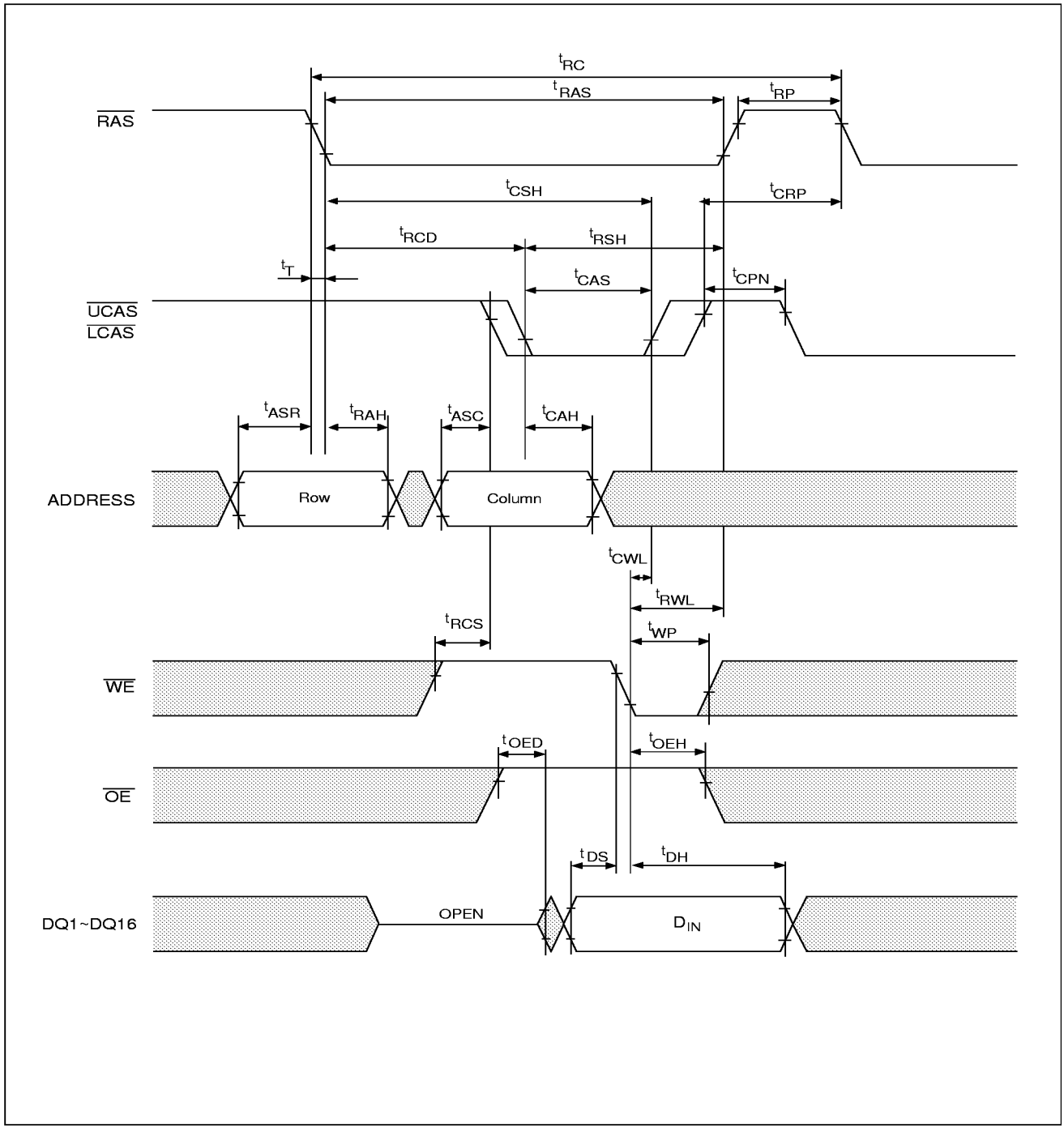
• **Word Early Write Cycle**



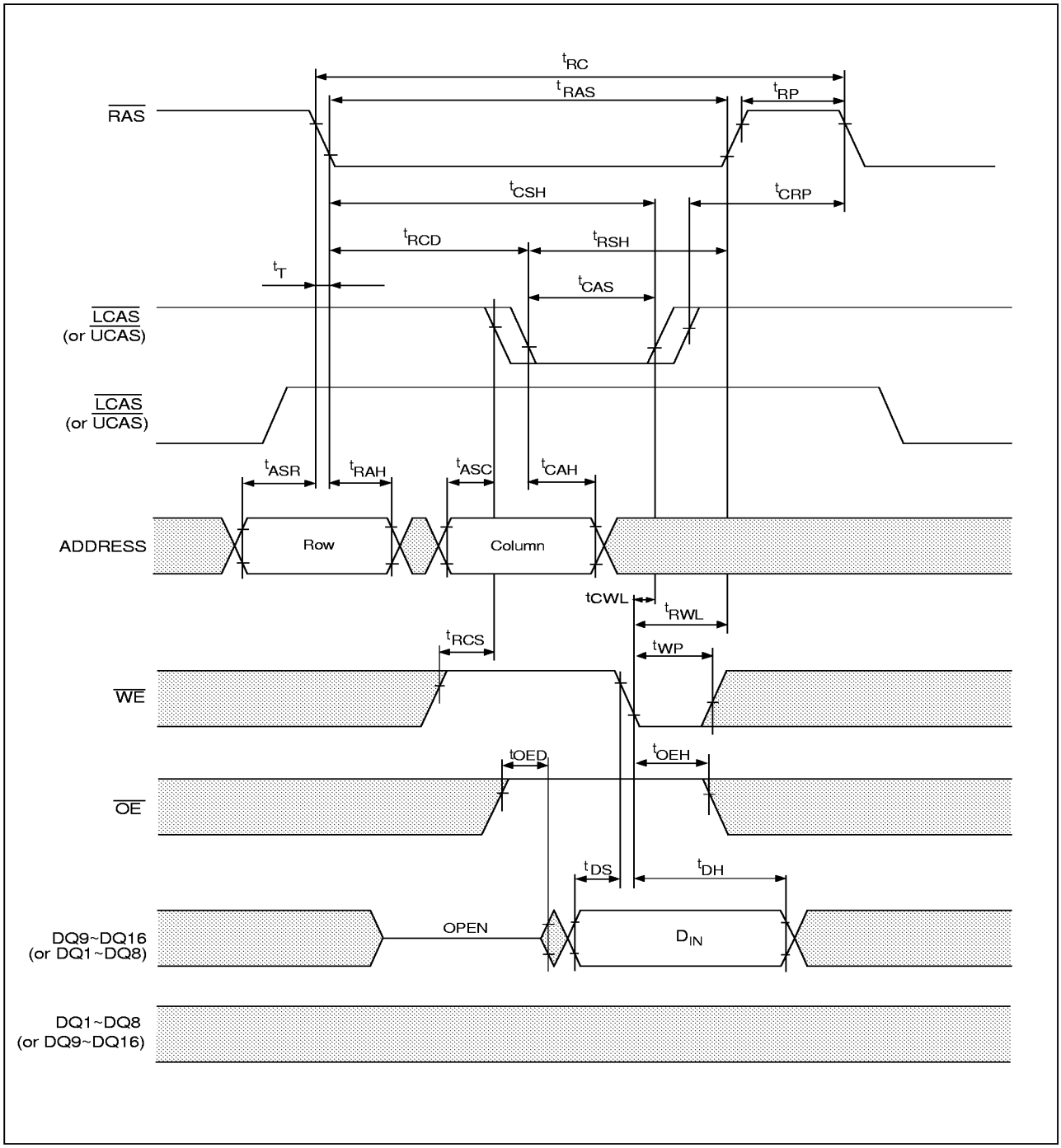
• **Byte Early Write Cycle**



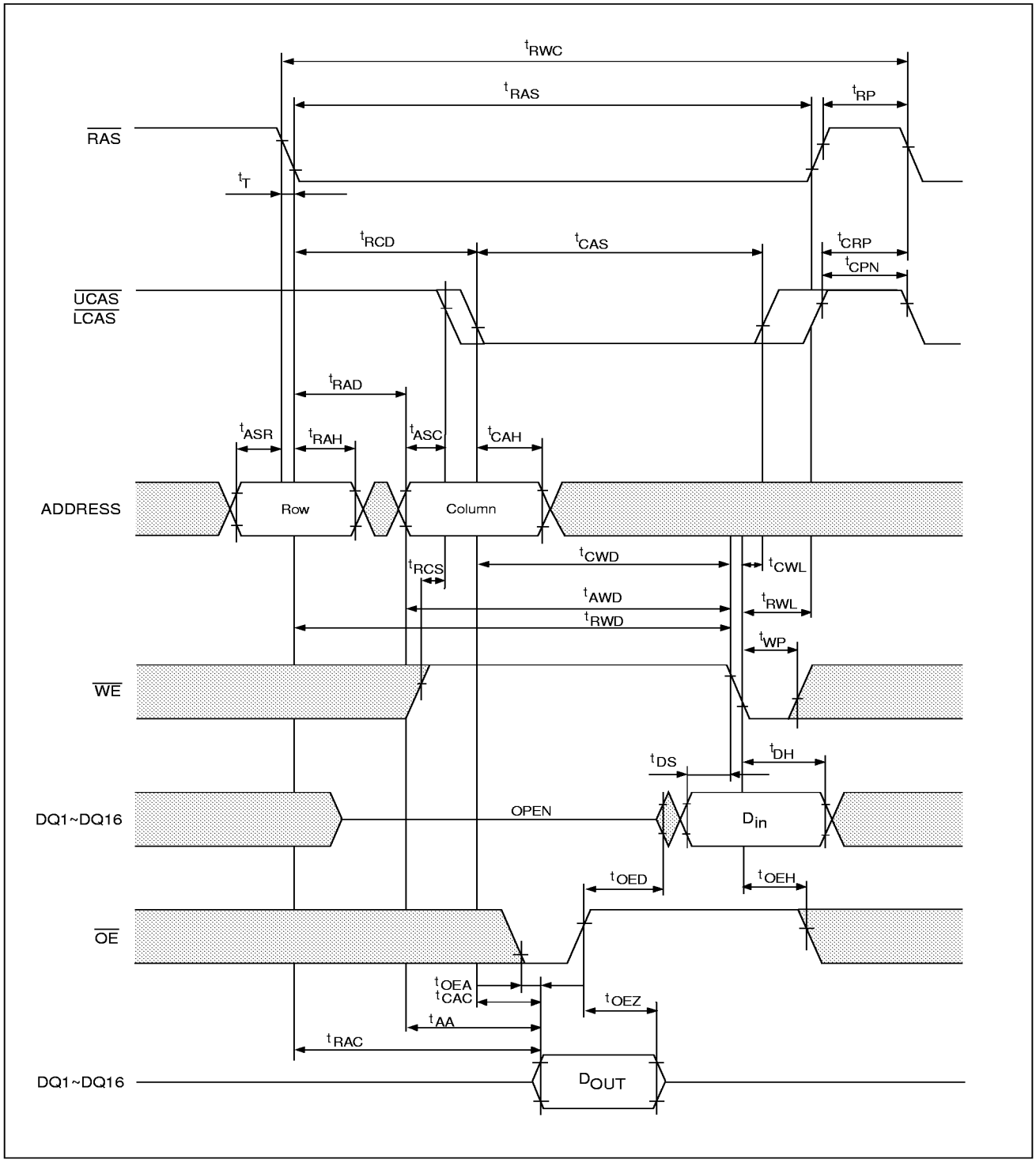
• **Word Delayed Write Cycle**



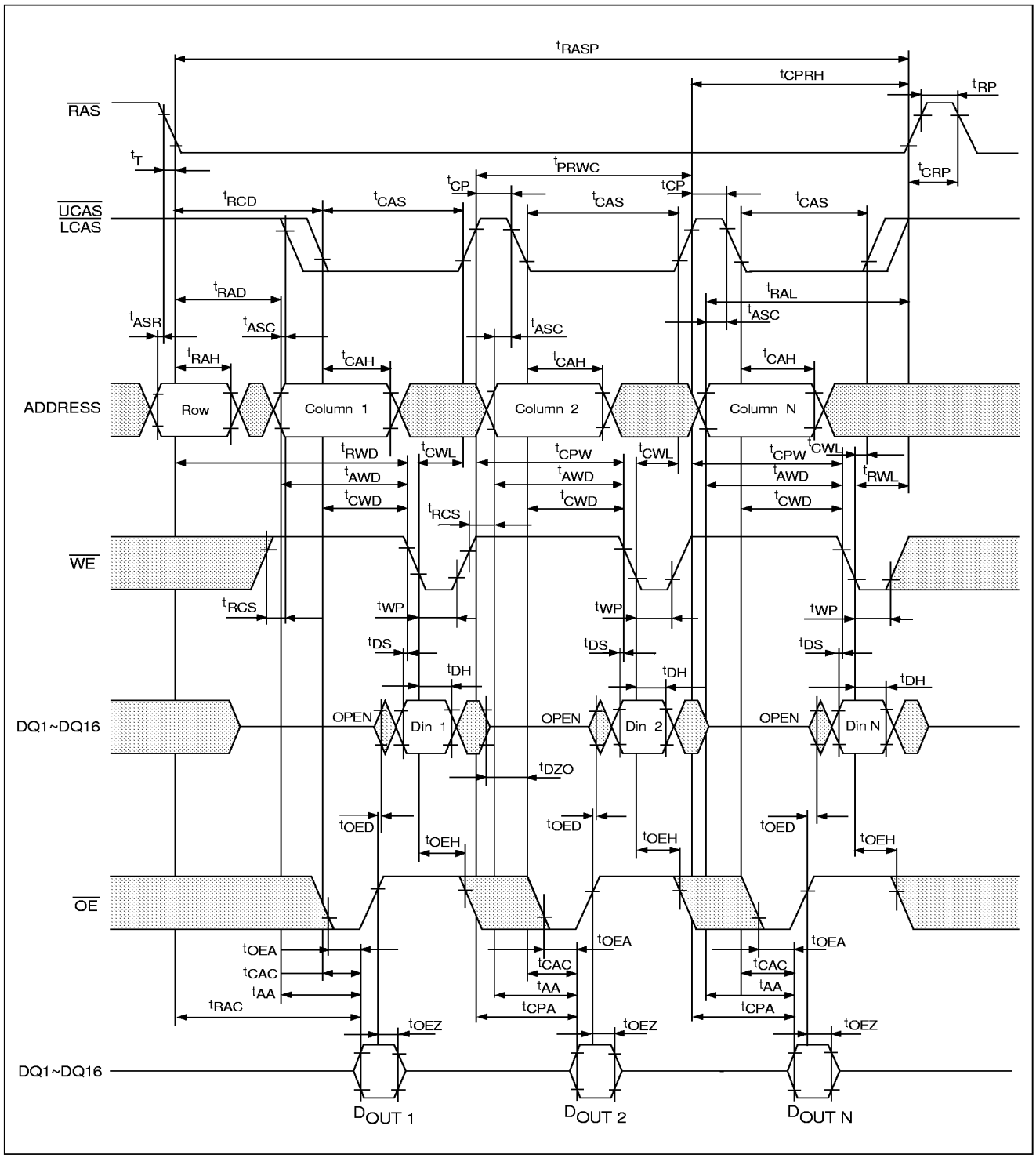
• **Byte Delayed Write Cycle**



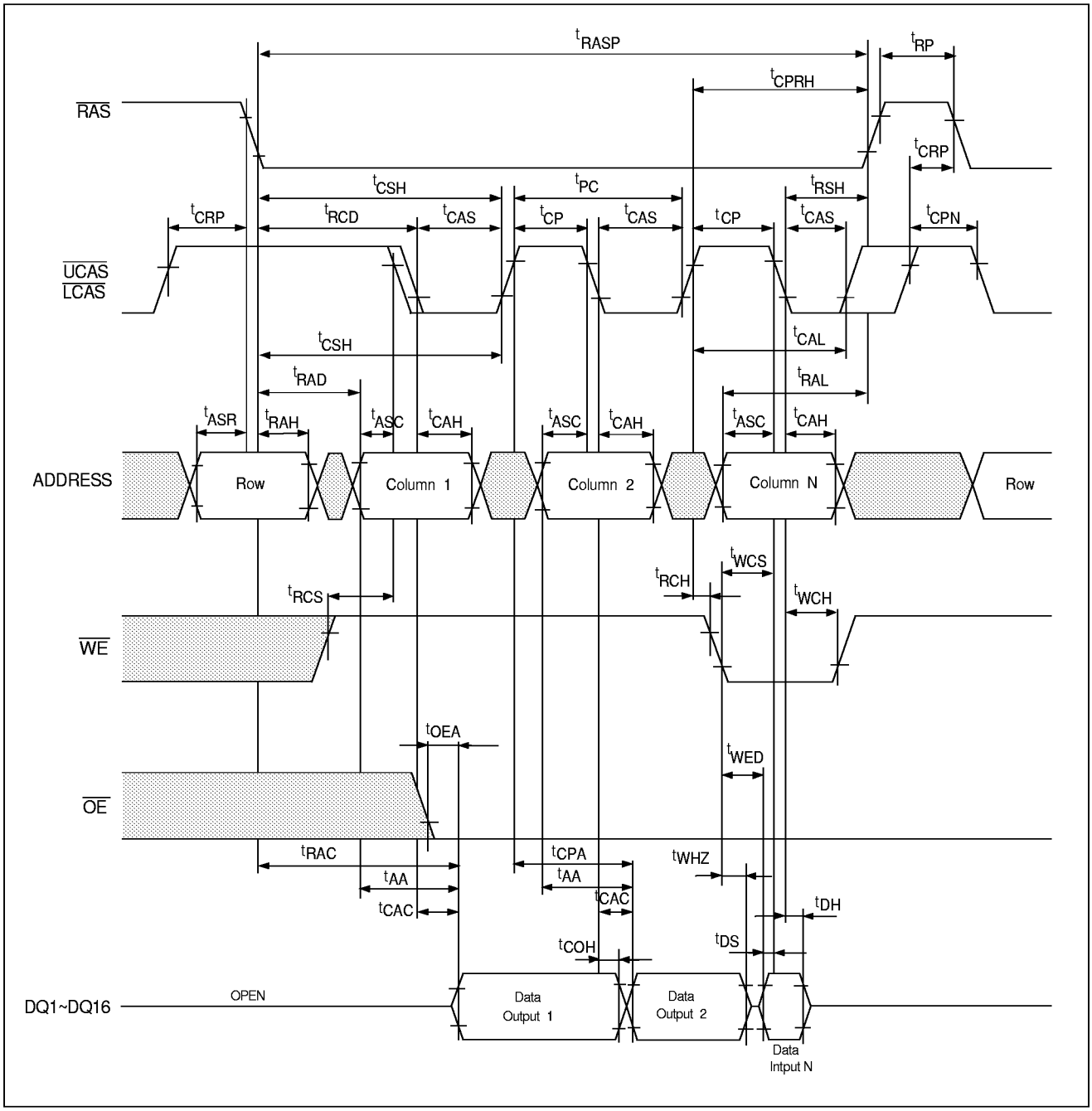
• **Word Read-Modify-Write Cycle**



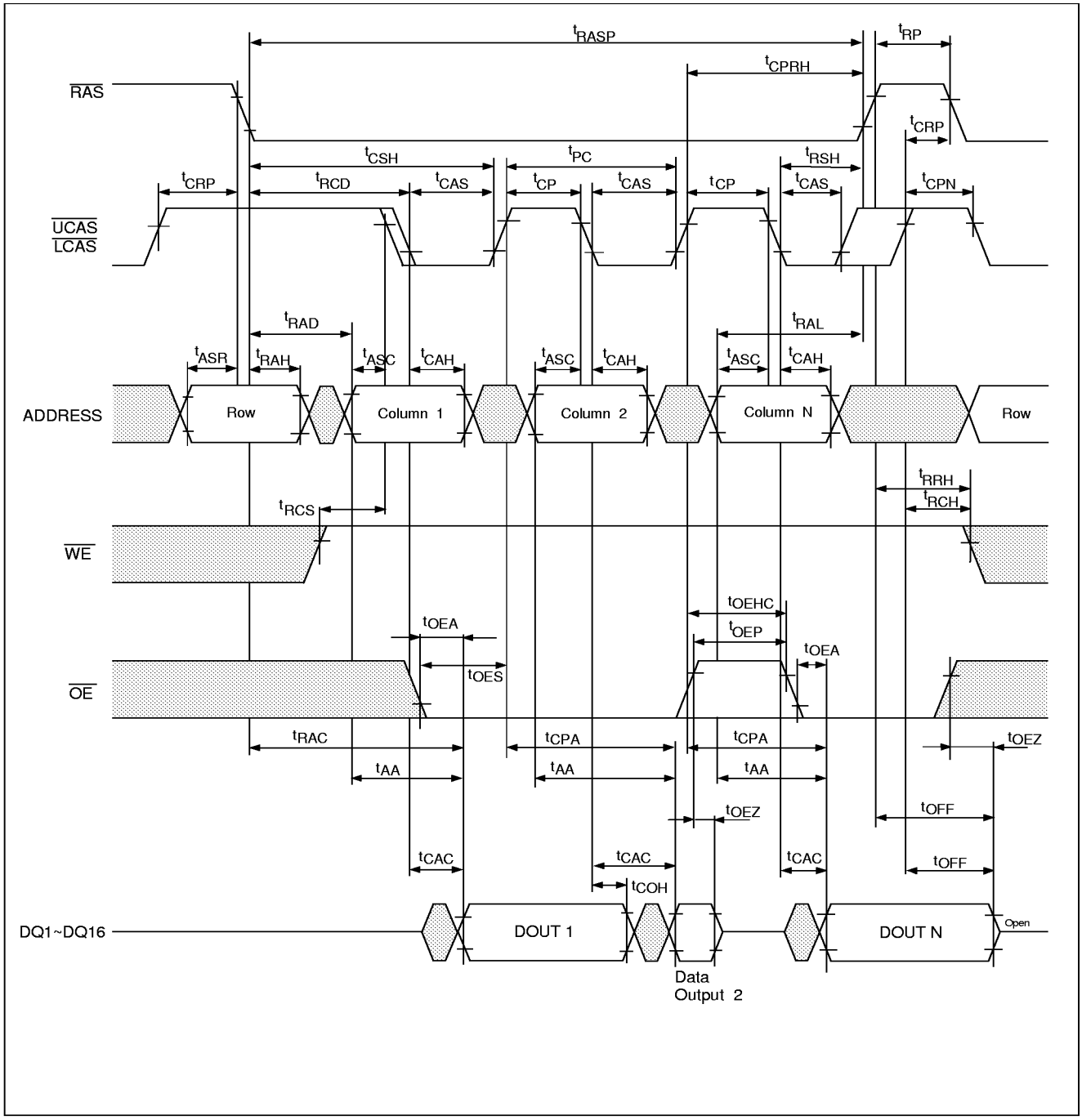
• **EDO Page Mode Word Read-Modify-Write Cycle**



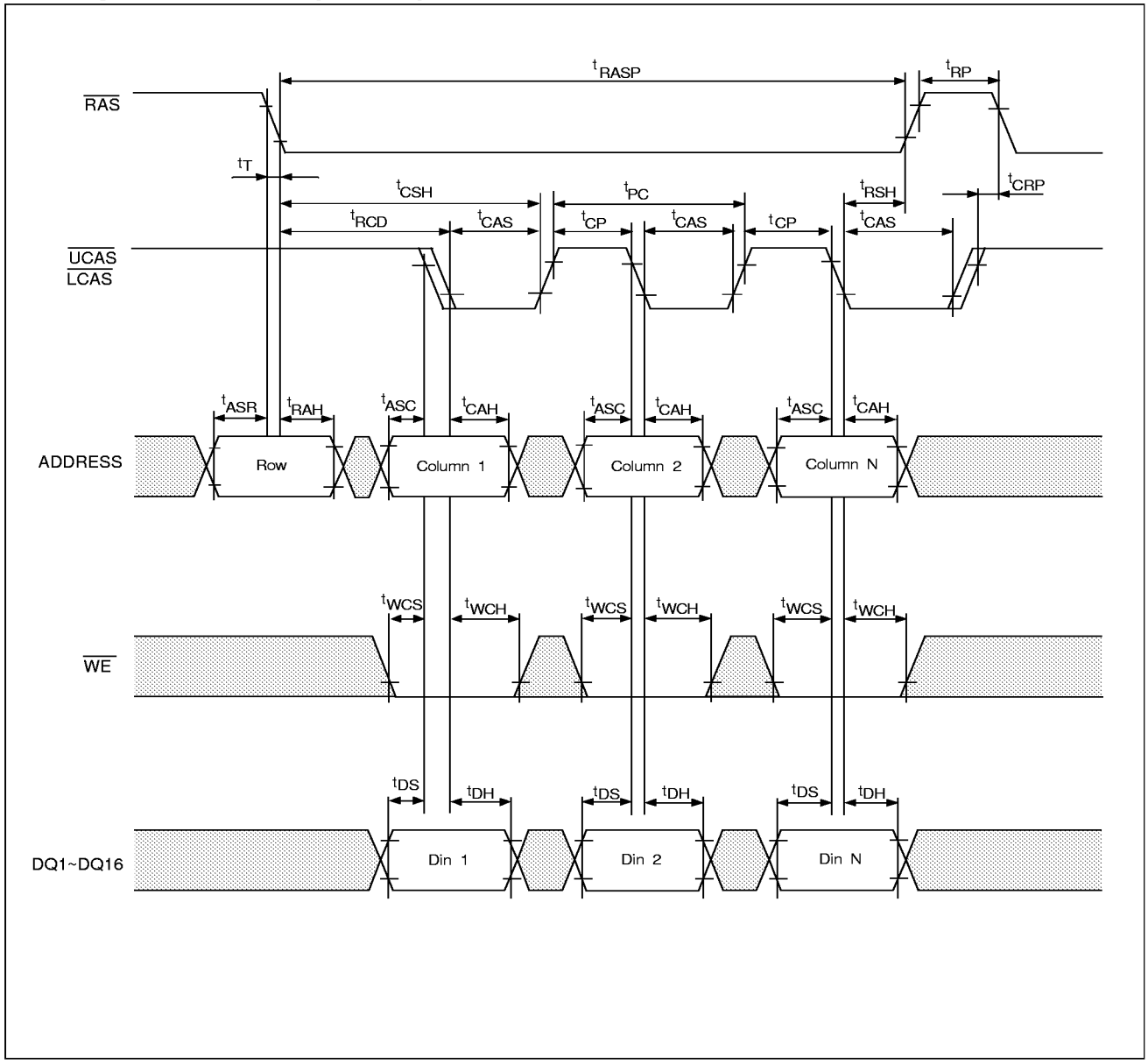
• **EDO Page Mode Word Read-Early-Write Cycle**



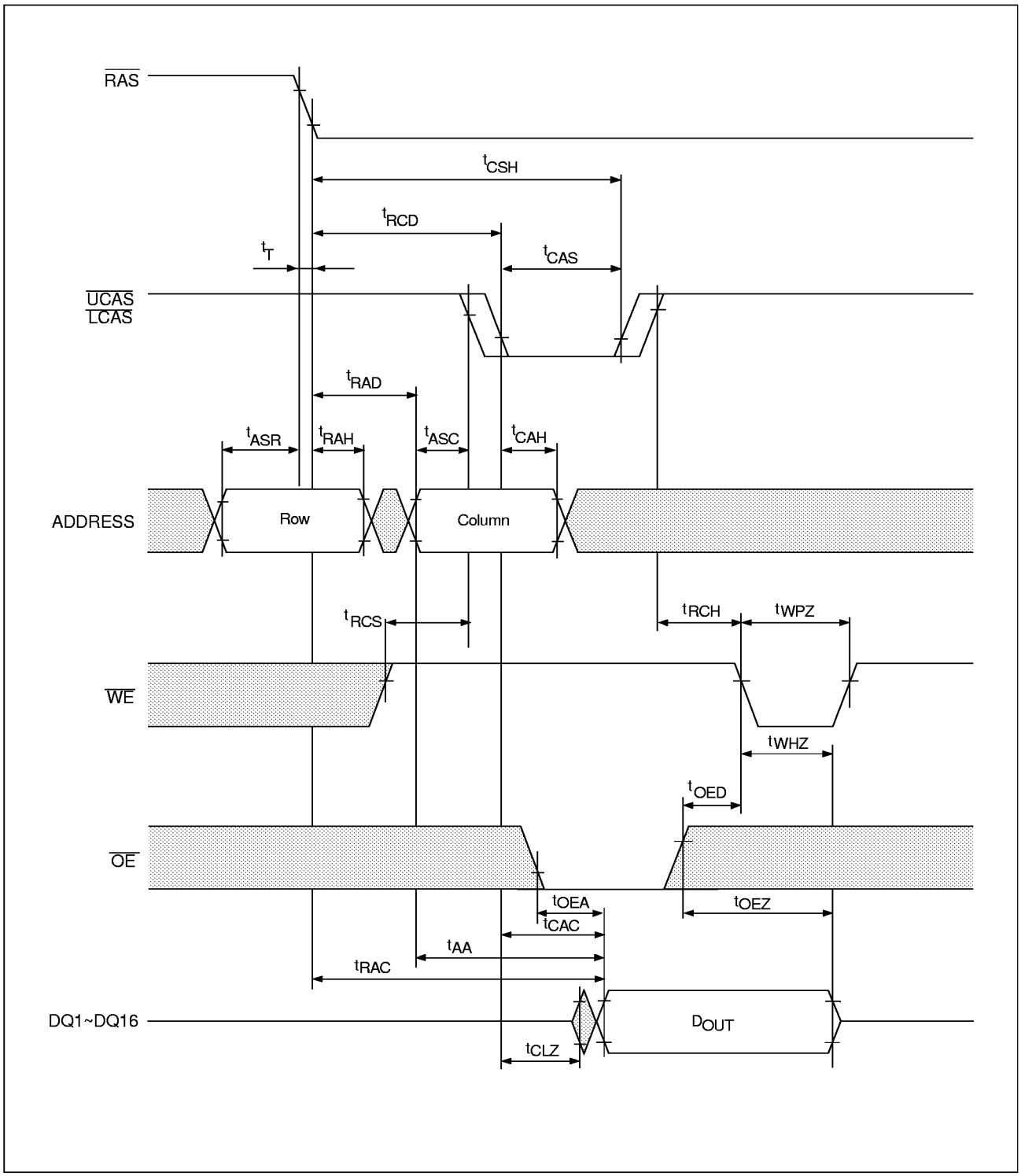
• **EDO Page Mode Word Read Cycle**



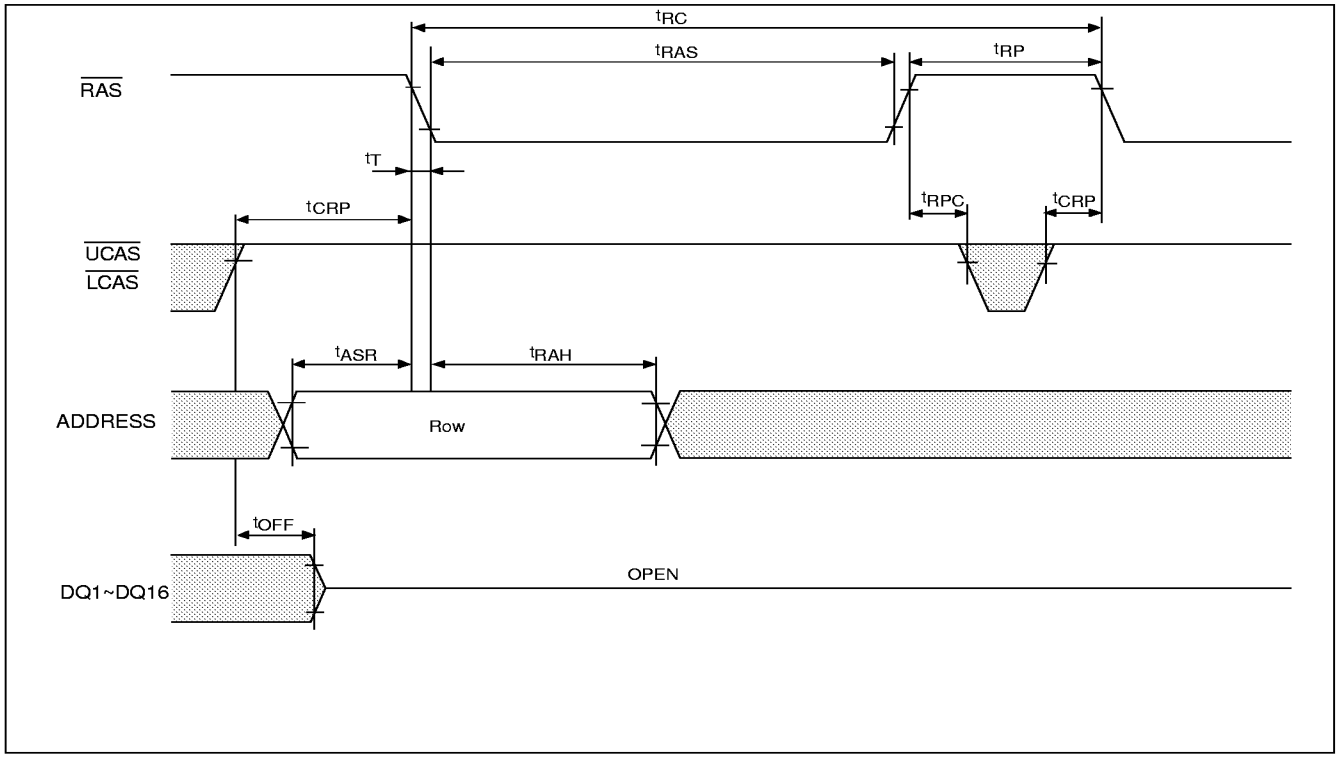
• **EDO Page Mode WORD Early Write Cycle**



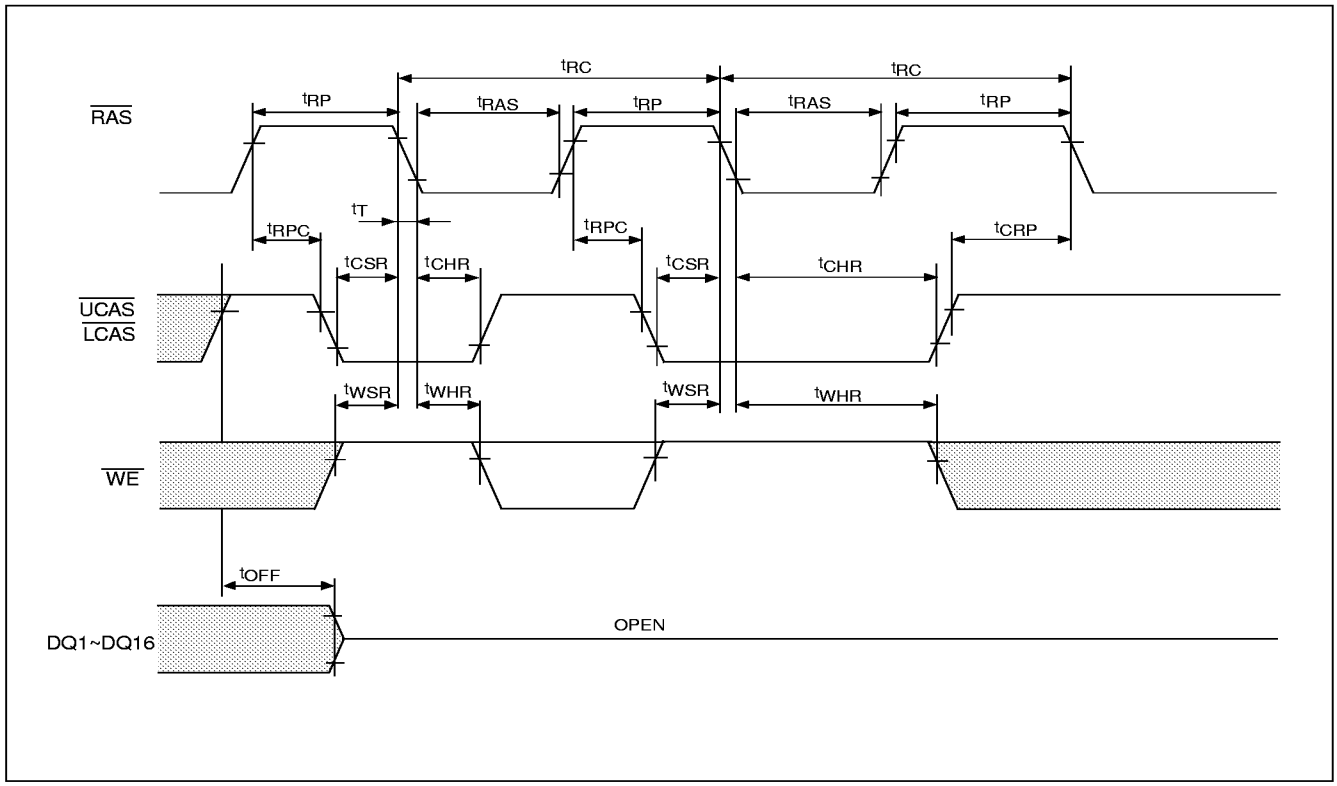
• **Read Cycle with $\overline{WE}$ Controlled Disable**



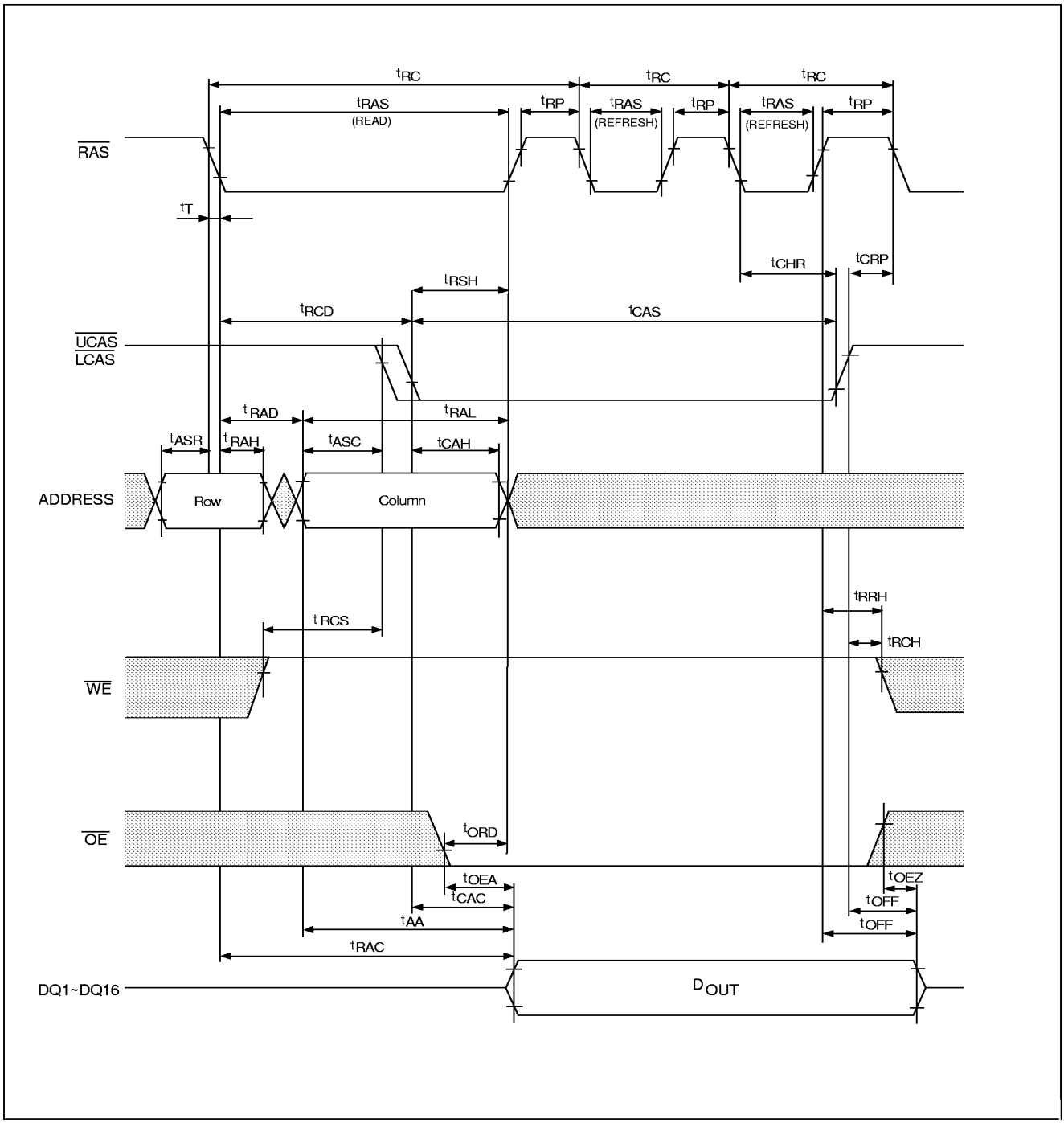
$\overline{RAS}$ - Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



• **Hidden Refresh Cycle**



Ordering information

Part Number	Access Time	Package
VG264265CJ - 25	25 ns	
VG264265CJ - 28	28 ns	
VG264265CJ - 3	30 ns	400mil
VG264265CJ - 35	35 ns	40 - Pin
VG26(V)4265CJ - 4	40 ns	Plastic SOJ
VG26V4265CJ - 5	50 ns	
VG26V4265CJ - 6	60 ns	

VG26(V)4265CJ - 3

- VG → • VIS Memory Product
- 26 → • Technology/Design Rule
- V → • 3.3V Version
- 4265 → • Device Type/Configuration
- C → • Mask/Design Version
- J → • Package Type, J : SOJ
- 3 → • Speed -5V: 25, 28, 30, 35, 40ns
  -3.3V: 40, 50, 60ns

Packaging Information
• 400mil, 40-pin Plastic SOJ

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	3.51	3.76	0.128	0.138	0.148
A1	2.08	---	---	0.082	---	---
b	0.38	---	0.51	0.015	---	0.020
b1	0.38	---	0.46	0.015	---	0.018
b2	0.66	0.71	0.81	0.026	0.028	0.032
c	0.18	---	0.33	0.007	---	0.013
c1	0.18	---	0.28	0.007	---	0.011
e	1.27 BASIC			0.050 BASIC		
D	25.91	26.04	26.16	1.020	1.025	1.030
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40 BASIC			0.370 BASIC		
R1	0.76	0.89	1.02	0.030	0.035	0.040
θ	3	---	16	3	---	16

NOTE:
1. CONTROLLING DIMENSION : INCHES
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION. INTERLEAD PROTRUSION SHALL NOT EXCEED 0.01" PER SIDE.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE SHOULDER WIDTH TO EXCEED b2 MAX BY MORE THAN 0.005" DAMBAR INTRUSION SHALL NOT REDUCE THE SHOULDER WIDTH TO LESS THAN 0.001" BELOW b2 MIN.