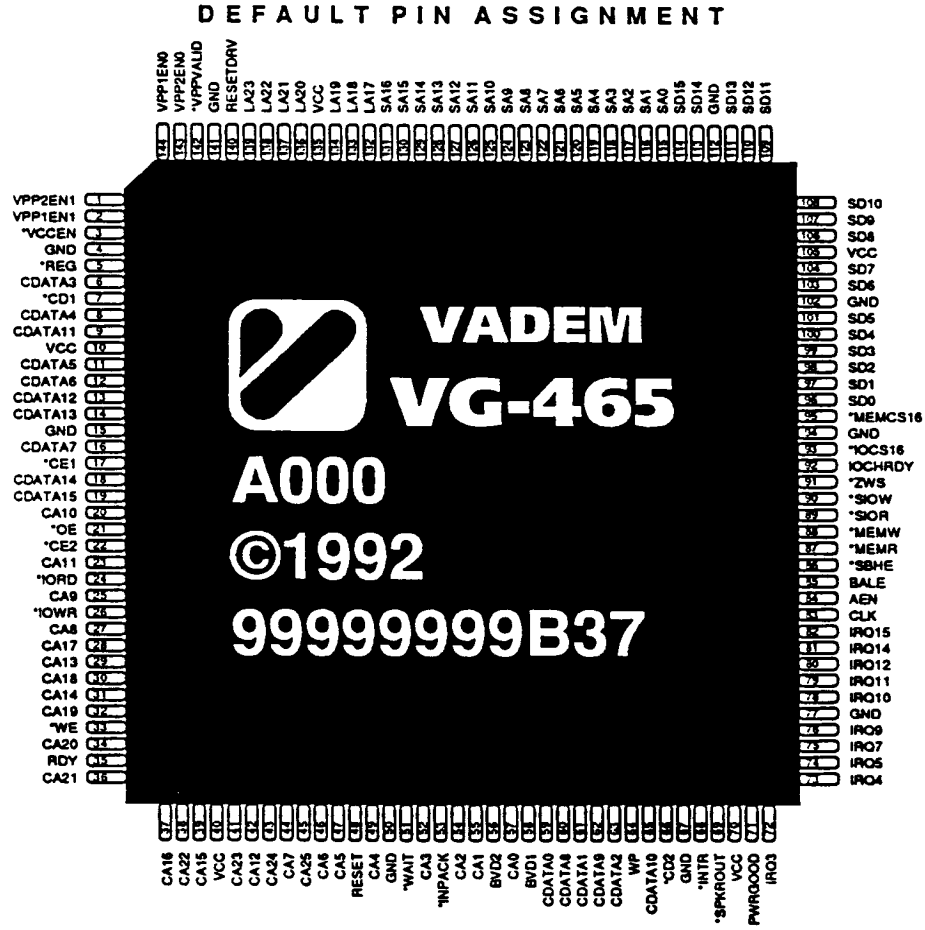
Pin Diagram

This section provides the pin assignment, signal description, block diagram, and pin descriptions for the VG-465 PC Card Socket Controller.

Pin Diagram
Figure 1-1



ALTERNATIVE PIN DEFINITIONS

PIN #	DEFAULT	ALTERNATIVE(S)
35	RDY/*BSY	*IREQ
56	BVD2	*SPKR
58	BVD1	*STSCHG, *RI
64	WP	*IOIS16
142	*VPPVALID	SRDATA, GPIO2, *RIO, *PCS1, LED, *CHIPSEL
143	VPP2EN0	*SRLOAD, GPIO1, *RIO
144	VPP1EN0	SRCLK, GPIO0, PCS0

Signal Description

Pin #	Signal Names	Type	Characteristics	# Pins
84	AEN	I	TTL Compatible	1
85	BALE	I	TTL Compatible	1
58	BVD1 (*STSCHG/*RI)	I	TTL Compatible	1
56	BVD2 (*SPKR)	I	TTL Compatible	1
45,43,41,38, 36,34,32,30, 28,37,39,31, 29,42,23,20, 25,27,44,46, 47,49,52,54, 55,57	CA[25:0]	O	4mA Tri-State	26
66,7	*CD[2:1]	I	TTL Compatible	2
19,18,14,13, 9,65,62,60, 16,12,11,8, 6,63,61,59	CDATA[15:0]	I/O	I = TTL Compatible O = 4mA Tri-State	16
22, 17	*CE[2:1]	O	4mA Tri-State	2
83	CLK	I	CMOS	1
4,15,50,67, 77,94,102, 112,141	GND	I		9
68	*INTR/*RIO	I/O	I = TTL Compatible O = 4mA Tri-State	1
144	GPIO0(SRCLK)	I/O	I = TTL Compatible O = 4mA Tri-State	1
143	GPIO1(*SRLOAD)	I/O	I = TTL Compatible O = 4mA Tri-State	1
142	GPIO2(SRDATA)	I/O	I = TTL Compatible O = 4mA Tri-State	1
53	*INPACK	I	TTL Compatible	1
92	IOCHRDY	O	16 mA Tri-State	1
93	*IOCS16	O	16 mA 5V Open Drain	1
24	*IORD	O	4mA Tri-State	1
26	*IOWR	O	4mA Tri-State	1
82-78, 76-72	IRQs	O	4mA Tri-State	10
139-136, 134-132	LA[23:17]	I	TTL Compatible	7
95	*MEMCS16	O	16 mA 5V Open Drain	1
87	*MEMR	I	TTL Compatible	1

Signal Description (cont.)

Pin #	Signal Names	Type	Characteristics	# Pins
88	*MEMW	I	TTL Compatible	1
21	*OE	O	4mA Tri-State	1
71	PWRGOOD	I	Schmitt Trigger	1
35	RDY/*BSY (*IREQ)	I	TTL Compatible	1
5	*REG	O	4mA Tri-State	1
48	RESET	O	2mA Tri-State	1
140	RESETDRV	I	Schmitt Trigger	1
131-115	SA[16:0]	I	TTL Compatible	17
86	*SBHE	I	TTL Compatible	1
89	*SIOR	I	TTL Compatible	1
90	*SIOW	I	TTL Compatible	1
114-113, 111-106 104-103, 101-96	SD[15:0]	I/O	I = TTL Compatible O = 8mA Tri-State	16
69	*SPKROUT	I/O	I = TTL Compatible O = 2mA Tri-State	1
10,40,70, 105,135	*VCC	I		5
3	*VCCEN	O	4mA Output	1
2	VPP1EN1	O	2mA Output	1
1	VPP2EN1	O	2mA Output	1
51	*WAIT	I	TTL Compatible	1
33	*WE/*PRGM	O	4mA Tri-State	1
64	WP (*IOIS16)	I	TTL Compatible	1
91	*ZWS	O	16mA 5V Open Drain	1

Pin Descriptions

Symbol	Type	Pin No.	Description
AEN	I	84	System Address Enable. High during DMA cycles, low otherwise.
BALE	I	85	Bus Address Latch Enable. An active high input used to latch LA[23:17] at the beginning of a bus cycle.
BVD1 (*STSCHG/*RI)	I	58	If BVD1 is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost. For I/O PC Cards, this signal is held high when either or both the Signal on Change bit and Changed bit in the Card Status Register on the PC Card are set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. Or this pin is connected to Ring Indicate, which is qualified by Ring Indicate Enable to be *RIO through *INTR or GPIO pins.
BVD2 (*SPKR)	I	56	BVD1 and BVD2 are generated by memory PC Cards with onboard batteries. These signals indicate the health of the battery. Both are asserted high when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery should be replaced, although data integrity on the memory PC Card is still assured. When the I/O interface is selected, BVD2 may be used to provide a single amplitude Digital Audio waveform intended to be passed through to the system's speaker without signal conditioning.
CA[25:0]	O	45,43,41, 38,36,34, 32,30,28, 37,39,31, 29,42,23, 20,25,27, 44,46,47, 49,52,54, 55,57	Card Address.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*CD[2:1]	I	66,7	Detects proper card insertion. The signals are connected to ground internally on the PC Card and will be forced low whenever a card is placed in a host socket. Status is available to software through the Interface Status Register.
CDATA[15:0]	I/O	19,18,14, 13,9,65, 62,60,16, 12,11,8, 6,63,61, 59	Card Data.
*CE[2:1]	O	22,17	Active low card enable signals. *CE1 is used to enable even bytes, *CE2 for odd bytes. A multiplexing scheme based on A0, *CE1, *CE2 allows 8-bit hosts to access all data on CDATA[7:0] if desired.
CLK	I	83	System clock.
GPIO0 (SRCLK)	I/O	144	General Purpose I/O 0: When the mouse interface is not enabled, depending on the setting of the GPIO Configuration Register, this pin can function as *VPP1EN0 output (power control signal for VPP1), PCS0 (active high programmable chip select 0), or general purpose I/O. It is used as the Shift Register Clock output if the mouse interface is enabled.
GPIO1 (*SRLOAD)	I/O	143	General Purpose I/O 1: When the mouse interface is not enabled, depending on the setting of the GPIO Configuration Register, this pin can function as VPP2EN0 output (power control signal for VPP2), *RIO output, or general purpose I/O. It is used as the Shift Register Load output if the mouse interface is enabled.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
GPIO2 (SRDATA)	I/O	142	General Purpose I/O 2: When the mouse interface is not enabled, depending on the setting of the GPIO Configuration Register, this pin can function as the following signals: *VPPVALID input (active low indicating VPP power supplies are at the proper voltage), *RIO output (pass through of Ring Indicator from PC Card), *PCS1 output (active low programmable chip select 1), *CHIPSEL input (from decoder if external address decoding is used), *LED output (pass through of BVD2 / *SPKR from PC Card disk drive, or general purpose I/O. It is used as the Shift Register Data input if the mouse interface is enabled.
*INPACK	I	53	Input Acknowledge. Asserted by some PC Cards during I/O read cycles. This signal is used by the VG-465 to control the enable of its input data buffer between the card and the CPU.
*INTR / *RIO	I/O	68	Interrupt Request / Ring Indicator output: Active low output requesting a nonmaskable interrupt to the CPU. Ring Indicator from PC Card can be routed to this pin if not routed to a GPIO pin. Also a resistor strapping input during RESETDRV to select one of four PC Card sockets.
IOCHRDY	O	92	I/O Channel Ready. This active high signal indicates that the current I/O bus cycle has completed. When a PC Card needs to extend a Read or Write cycle, the VG-465 pulls IOCHRDY low. IOCHRDY can be deasserted by either *WAIT, or by programming to add wait states for 16-bit memory and I/O cycles. If *WAIT is used in 16-bit mode, the wait state generator has to be set to 1 wait state.
*IOCS16	O	93	This active low I/O 16-bit chip select signal indicates to the host system the current I/O cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*IORD	O	24	I/O Read signal is driven active to read data from the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
*IOWR	O	26	I/O Write signal is driven active to write data to the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
IRQs	O	82-81, 80-78, 76,75, 74-72	IRQ[15, 14, 12:9, 7, 5:3].
LA[23:17]	I	139-136, 134-132	Local Address bus used to address memory devices on the ISA-bus. Together with the system address signals, they address up to 16MB on the ISA bus.
*MEMCS16	O	95	This active low 16-bit memory chip select signal indicates to the host system that the current memory cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is
*MEMR	I	87	Active low signal indicates a memory read cycle.
*MEMW	I	88	Active low signal indicates a memory write cycle.
*OE	O	21	Active low signal used to gate memory reads from memory cards.
PWRGOOD	I	71	Power Good is an active high signal which indicates that power to the system is stable. Connect to ground if not used.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
RDY/*BSY (*IREQ)	I	35	Memory PC Cards drive Ready / *Busy low to indicate that the memory card circuits are busy processing a previous write command. It is set high when they are ready to accept a new data transfer command. For I/O PC Cards, this pin is used as an interrupt request and driven low to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested.
*REG	O	5	Select attribute memory. This signal is set inactive (high) for all accesses to common memory of a PC Card. When it is active, access is limited to Attribute Memory when *WE or *OE are active, and to I/O ports when *IORD or *IOWR are active. I/O PC Cards will not respond to *IORD or *IOWR when the *REG signal is inactive. During DMA operations the *REG signal is inactive.
RESET	O	48	Provides a hard reset to a PC Card and clears the Card Configuration Option Register, thus placing card in an unconfigured (memory interface) state.
RESETDRV	I	140	Active high indicates a main system reset.
SA[16:0]	I	131-115	System Address bus used to address memory and I/O devices on the ISA bus. These signals are latched and are valid throughout the bus cycle.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*SBHE	I	86	System Byte High Enable. When asserted, this active low signal indicates that a data transfer is occurring on the upper byte of the system data bus.
SD[15:0]	I/O	114-113, 111-106, 104-103, 101-96	System Data Bus.
*SIOR	I	89	This active low I/O read signal instructs the VG-465 to drive data onto the data bus.
*SIOW	I	90	This active low I/O write signal instructs the VG-465 to latch the data on the data bus.
*SPKROUT	I/O	69	Digital audio signal which provides a single amplitude (digital) audio waveform to drive the system's speaker. Passes through *SPKR from an I/O PC Card. This signal must be held high when no audio signal is present. Also a resistor strapping input during RESETDRV to select one of four PCSCs.
*VCCEN	O	3	Power Control signal for card Vcc.
VPP1EN1	O	2	Power Control signal for card Vpp1.
VPP2EN1	O	1	Power Control signal for card Vpp2.
*WAIT	I	51	This signal is driven by the PC Card to delay completion of the memory or I/O cycle in progress.
*WE/*PRGM	O	33	The host uses *WE for gating memory write data, and for memory PC Cards that employ programmable memory.

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
WP (*IOIS16)	I	64	Reflects the status of the Write Protect switch on some memory PC Cards. If the memory PC Card has no write protect switch, the card will connect this line to ground (the card can always be written) or to Vcc (permanently write protected). When the I/O interface is selected, this pin is used for the "I/O is 16-bit Port" function: asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port which is addressed is capable of 16-bit access. If this signal is not asserted during a 16-bit I/O access, the system will generate 8-bit references to the even and odd byte of the 16-bit port being accessed. If 8-bit window size is selected, *IOIS16 is ignored.
*ZWS	O	91	Zero Wait State. An active low output indicates that the PC Card wishes to terminate the present bus cycle without inserting additional wait states. This cycle will not be driven during a 16-bit access.