VITESSE
SEMICONDUCTOR CORPORATION

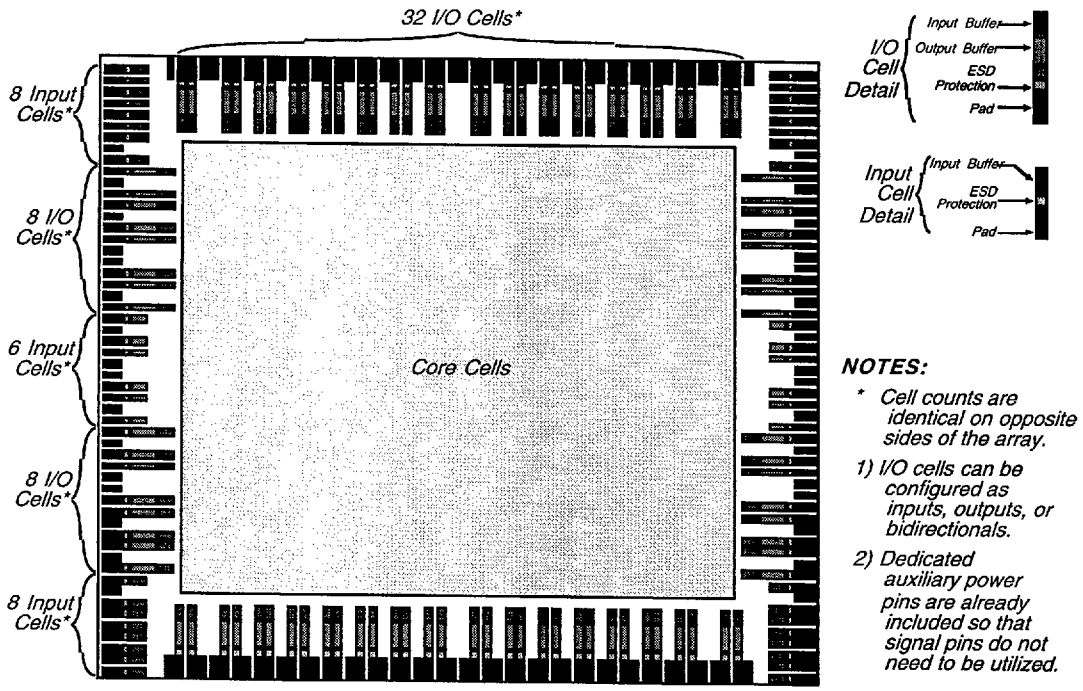
Data Sheet
Viper Family

High Performance, Low Cost
Viper Family Gate Arrays

Features

- 7,000-13,000 Usable Gates, Channelless Array Architecture
- Industry Standard Plastic Packaging
- Superior Speed/Power Performance and Cost Comparable to BiCMOS
- Production-Proven H-GaAs III Enhancement/ Depletion MESFET Process
- ECL, PECL, TTL, or Mixed Inputs/Outputs
- Array Performance
  - Typical gate delay: 118 ps @ 0.19 mW *(unbuffered 2-in NOR, F.O.= 1, 0.17 mm wire)*
  - Typical gate delay: 116 ps @ 0.59 mW *(buffered 2-in NOR, F.O.= 3, 0.51 mm wire)*
- Robust Clock Distribution Scheme for Minimized Clock Skew
- Multiple Buffering Options for Optimal Speed/ Power Solution

VGLC15K Gate Array Floorplan



NOTES:

* *Cell counts are identical on opposite sides of the array.*

1) I/O cells can be configured as inputs, outputs, or bidirectionals.

2) Dedicated auxiliary power pins are already included so that signal pins do not need to be utilized.

Introduction

The Viper family of gate arrays provides the best cost-per-function solution for the requirements of system applications from 50 to over 200 MHz. By combining the high performance of H-GaAs technology with the low cost of molded-plastic packages, Viper delivers two to three times the performance of BiCMOS at comparable cost. This allows the designer to implement much simpler architectures to achieve performance targets.

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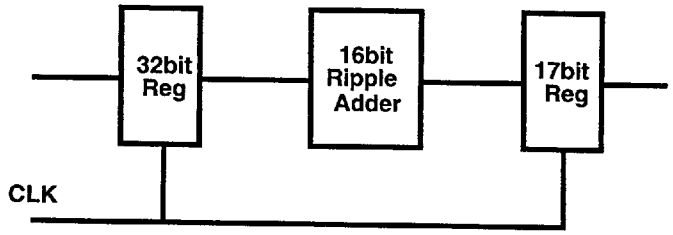
For example, assume that a design incorporates a 16-bit adder that must operate at 100 MHz. As shown in Figure 1, the BiCMOS adder requires 125 registers in a heavily pipelined architecture. However, Viper requires only 49 registers in a very simple ripple adder architecture to achieve 100 MHz, simplifying clock distribution and testability. Additionally, the Viper implementation consumes less power than the BiCMOS solution.

The Viper family is manufactured in the production proven H-GaAs III process, the same process used to build the Vitesse FX350K gate array which integrates over 1 million transistors on a single chip. Viper incorporates a channelless architecture allowing the first layer of metal to be routed over unused cells. This architecture eliminates the need for pre-defined channels allowing much greater density and flexibility than channelled arrays.

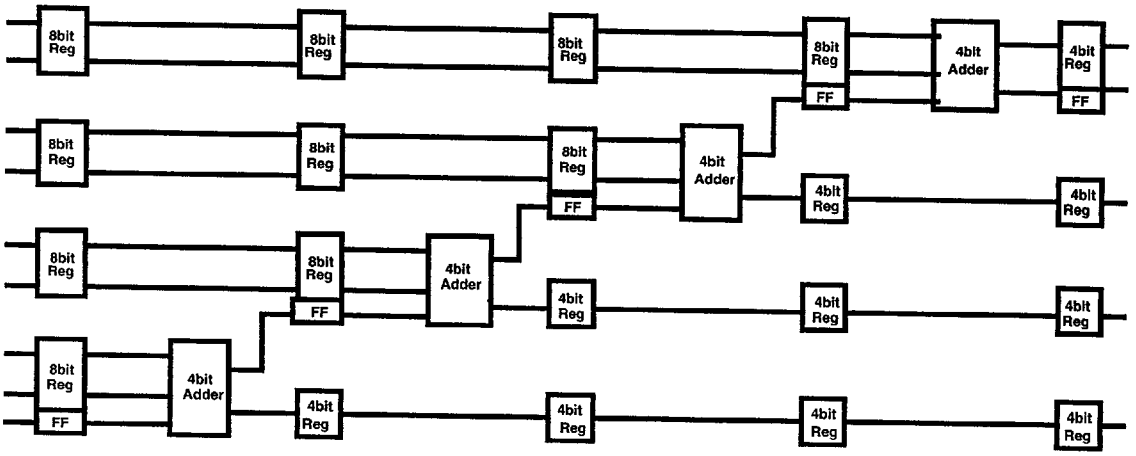
As with all Vitesse ASIC products, the Viper arrays are compatible with industry-standard TTL, ECL, and pseudo-ECL (PECL) signal levels, and utilize standard power supplies. Designs are supported on the ASIC industry's most popular CAE/EDA platforms for schematic capture, simulation, and logic synthesis. In addition, Vitesse offers customers a suite of proprietary tools which greatly enhance the ASIC design process.

Figure 1: Technology Comparison - 100 MHz 16-Bit Adder

Viper Ripple Architecture: 49 Registers



BiCMOS Pipelined Architecture: 125 Registers



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Technology

The H-GaAs III process represents the third enhancement to the original H-GaAs technology which was developed by Vitesse in 1986 to manufacture high yielding, LSI and VLSI digital GaAs circuits. H-GaAs III features 0.6 micron self-aligned gate MESFETs and four levels of standard aluminum interconnect.
The Viper arrays utilize direct-coupled FET (DCFL) logic in the core cells. The basic logic structure in DCFL is a 2-input NOR gate. Millions of hours of life testing have proven the reliability of the H-GaAs process technology and the DCFL logic structure.

Applications

The Viper arrays provide an optimum ASIC solution for applications at 50MHz or higher. Viper offers much shorter loaded gate delays than BiCMOS. The performance advantage of Viper enables system designers to consider simpler architectural alternatives, such as serializing data streams and eliminating pipeline stages - design complexities that would be necessary to achieve the same performance in BiCMOS.

Computers

The competitive price per function and the performance advantage that the Viper arrays offer, makes them ideally suited for cache control and other processor support functions as well as graphics and signal processing applications. In these applications, the clock rate is set by the processor. To achieve the required performance in BiCMOS, the architecture must be quite complex.
For example, to achieve 0-wait state performance in a Pentium™-based system, BiCMOS cache control designs would require very deep pipelines or interleaving as the performance pushes up against the top end of the capability of BiCMOS technology. The 2-3X performance advantage of Viper allows the designer to implement a simpler architecture to achieve the required performance. Viper is also excellent for consolidating high speed programmable logic devices into a single array. This application increases system performance by eliminating chip-to-chip delay and reduces board space and overall system cost.

Communications

Low cost and high performance allow Viper to serve as an enabling technology for high speed parallel data transfer between, for example, CPUs and disk arrays. Mux/demux implementations for this serial communication link and both standard and self-routing ATM switches can be implemented in a Viper array.

Packaging

Viper arrays are packaged in low-cost, thermally-enhanced plastic molded packages. Originally developed as a solution for the power consumption of BiCMOS technology, these packages feature standard EIAJ footprints. For thermal enhancement, the die attaches directly to a copper heat spreader in a cavity down configuration. This copper mass serves as an excellent thermal path between the die junction and the package case. Standard mold compound is used to encapsulate the package such that the heat spreader surface becomes a part of the top surface of the package.

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Table 1: Viper Array Specific Features

Array Name	*# of Internal Gates*		*# of Input Cells*	*# of I/O Cells*	*Total Signal Pins*	*Package Options*
	Usable Gates	*D Flip-Flops*				
VGLC10K	7K	700K	7	24	31	52 PQFP(1)
			31	40	71	100 PQFP(2)
VGLC12K	10K	1K	39	52	91	144 PQFP(3)
VGLC15K	13K	1.3K	36	99	135	208 PQFP(3)

NOTE: (1) EIAJ footprint, 14 x 14 mm body size, thermally enhanced package.
(2) EIAJ footprint, 14 x 20 mm body size, thermally enhanced package.
(3) EIAJ footprint, 28 x 28 mm body size, thermally enhanced package.

Architecture

The Viper arrays contain three cell types: core logic cells, input only cells, and input/output (I/O) cells. All input only and input/output cells contain enough user-configurable logic to implement moderately complex functions such as multiplexers and flip flops, allowing the arrays to incorporate JTAG boundary scan functions.

Clock Distribution

A standard clock buffer and distribution scheme has been pre-defined for each member of the Viper Family. This robust clock tree minimizes signal skew to registered functions within the array. Clock skew of 90 ps across the die is achievable on the VGLC15K.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements needed for each logic function. The primitive element or building block is a cell which consists of a single depletion-mode transistor and two enhancement-mode transistors which can be connected to make a 2-input NOR gate.

Input Only Cells

Input only cells are located primarily on two edges of the periphery of the array. Input cells are also located in input/output cells. Input cells contain the equivalent of 24 user-configurable logic cells which can be personalized as logic functions in the macrocell library. Each input only cell has resources to form a JTAG boundary scan flip-flop for ECL and TTL only arrays. Input cells are compatible with TTL, ECL, and pseudo-ECL signals. All signal levels can be used in one chip design to optimize overall system performance. Input cells can provide 1x or 2x drive on either the true or complement signal. These cells also provide ESD input protection.

Input/Output (I/O) Cells

Input/Output cells are located on all four sides of the array. I/O cells can be configured as output drivers, input receivers, or bidirectional transceivers. TTL, ECL, and pseudo-ECL signal levels are supported on the same

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chip. The output portion of I/O cells contain the equivalent of 24 user-configurable logic cells which can implement functions from the macrocell library. Boundary scan can be easily accommodated since each I/O cell can be configured as a JTAG flip-flop for ECL and TTL only arrays. When configured as an ECL driver, the output cell can interface with ECL 100K receivers while driving a 50W load. Two output cells may be paralleled to drive a double-terminated transmission line (25W DC load).

Power Supplies

The Viper Family uses industry-standard power supplies. For a Viper array requiring only ECL levels, -2V is the only power supply required. For Viper arrays which use only TTL levels or PECL levels, +5V and +2V supplies are needed. If both ECL and TTL levels are required, -2V and +3.3V are the required power supplies.

Macrocell Library

The Viper Macrocell Library contains information to fully evaluate the function and performance of logic blocks (macrocells). The Viper library includes functional equivalents for all FURY™ and FX™ macrocells as well as several additional macrocell functions. The table below is a representative list of the macrocells which are available for Viper arrays. Performance characteristics for selected macrocells are given on page XX. For a complete set of specifications, refer to the FX/Viper Macrocell Library.

Table 2: Input/Output Buffers

Name	*Description*
BIE	ECL Bi-directional Buffer (1X Drive)
BIE25NR2	ECL Bi-directional 25W Buffer w/2-Input NOR (1X Drive)
BIE25NR2S	ECL Input Buffer & Bi-directional 25 W Buffer w/2-Input NOR (1X Drive)
BIE25NR2T	ECL Input Buffer & Bi-directional 25 W Buffer w/2-Input NOR (2X Drive)
BIE25NR3	ECL Bi-directional 25W Buffer w/3-Input NOR (1X Drive)
BIENR2	ECL Bi-directional Buffer w/2-Input NOR (1X Drive)
BIENR2S	ECL Bi-directional Buffer w/2-Input NOR (1X Drive)
BIENR2T	ECL Bi-directional Buffer w/2-Input NOR (2X Drive)
BIT	TTL Bi-directional Buffer (-2.V/+3.3 V) (1X Drive)
BITK	TTL Bi-directional Buffer (+2 V/+5 V) (1X Drive)
BIT2K	TTL Bi-directional Buffer (+2 V/+5 V) (1X Drive)
BITOC	TTL Bi-directional Buffer w/Open Collector Output (-2 V/+3.3 V) (1X Drive)
BITOCK	TTL Bi-directional Buffer w/Open Collector Output (+2 V/+5 V) (1X Drive)
IE1F	ECL Inverting Input Buffer (1X Drive)
IE1T	ECL Input Buffer (1X Drive)
IE2T	ECL Input Buffer (2X Drive)
IECK3	ECL Input Buffer w/Dual Outputs (3X Drive)
IEDIFF	ECL Differential Input Buffer (1X Drive)
IEDIF2	ECL Differential Input Buffer (2X Drive)
IEDIF3	ECL Differential Input Buffer w/Dual Outputs (3X Drive)

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Table 2: Input/Output Buffers

Name	*Description*
IEINV2T	ECL Input Buffer w/Conditional Inversion (2X Drive)
IETOM6	ECL Input Buffer w/ 6:1 Test Output
IT1T	TTL Input Buffer (1X Drive) (-2 V/+3.3 V)
IT1TK	TTL Input Buffer (1X Drive) (+2 V/+5 V)
OE	ECL Output Buffer
OE25	ECL 25W Output Buffer
OENOR3	ECL Output Buffer w/3-Input NOR
OEPNC	ECL Output Buffer w/PNC Test Mode
OESD	ECL Differential Output Buffer
OT	TTL Output Buffer (-2 V/+3.3 V)
OTPNC	TTL Output Buffer w/PNC Test Mode
OTK	TTL Output Buffer (+2 V/+5 V)
OTKPNC	TTL Output Buffer w/PNC Test Mode
OT2K	TTL Output Buffer (+2 V/+5 V)

Table 3: Input/Output Registers

Name	*Description*
BIEJ	ECL Bi-directional Buffer w/JTAG Register (1X Drive)
BIER	ECL Bi-directional Buffer w/Scan Register & Register Enable (1X Drive)
IEJ1T	ECL Input Buffer w/JTAG Register (1X Drive)
IELBS1T	ECL Input Buffer w/Scan Register & Bypass (1X Drive)
IEMDF	ECL Input Buffer w/Scan Register (1X Drive)
IER1T	ECL Input Buffer w/Scan Register & Register Enable (1X Drive)
IERINV1T	ECL Input Buffer w/Scan Register & Conditional Inversion (1X Drive)
OEDRR4	ECL Output Buffer w/Double Ranked Register
OEJ	ECL Output Buffer w/JTAG Register
OEMDF	ECL Output Buffer w/Scan Register
OER	ECL Output Buffer w/Scan Register & Register Enable
IETO	ECL Input Buffer w/RAM Test Output (1X Drive)
OETI	ECL Output Buffer w/RAM Test Mode

Table 4: Buffers/Inverters

Name	*Description*
CLK0	Clock Buffer (1.5X Drive)
CLK1	Clock Buffer (3X Drive)
LB3S	Inverter (1X Drive)
LDLY1	Delay Buffer (0.5X Drive)

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Table 4: Buffers/Inverters

Name	*Description*
LDLY2	Delay Buffer (0.5X Drive)
LDR1	Inverting Buffer/Line Driver (1X Drive)
LDR2	Inverting Buffer/Line Driver (2X Drive)
LDR3	Inverting Buffer/Line Driver (3X Drive)
LAND	2-Input AND Gate (1X Drive)
LANDU	2-Input AND Gate (0.5X Drive)
LAND3U	3-Input AND Gate (0.5X Drive)
LAND4	4-Input AND Gate (1X Drive)
LANDI31U	3-Input AND Gate w/Single Inverting Input (0.5X Drive)
LANDI41U	4-Input AND Gate w/Single Inverting Input (0.5X Drive)
LN2	2-Input NOR Gate (1X Drive)
LN2B	2-Input NOR Gate (2X Drive)
LN2US	2-Input NOR Gate (0.5X Drive)
LN3	3-Input NOR Gate (1X Drive)
LN3U	3-Input NOR Gate (0.5X Drive)
LN4	4-Input NOR Gate (1X Drive)
LN4B	4-Input NOR Gate (2X Drive)
LN4U	4-Input NOR Gate (0.5X Drive)
LN6	6-Input NOR Gate (1X Drive)
LN6U	6-Input NOR Gate (0.5X Drive)
LN9	9-Input NOR Gate (1X Drive)
LN9B	9-Input NOR Gate (2X Drive)
LN9U	9-Input NOR Gate (0.5X Drive)
LNA2	2-Input NAND Gate (1X Drive)
LNA2U	2-Input NAND Gate (0.5X Drive)
LNA2Z	Low Speed 2-Input NAND Gate (0.5X Drive)
LNA4	4-Input NAND Gate (1X Drive)
LNA4U	4-Input NAND Gate (0.5X Drive)
LNI21	2-Input NOR Gate w/Single Inverting Input (1X Drive)
LNI21U	2-Input NOR Gate w/Single Inverting Input (0.5X Drive)
LNI31	3-Input NOR Gate w/Single Inverting Input (1X Drive)
LNI31U	3-Input NOR Gate w/Single Inverting Input (0.5X Drive)
LNI42U	4-Input NOR Gate w/Dual Inverting Inputs (0.5X Drive)
LO2	2-Input OR Gate (1X Drive)
LO2B	2-Input OR Gate (2X Drive)
LO2U	2-Input OR Gate (0.5X Drive)
LO32B	3-Input OR Gate w/Dual Outputs (2X Drive)
LO34	3-Input OR Gate w/Quad Outputs (1X Drive)

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Table 4: Buffers/Inverters

Name	*Description*
LO3C	3-Input OR Gate (3X Drive)
LO4	4-Input OR Gate (1X Drive)
LO4B	4-Input OR Gate (2X Drive)
LO4U	4-Input OR Gate (0.5X Drive)
LOI21	2-Input OR Gate w/Single Inverting Input (1X Drive)
LOI21U	2-Input OR Gate w/Single Inverting Input (0.5X Drive)
LOI31	3-Input OR Gate w/Single Inverting Input (1X Drive)
LOI31U	3-Input OR Gate w/Single Inverting Input (0.5X Drive)
LOI42	4-Input OR Gate w/Dual Inverting Inputs (1X Drive)
LOI42U	4-Input OR Gate w/Dual Inverting Inputs
LX1	2-Input Exclusive OR Gate (1X Drive)
LX1U	2-Input Exclusive OR Gate (0.5X Drive)
LX2	2-Input Exclusive NOR Gate (1X Drive)
LX2U	2-Input Exclusive NOR Gate (0.5X Drive)
LX3	3-Input Exclusive OR Gate (1X Drive)
LX4	4-Input Exclusive OR Gate (1X Drive)

Table 5: Complex Gates

Name	*Description*
OA21	2-1 Input OR-AND Complex Gate (1X Drive)
OA21U	2-1 Input OR-AND Complex Gate (0.5X Drive)
OA22	22-InputOR-ANDComplexGate(1XDrive)
OA22B	2 2-Input OR-AND Complex Gate (2X Drive)
OA22U	2 2-Input OR-AND Complex Gate (0.5X Drive)
OA222	3 2-Input OR-AND Complex Gate (1X Drive)
OA222B	3 2-Input OR-AND Complex Gate (2X Drive)
OA222U	3 2-Input OR-AND Complex Gate (0.5X Drive)
OA2222	4 2-Input OR-AND Complex Gate (1X Drive)
OA2222B	4 2-Input OR-AND Complex Gate (2X Drive)
OA2222U	4 2-Input OR-AND Complex Gate (0.5X Drive)
OA2X6	6 2-Input OR-AND Complex Gate (1X Drive)
OA2X6U	6 2-Input OR-AND Complex Gate (0.5X Drive)
OA2X9	9 2-Input OR-AND Complex Gate(1X Drive)
OA2X9U	9 2-Input OR-AND Complex Gate (0.5X Drive)
OA2X12	12 2-Input OR-AND Complex Gate (1X Drive)
OA41	4-1 Input OR-AND Complex Gate (1X Drive)
OA41U	4-1 Input OR-AND Complex Gate (0.5X Drive)

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Table 5: Complex Gates

Name	*Description*
OA4321	4-3-2-1 Input OR-AND Complex Gate (1X Drive)
OA4321U	4-3-2-1 Input OR-AND Complex Gate (0.5X Drive)
OA44	2 4-Input OR-AND Complex Gate (1X Drive)
OA44U	2 4-Input OR-AND Complex Gate (0.5X Drive)
OA4444	4 4-Input OR-AND Complex Gate (1X Drive)
OA4444U	4 4-Input OR-AND Complex Gate (0.5X Drive)
OAI221U	2-1 Input OR-AND Complex Gate w/Inverting AND Input
OAI231U	2-1-1 Input OR-AND Complex Gate w/Single Inverting AND Input
ON22	2 2-Input OR-NAND Complex Gate (1X Drive)
ON22B	2 2-Input OR-NAND Complex Gate (2X Drive)
ON222	3 2-Input OR-NAND Complex Gate (1X Drive)
ON222B	3 2-Input OR-NAND Complex Gate (2X Drive)
ON2222	4 2-Input OR-NAND Complex Gate (1X Drive)
ON2222B	4 2-Input OR-NAND Complex Gate (2X Drive)
ON2X9	9 2-Input OR-NAND Complex Gate (1X Drive)
ON2X9U	9 2-Input OR-NAND Complex Gate (0.5X Drive)

Table 6: Encoders/Decoders

Name	*Description*
LDE4	2-4 Decoder

Table 7: Multiplexers

Name	*Description*
LM1	2:1 Multiplexer (1X Drive)
LM1B	2:1 Multiplexer (2X Drive)
LM1U	2:1 Multiplexer (0.5X Drive)
LM3	4:1 Multiplexer (1X Drive)
LM3B	4:1 Multiplexer (2X Drive)
LM3U	4:1 Multiplexer (0.5X Drive)
LM3X2U	Dual 4:1 Multiplexer (0.5X Drive)
LM7	8:1 Multiplexer (1X Drive)

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Table 8: Latches

Name	*Description*
LLN1	Negative Transparent D Latch (1X Drive)
LLP1	Positive Transparent D Latch (1X Drive)
LLP1U	Positive Transparent D Latch (0.5X Drive)
LLP2	Positive Transparent D Latch w/2-Input OR (1X Drive)
LLP3	Positive Transparent D Latch w/2:1 Mux (1X Drive)
LLP4U	Positive Transparent D Latch w/Q & QN Outputs (0.5X Drive)

Table 9: Flip-Flops

Name	*Description*
LFP1	Positive Edge D Flip-Flop (1X Drive)
LFP1B	Positive Edge D Flip-Flop (2X Drive)
LFP1U	Positive Edge D Flip-Flop (0.5X Drive)
LFP2	Low Power Positive Edge D Flip-Flop (1X Drive)
LFP2U	Low Power Positive Edge D Flip-Flop (0.5X Drive)
LFP3	Positive Edge D Flip-Flop w/Set & Reset (1X Drive)
LFP3U	Positive Edge D Flip-Flop w/Set & Reset (0.5X Drive)
LFP4	Positive Edge D Flip-Flop w/Set (1X Drive)
LFP5	Positive Edge D Flip-Flop w/4-Input OR (1X Drive)
LFP6U	Positive Edge D Flip-Flop w/Q, QN Outputs & Set, Reset (0.5X Drive)
LJK1U	Positive Edge JK Flip-Flop (0.5X Drive)
LJK3U	Positive Edge JK Flip-Flop w/Set & Reset (0.5X Drive)
LTF3U	T Flip-Flop w/Set & Reset (0.5X Drive)

Table 10: Registers

Name	*Description*
LDRR4	Double Ranked Register (1X Drive)
LDRR4U	Double Ranked Register (1X Drive)
LJP1	JTAG Register (1X Drive)
LSP1	Scan Register (1X Drive)
LSP1U	Scan Register (0.5X Drive)
LSP1Z	Low Speed Scan Register (0.5X Drive)
LSP1R	Scan Register w/Reset (1X Drive)
LSP2	Scan Register w/Enable (1X Drive)
LSP2U	Scan Register w/Enable (0.5X Drive)
LSP3	Scan Register w/Enable (1X Drive)
LSP3B	Scan Register w/Enable (2X Drive)

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Table 10: Registers

Name	*Description*
LSP3U	Scan Register w/Enable (0.5X Drive)
LSP4	Scan Register w/Enable & Bus Inputs (1X Drive)
LSP4U	Scan Register w/Enable & Bus Inputs (0.5X Drive)

Table 11: Arithmetic Functions

Name	*Description*
CNT1	Positive Edge Triggered 1-Bit Counter (1.5X Drive)
LA1	Half-Adder (1X Drive)
LA1U	Half-Adder (0.5X Drive)
LA2	Full-Adder (1X Drive)
LA2B	Full-Adder (2X Drive)
LA2U	Full-Adder (0.5X Drive)
LADD4	4-Bit Adder (1X Drive)
LCAR4	4-Bit Carry-Lookahead Generator w/Inverted Outputs (1X Drive)
LCL1	4-Bit Carry-Lookahead Generator w/block Outputs (1X Drive)
LCL2	4-Bit Carry-Lookahead Generator w/Carry Outputs (1X Drive)
LCL3	4-Bit Carry-Lookahead Generator w/3 Carry Outputs (1X Drive)
LCS1	1-Bit Carry Select Adder (1X Drive)
LCSA1	3-2 Carry Save Adder (1X Drive)
XN2222	4-Bit Comparator w/Inverted Output (1X Drive)

Table 12: Fixed Clock Tree Drivers

Name	*Description*
CLK40K	ECL Differential Input Fixed Clock Tree for 40K Array
CLK40KT	TTL Input Fixed Clock Tree for 40K Array

Table 13: Miscellaneous

Name	*Description*
LOAD	Load Macro
PD	Pull-Down to VTT (-2 V/0 V, -2 V/+3.3 V) or VCC (+2 V/+5 V)

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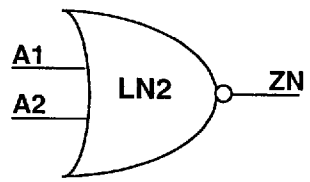
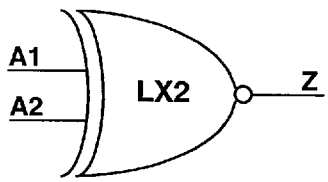
Selected Macrocell AC Performance

(Over Recommended Operating Conditions, Commercial Temperature Range

LN2: Buffered 2-input NOR	*Parameter*		*Min*	*Typ*	*Max*	*Units*
	Propagation Delay					
	A1, A2 to ZN	Rising Signal	24	—	104	ps
		Falling Signal	15	—	65	ps
	Load Dependent Delay					
	Delay/Fan-out	Rising Signal	3		11	ps
		Falling Signal	2		8	ps
	Delay / mm wire	Rising Signal	44	—	189	ps
		Falling Signal	24	—	104	ps
	Power Dissipation		-	0.58	0.87	mW

LN2: 2-input XNOR	*Parameter*		*Min*	*Typ*	*Max*	*Units*
	Propagation Delay					
	A1, A2 to ZN	Rising Signal	54	—	442	ps
		Falling Signal	69	—	403	ps
	Load Dependent Delay					
	Delay/Fan-out	Rising Signal	3	—	11	ps
		Falling Signal	2	—	10	ps
	Delay / mm wire	Rising Signal	44	—	189	ps
		Falling Signal	31	—	133	ps
	Power Dissipation		-	1.12	1.68	mW

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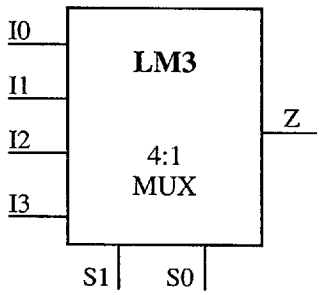
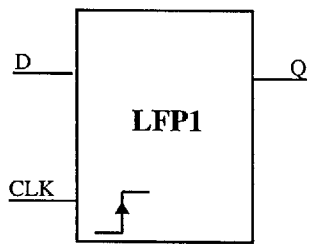
LM3: 4:1 Multiplexer	*Parameter*		*Min*	*Typ*	*Max*	*Units*
	Propagation Delay					
	S0, S1 to Z	Rising Signal	63	—	468	ps
		Falling Signal	81	—	442	ps
	I0-I3 to Z	Rising Signal	63	—	273	ps
		Falling Signal	81	—	351	ps
	Load Dependent Delay					
	Delay/Fan-out	Rising Signal	3	—	13	ps
		Falling Signal	2	—	10	ps
	Delay / mm wire	Rising Signal	50	—	215	ps
		Falling Signal	31	—	133	ps
	Power Dissipation		-	1.67	2.50	mW

LFP1: Positive Edge Triggered D Flop-flop	*Parameter*		*Min*	*Typ*	*Max*	*Units*
	Propagation Delay					
	CLK to Q	Rising Signal	54	—	234	ps
		Falling Signal	87	—	377	ps
	t_{SET-UP}		30	—	130	ps
	t_{HOLD}		21	—	91	ps
	Load Dependent Delay					
	Delay/Fan-out	Rising Signal	5	—	11	ps
		Falling Signal	6	—	9	ps
	Delay / mm wire	Rising Signal	90	—	189	ps
		Falling Signal	81	—	127	ps
	Power Dissipation		—	2.03	3.05	mW

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Absolute Maximum Ratings for ECL Only (-2V) and Mixed ECL/TTL (-2V, +3.3V) Power Supply Levels (1)

Power Supply Voltage (ECL), V_{TT} potential to GND ..... -2.2V to +0.5 V
Power Supply Voltage (TTL), V_{TTL} potential to GND ..... -0.5V to +4.3 V
ECL Input Voltage Applied, ($V_{IN\ ECL}$) ..... +0.5V to V_{TT} - 1.0 V
TTL Input Voltage Applied, ($V_{IN\ TTL}$) ..... -0.5V to V_{TTL} + 1.0 V
ECL, PECL, or TTL Output Current, I_{OUT} 50mA
Case Temperature Under Bias, (T_C) ..... -55 to +125°C
Storage Temperature, (T_{STG}) ..... -65C to +150°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions for ECL Only (-2V) and Mixed ECL/TTL (-2V, +3.3V) Power Supply Levels

ECL Supply Voltage, (V_{TT}) ..... -2.0V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +3.3V ± 5%
Commercial Operating Temperature Range, (T)(1). ..... 0 to 70°C

NOTES: (1) Lower limit is ambient temperature and upper limit is case temperature.

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DC Characteristics for ECL Only (-2V) and Mixed ECL/TTL (-2V, +3.3V) Power Supply Levels

Table 14: TTL Inputs/Outputs *(Over recommended commercial operating conditions, TTLGND = GND)*

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	0.4	V	I_{OL} = 16 mA
V_{IH}	Input HIGH voltage	2.0	V_{TTL} +1.0	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	50	µA	$V_{IN} = V_{TTL}$ -1.0V
I_{IL}	Input LOW current	-500	—	µA	V_{IN} = 0.4V
I_{OZH}	3-State Output OFF Current HIGH	—	200	µA	V_{OUT} = 2.4V
I_{OZL}	3-State Output OFF Current LOW	-100	—	µA	V_{OUT} = 0.4V
I_{OCZ}	Open collector output leakage current	—	200	µA	V_{OUT} = 2.4V

Table 15: ECL Inputs/Outputs *(Over recommended commercial operating conditions with internal V_{REF} $V_{CC} = V_{CCA}$ = GND, Output load 50Ω to V_{TT})*

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-1020	-700	mV	$V_{IN} = V_{IH}^{(max)}$
V_{OL}	Output LOW voltage	-2000	-1620	mV	or $V_{IL}^{(min)}$
V_{IH}	Input HIGH voltage	-1100	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	200	µA	$V_{IN} = V_{IH}^{(max)}$
I_{IL}	Input LOW current	-50	—	µA	$V_{IN} = V_{IL}^{(min)}$

NOTES:
(1) Differential ECL output pins must be terminated identically

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Absolute Maximum Ratings for TTL /PECL (+2V, +5V) Power Supply Levels[1]

Power Supply Voltage, (V_{MM}) potential to GND ..... -0.5V to +2.5V
Power Supply Voltage, V_{TTL} potential to GND ..... -0.5V to +5.5V
TTL Input Voltage Applied, ($V_{IN\ TTL}$)[2] ..... -0.5V to V_{TTL} + 0.5V
PECL Input Voltage Applied, ($V_{IN\ PECL}$)[2] ..... V_{TTL} -2V to V_{TTL} + 0.5V
TTL or PECL Output Current, I_{OUT} (DC, output HI) 50mA
Case Temperature Under Bias, (T_C) ..... -55C to +125°C
Storage Temperature, (T_{STG})[3] ..... -65C to +150°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT}, V_{TTL} must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.
(3) Lower limit is ambient temperature and upper limit is case temperature.

Recommended Operating Conditions for TTL/PECL (+2V, +5V) Power Supply Levels

Supply Voltage, (V_{MM}) ..... +2.0V ± 5%
Supply Voltage, (V_{TTL}) ..... +5.0V ± 5%
Commercial Operating Temperature Range, (T)[1] ..... 0 to 70°C

NOTE: (1) Lower limit is ambient temperature and upper limit is case temperature.

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DC Characteristics for TTL/PECL +2V, +5V Power Supply Levels

Table 16: TTL Inputs/Outputs *(Over recommended commercial operating conditions, TTLGND = GND)*

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	V_{TTL} +0.5	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	50	µA	$V_{IN} = V_{TTL}$ -1.0V
I_{IL}	Input LOW current	-500	—	µA	V_{IN} = 0.5V
I_{OZH}	3-State Output OFF Current HIGH	—	200	µA	V_{OUT} = 2.4V
I_{OZL}	3-State Output OFF Current LOW	-200	—	µA	V_{OUT} = 0.5V
I_{OCZ}	Open collector output leakage current	—	200	µA	V_{OUT} = 2.4V

Table 17: PECL Inputs/Outputs (Over recommended commercial operating conditions full external V_{REF} = *V_{TTL} -1.32, Output load 50Ω to V_{TTL}-2.0V).*

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	V_{TTL} -1020	V_{TTL} -700	mV	
V_{OL}	Output LOW voltage	V_{TTL} -2000	V_{TTL} -1620	mV	
V_{IH}	Input HIGH voltage	V_{TTL} -1100	V_{TTL} -700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	V_{TTL} -2000	V_{TTL} -1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	200	µA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW current	-50	—	µA	$V_{IN} = V_{IL}$ (min)

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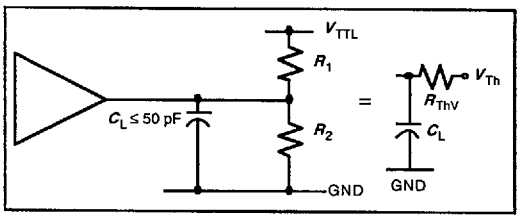
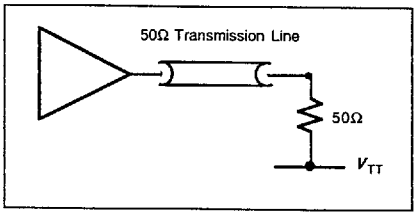
Equivalent Circuits for Output Loads

TTL



ECL



PECL

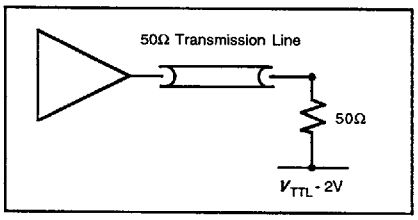


Table 18: Equivalent Circuits for Output Loads

Power Supplies	R_1	R_2	R_{ThV}	V_{ThV}
+2, +5	467	301	183	1.96V
-2, +3.3	252	189	108	2.14V

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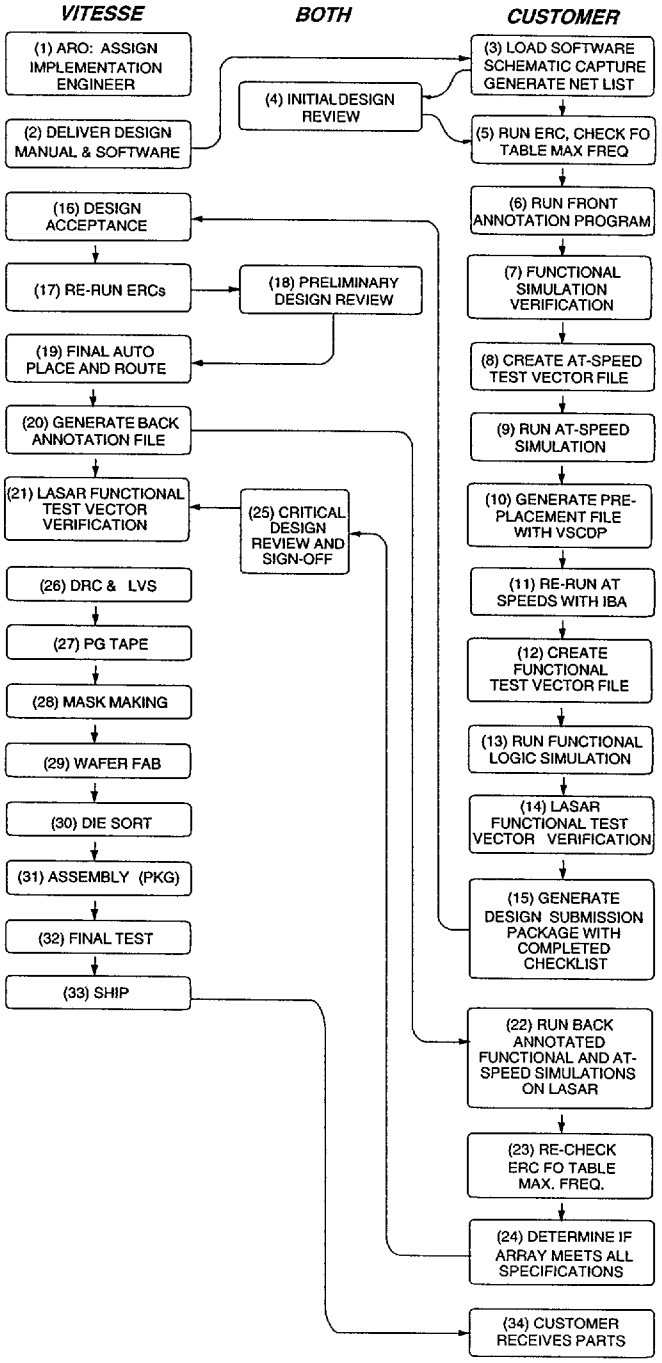
Figure 2: Gate Array Design Flow



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Option Development Procedure

Vitesse offers its customers the option of designing their own gate array, or having Vitesse engineers perform a turn-key implementation of the design based on mutually agreed specifications. In either case, a Vitesse implementation engineer is assigned to every customer to answer questions and track the progress of the design from start to finish. In addition, the following steps are normally performed by Vitesse engineers:

- Placement and routing of the design
- Net-length extraction
- Fan-out and metal delay calculation
- Final design rule checking and layout versus schematic verification

Through experience with many gate array designs, Vitesse has created a design automation framework and a well-defined flow for smooth implementation of customer designs. The flowchart on the previous page summarizes the typical gate array project flow and the various tasks delegated to the customer or to Vitesse. For complete details on development options refer to the FX/Viper Design Manual.

CAE/EDA Tools/Support

Viper designs are currently supported on Mentor, Synopsys, Cadence, and Viewlogic platforms. Cadence includes support for Composer and Verilog-XL. LASAR simulation software is used to verify the functional and AC performance of the design by accounting for on-chip timing variations. Macrocell libraries for the MOTIVE™ timing verifier from Quad Design are also available. A Vitesse Design Kit includes documentation and software to allow a designer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation after place and route. To facilitate floorplanning and block pre-placement, Vitesse has developed an interactive graphical pre-placement tool, supported in the X Windows™ environment, which the customer may use for their design. Cadence place and route tools are used for the actual physical implementation at Vitesse.

Training

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its' products specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent of the appropriate Vitesse officer is prohibited.

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