GENERAL DESCRIPTION

This IP Core has been developing for AFE(Analog-front-end) Function of Voice Signal Processing with 14bit 8KHz Voice Codec. The Core consists of 14bit linear monolithic PCM CODEC/transmit and receive band-pass filters utilizing the Sigma-Delta A/D and D/A conversion Architecture. It offers a number of programmable functions accessed through a serial control channel that easily interfaces to any classical micro controller. This IP Core is suitable for digital mobile phones, as cellular and cordless phones, or any battery powered equipment.

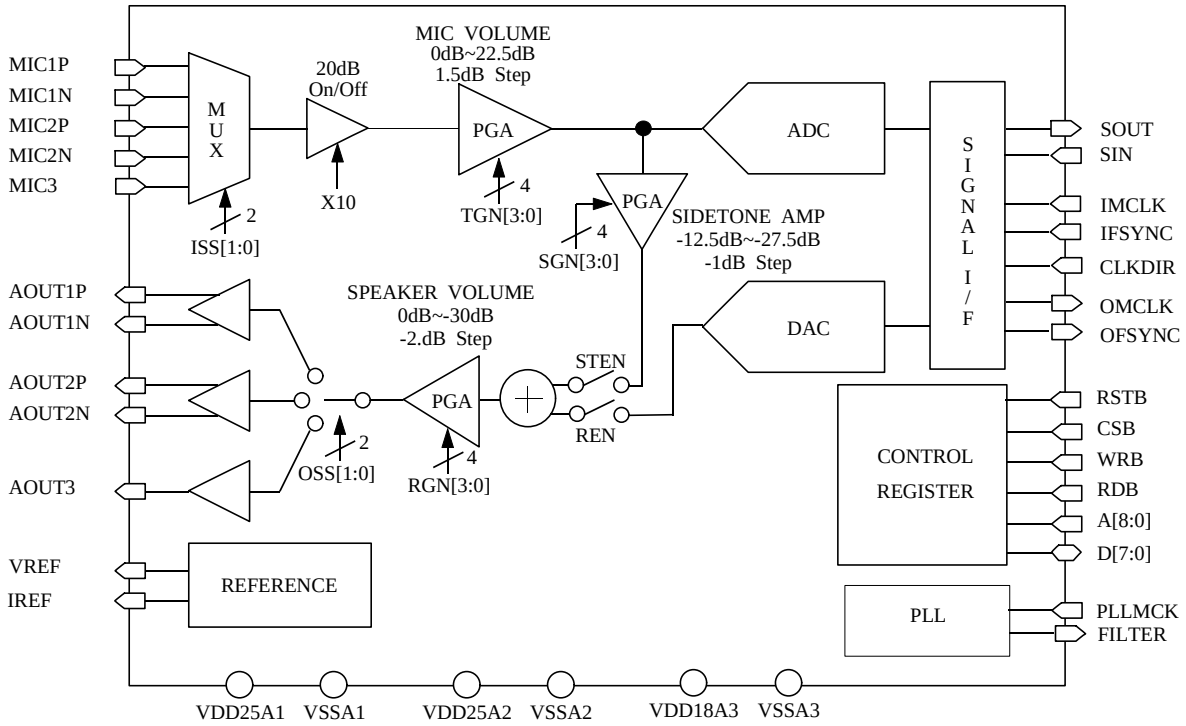
FEATURES

- Analog 2.5Volt / Digital 1.8Volt Operation
- Linear 14bit Codec
- 3 Mic Inputs (2 Differential and 1 Single)
- 3 Analog Ouptuts 32ohm Driver (2 Differential and 1 Single)
- Mic Volume 0dB ~ 22.5dB & 20dB Gain On/Off
- Speaker Volume 0dB ~ -30dB
- Sidetone -12.5dB ~ -27.5dB
- Serial Data Input, Output Format
- Control Register Interface for μ-Controller

APPLICATIONS

- CDMA

FUNCTIONALBLOCK DIAGRAM



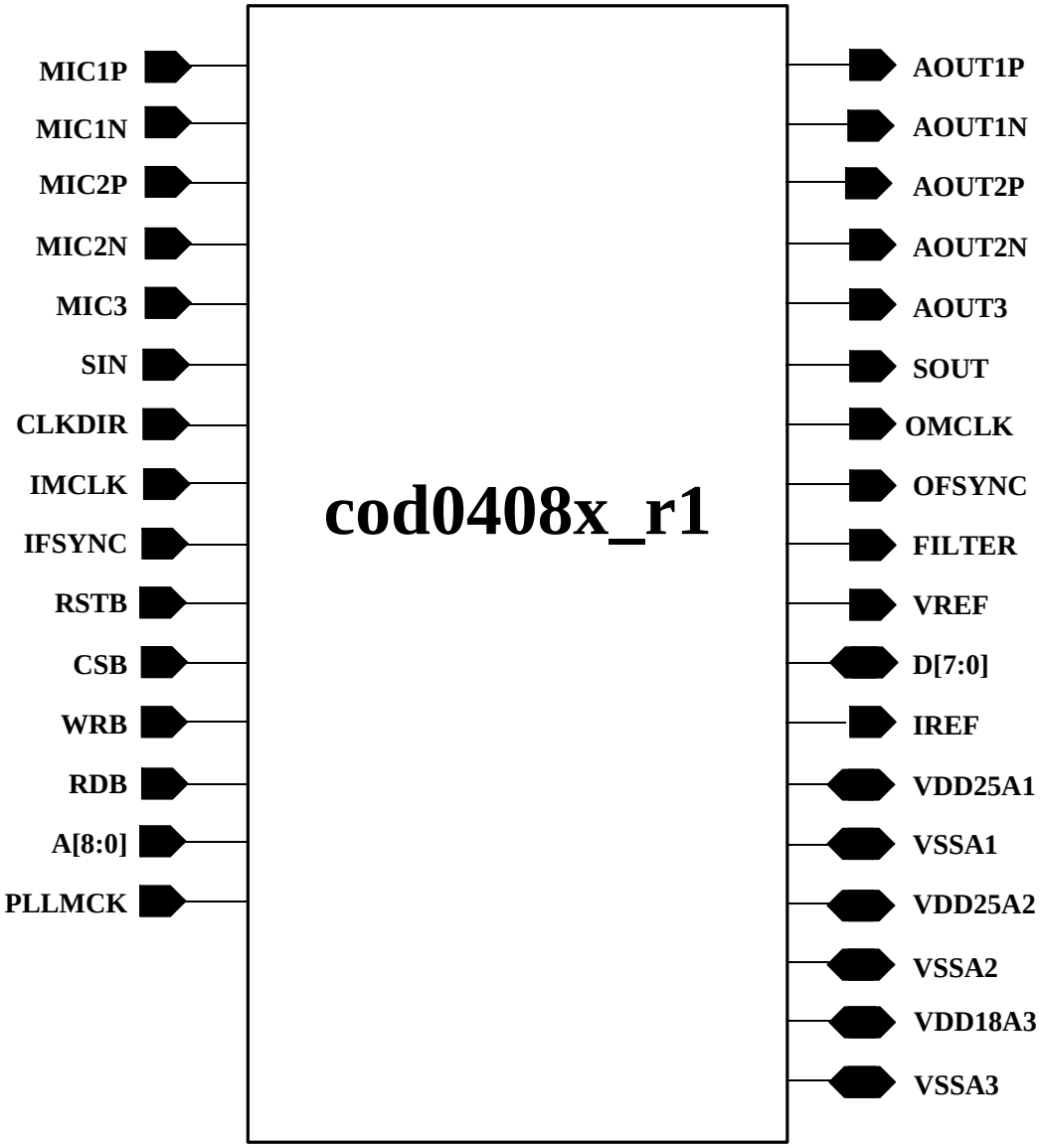
CORE PIN DIAGRAM

PIN NAME	Type	I/O Type	FUNCTION
Power Pins			
VDD25A1	P		Analog Power Supply 1 (2.5V)
VSSA1	G		Analog Ground 1
VDD25A2	P		Analog Power Supply 2 (2.5V)
VSSA2	G		Analog Ground 2
VDD18A3	P		Digital Power Supply 3 (1.8V)
VSSA3	G		Digital Ground 3
Analog Pins			
MIC1P	AI		Mic Input 1 Positive
MIC1N	AI		Mic Input 1 Negative
MIC2P	AI		Mic Input 2 Positive
MIC2N	AI		Mic Input 2 Negative
MIC3	AI		Mic Input 3 (Single Input)
AOUT1P	AO		Differential Output 1 Positive
AOUT1N	AO		Differential Output 1 Negative
AOUT2P	AO		Differential Output 2 Positive
AOUT2N	AO		Differential Output 2 Negative
AOUT3	AO		Single Output
VREF	AO		Reference Output
IREF	AO		Analog Current Control
FILTER	AO		PLL Loop Filter Control
Digital Pins			
SOUT	DO		ADC Serial Data Ouput
SIN	DO		DAC Serial Data Input
IMCLK	DI		Master Clock Input (If CLKDIR="L", IMCLK="L". If CLKDIR="H", IMCLK is Active (=2.048MHz))
IFSYNC	DI		Frame Sync Pulse Input (If CLKDIR="L", IFSYNC="L". If CLKDIR="H", IFSYNC is Active)
CLKDIR	DI		Master Clock /Frame Sync Pulse Active Direction Control Clock (If CLKDIR="L", OMCLK / OFSYNC is Active State. If CLKDIR="H", IMCLK / IFSYNC is Active State)
OMCLK	DO		Master Clock Output (If CLKDIR="L", OMCLK is Active.(=2.048MHz) If CLKDIR="H", OMCLK="L")
OFSYNC	DO		Frame Sync Pulse Output (If CLKDIR="L", OFSYNC is Active. If CLKDIR="H", OFSYNC="L")
RSTB	DI		Power-On-Reset and Reset Control Input (Low Active)
CSB	DI		Chip Select (Low Active)
WRB	DI		Write Enable (Low Active)
RDB	DI		Read Enable (Low Active)
A[8:0]	DI		Control Register Address
D[7:0]	DB		Control Register Data Input (WR is Enabled) Control Register Data Output (RD is Enabled)
PLLMCLK	DI		PLL Input Clock (=10MHz)

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional
- AP : Analog Power
- AG : Analog Ground
- DP : Digital Power
- DG : Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD25A1 VDD25A2 VDD18A3	2.5 2.5 1.8	V
Analog Input Voltage	-	VSSA1 to VDD25A1 VSSA2 to VDD25A2	V
Digital Input Voltage	-	VSSA3 to VDD25A3	V
Digital Output Voltage	V_{OH}, V_{OL}	VSSA3 to VDD25A3	V
Storage Temperature Range	Tstg	-45 to 125	°C

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5KΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD25A1,VDD25A2 VDD18A3	2.25 1.62	2.5 1.8	2.75 1.98	V V
Supply Voltage Difference	VDD25A1, VDD25A2, VDD18A3	-0.1	0.0	0.1	V
Digital Input Voltage		1.62	1.8	1.98	V
Analog Input Voltage			1.6		Vp-p
Operating Temperature	Topr	0	-	70	°C

NOTES

1. It is strongly recommended that all the supply pins (VDD25A1, VDD25A2) be powered from the same source to avoid power latch-up.

AC ELECTRICAL CHARACTERISTICS

(Measurement Bandwidth is 20Hz~4KHz. Full scale input sine wave 1KHz, FS=8KHz, @VDD25A1=2.5V, VDD25A2=2.5V, VDD18A3=1.8V Ta=25°C,Unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		-	14	-	Bits	
Sampling rate		-	8	-	KHz	-
ADC Characteristics						
* Signal to Distortion Ratio		-	65	-	dB	0dB Input : Linear
Offset Error		-	-	±20	mV	-
Input Voltage Range		-	1.6	-	Vpp	-

DAC Characteristics						
* Signal to Distortion Ratio		-	65	-	dB	0dB Input : Linear
Offset Error		.	.	±20	mV	-
Output Voltage Range		-	1.6 3.2	- -	Vpp Vpp	- Differential
PLL Characteristics						
Cycle Jitter		-	±100	-	ps	
Duty Ratio		-	45:55	-	%	
Lock Time		-	150	-	us	
Power Supply						
Power consumption (Operating Mode) Analog Digital			 6.5 0.5	 - -	 mA mA	 No load -
Power consumption (Power down mode)			50		uA	

TRANSMISSION CHARACTERISTICS

(Measurement Bandwidth is 60Hz~4KHz. Full scale, FS=8KHz, @VDD25A1=2.5V, VDD25A2=2.5V, VDD18A3=1.8V Ta=25° C ,,Unless otherwise specified.)

Characteristics	Test Condition	Min	Typ	Max	Unit
Transmit Gain Variation with Frequency	Relative to 1000Hz f = 60Hz f = 200Hz f = 300Hz f = 400Hz ~ 3000Hz f = 3400Hz] f = 4000Hz f = 8000Hz	 - - - - - - -	 - - - - - - -	 -7.9 -1.5 -0.6 -0.2 -1.1 -17.8 -62.8	 dB dB dB dB dB dB dB
Receive Gain Variation with Frequency	Relative to 1000Hz f = 60Hz f = 200Hz f = 300Hz f = 400Hz ~ 3000Hz f = 3400Hz] f = 4000Hz	 - - - 0.6 - -	 - - - - - -	 -8.2 -1.4 -0.6 -0.2 -0.7 -17.8	 dB dB dB dB dB dB
Transmit Delay	f = 60hz ~ 3000Hz	-	-	750	us
Receive Delay	f = 60Hz ~ 3000Hz	-	-	750	us

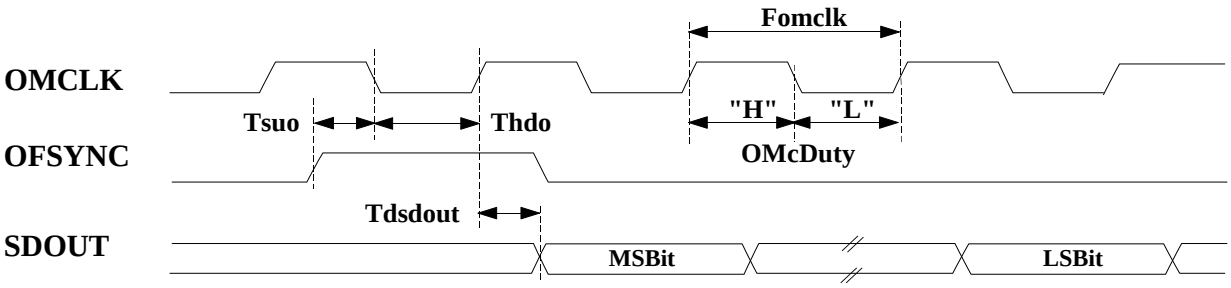
CONTROL CLOCKS CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
OMCLK Frequency	Fomclk	-	2.048	-	MHz
OMCLK Duty Cycle (H/L)	OMcDuty	-	50:50	-	%
OFSYNC Frequency	Fosync	-	8	-	KHz
OFSYNC High Period	Tosynch		488		ns
IMCLK Frequency	Fimclk	-	2.048	-	MHz
IMCLK Duty Cycle (H/L)	IMcDuty	-	50:50	-	%
IFSYNC Frequency	Fisync	-	8		KHz
IFSYNC High Period	Tisynch	244	488		ns

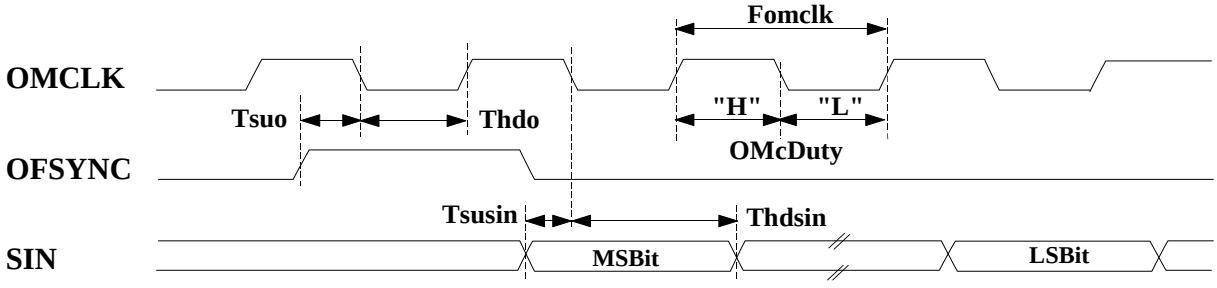
OMCLK Falling and OFSYNC SetUp	Tsuo	10	-	-	ns
OMCLK Falling and OFSYNC Hold	Thdo	10	-	-	ns
OMCLK Rising and SDOUT Delay	Tdsdout	-	-	10	ns
OMCLK Falling and SIN SetUp	Tsusin	10	-	-	ns
OMCLK Falling and SIN Hold	Thdsin	10	-	-	ns
IMCLK Falling and OFSYNC SetUp	Tsui	10	-	-	ns
IMCLK Falling and OFSYNC Hold	Thdi	10	-	-	ns
IMCLK Rising and SDOUT Delay	Tdsdout	-	-	10	ns
IMCLK Falling and SIN SetUp	Tsusin	10	-	-	ns
IMCLK Falling and SIN Hold	Thdsin	10	-	-	ns
WR Rising and A[8:0] SetUp	Tsuwra	20	-	-	ns
WR Rising and A[8:0] Hold	Thdwra	20	-	-	ns
WR Rising and DATA[7:0] SetUp	Tsuwrd	10	-	-	ns
WR Rising and DATA[7:0] Hold	Thdwrd	10	-	-	ns
RD Falling and A[8:0] SetUp	Tsurda	10	-	-	ns
RD Rising and A[8:0] Hold	Thdrda	20	-	-	ns
RD Falling and DATA[8:0] Delay	Tdrdf	-	-	10	ns
RD Rising and DATA[8:0] Delay	Tdrdr	-	-	10	ns

Timing Diagram

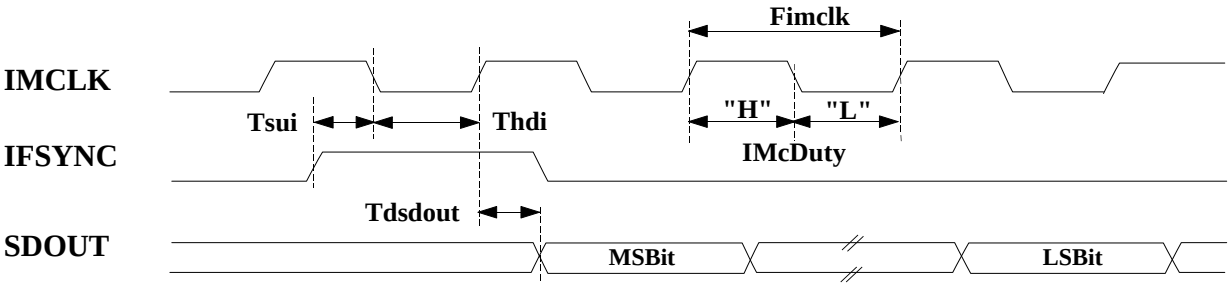
Serial Data Interface



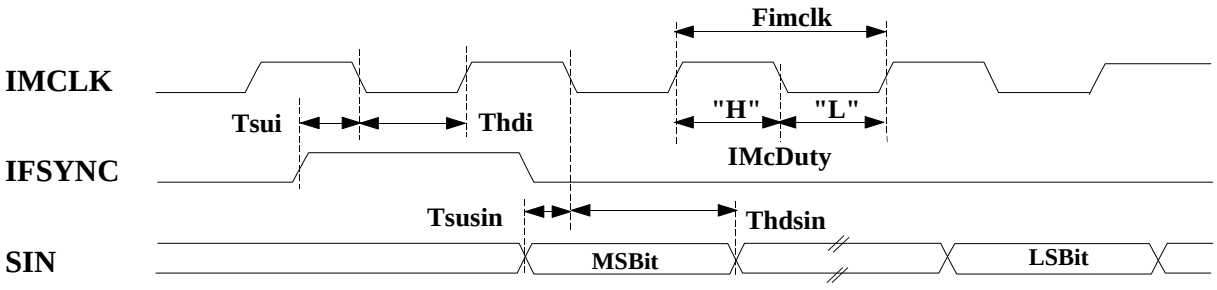
CODEC to Scom Timing (When CLKDIR="L")



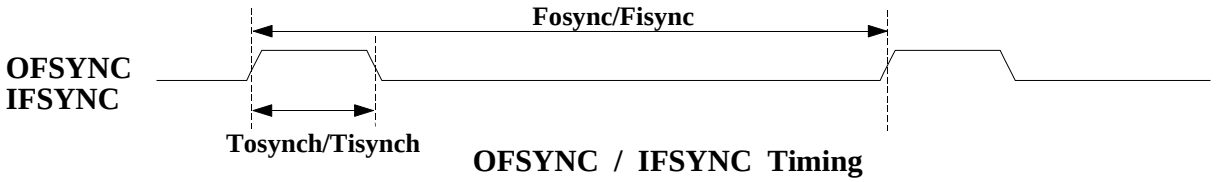
Scom to CODEC Timing (When CLKDIR="L")



CODEC to Scom Timing (When CLKDIR="H")

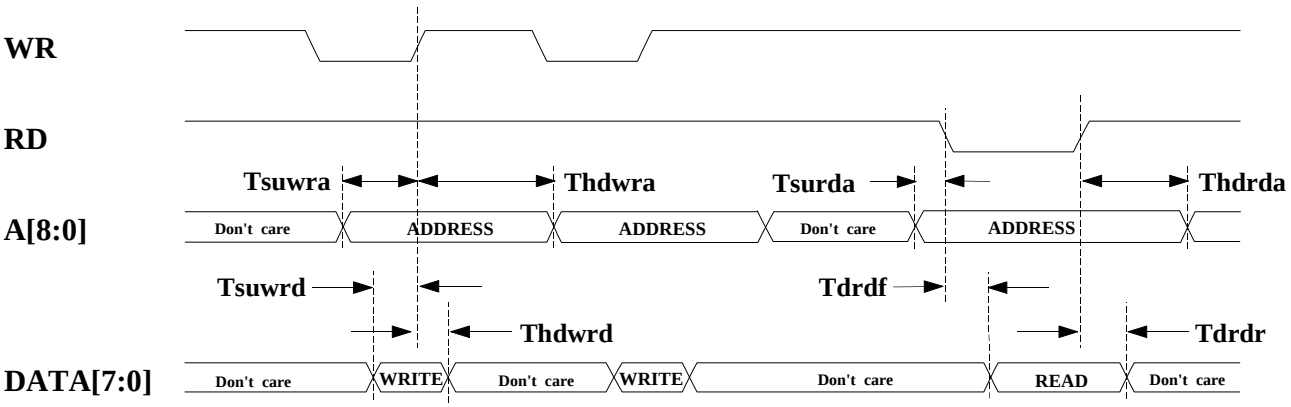


Scom to CODEC Timing (When CLKDIR="H")



OFSYNC / IFSYNC Timing

Control Register Interface



Programmable Functions

Control Register Mapping Table

ADDRESS	FUNCTION	DATA[7:0]							
A[8:0]		7	6	5	4	3	2	1	0
0D0h	Status	X	X	X	X	X	X	PLOCK	INIT
0D1h	Power Management	X	X	X	X	X	PW[2]	PW[1]	PW[0]
0D2h	Path Select	ISS[1]	ISS[0]	STEN	OSS[1]	OSS[0]	X	X	X
0D3h	Mic Volume	T20DB	X	X	X	TGN[3]	TGN[2]	TGN[1]	TGN[0]
0D4h	Speaker Volume	X	X	X	X	RGN[3]	RGN[2]	RGN[1]	RGN[0]
0D5h	Sidetone Volume	X	X	X	X	SGN[3]	SGN[2]	SGN[1]	SGN[0]
0D6h	Miscellaneous	X	X	X	X	X	X	CALDIS	DLB
0D7h	Test Path	X	TLBM	DIBYP	MOBYP	AMOPI	ABYP	ALBM	DLBM

Status Register (0D0H); Read Only

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	X	X	PLOCK	INIT	
							0	Under Initializing
							1	Initialize Done
						0		Not Lock
						1		PLL Lock Detected

Power Management (0D1H)

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	X	PW[2]	PW[1]	PW[0]	
					0	0	0	All Power Down (*)
					0	0	1	Standby Mode
					0	1	0	Rx Power Up, Tx Power Down
					0	1	1	Tx Power Up, Rx Power Down
					1	x	x	All Power Up

Path Selection (0D2H)

7	6	5	4	3	2	1	0	FUNCTION
ISS[1]	ISS[0]	STEN	OSS[1]	OSS[0]	REN	X	X	
0	0							All Muted (*)
0	1							MIC1P, MIC1N Selected
1	0							MIC2P, MICT2N Selected
1	1							MIC3 Selected

		0 1						Sidetone Disabled (*) Side Tone Enabled
			0 0 1 1	0 1 0 1				All Muted (*) AOUT1P, AOUT1N Selected AOUT2P, AOUT2N Selected AOUT3 Selected
					0 1			Rx path Disabled (*) Rx path Enabled

Mic volume control register (0D3H)

7	6	5	4	3	2	1	0	FUNCTION
T20DB	X	X	X	TGN[3]	TGN[2]	TGN[1]	TGN[0]	
0 1								0dB Selected (*) 20dB Selected
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	0dB Selected (*) 1.5dB Selected - 22.5dB Selected

Speaker Volume Control Register (0D4H)

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	RGN[3]	RGN[2]	RGN[1]	RGN[0]	
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	0dB Selected (*) -2dB Selected - -30dB Selected

Sidetone Volume Control Register (0D5H)

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	SGN[3]	SGN[2]	SGN[1]	SGN[0]	
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	-12.5dB Selected (*) -13.5dB Selected - -27.5dB Selected

Miscellaneous Control Register (0D6H)

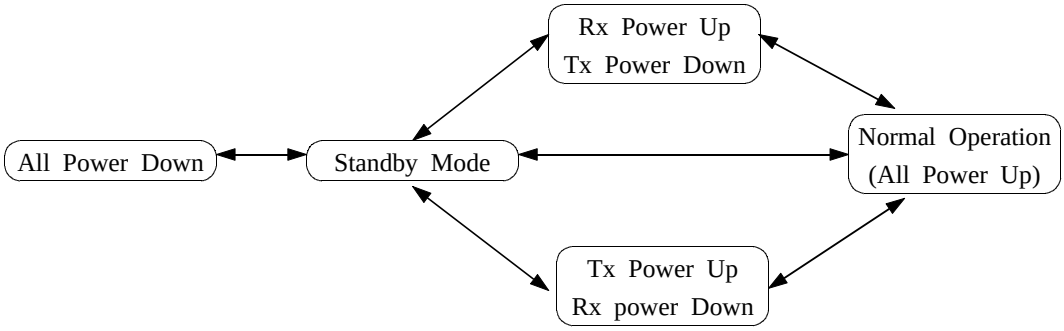
7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	X	X	CALDIS	DBYP	
						0 1		Calibration Function Enabled (*) Calibration Function Disabled
							0 1	Serial Data Loop Back Disabled (*) Serial Data Loop Back Enabled

Test Mode Control Register (0D7H)

7	6	5	4	3	2	1	0	FUNCTION
X	TLBM	DIBYP	MOBYP	AMOPI	ABYP	ALBM	DLBM	
	0							ADC/DAC Loop Mode disabled (*)
	1							ADC/DAC Loop Mode enabled
		0						Digital Decimator Filter Input Bypass Disabled (*)
		1						Digital Decimator Filter Input Bypass Enabled
			0					Digital Modulator Output Bypass Disabled (*)
			1					Digital Modulator Ourput Bypass Enabled
				0				Analog Moulator Output / Postfilter Input Bypass Disabled (*)
				1				Analog Moulator Output / Postfilter Input Bypass Enabled (*)
					0			Analog Bypass Disabled (*)
					1			Analog Bypass Enabled
						0		Analog Loop Back Disabled (*)
						1		Analog Loop Back Enabled
							0	Digital Loop Back Disabled (*)
							1	Digital Loop Back Enabled

Power Down/Up Mangement Guide

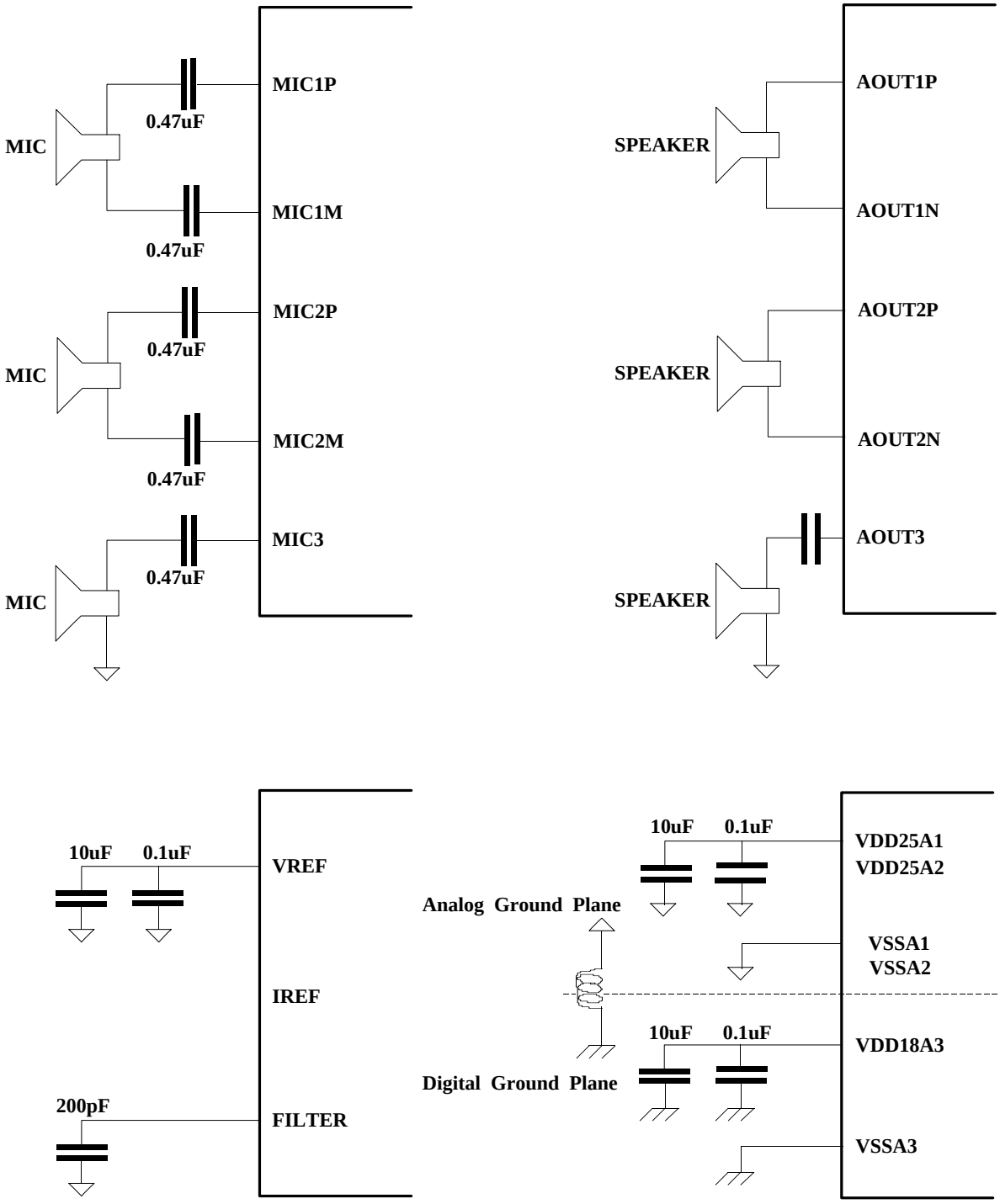
COD0408X_R1 is capable of operating at required power when no activity is required. The State of power



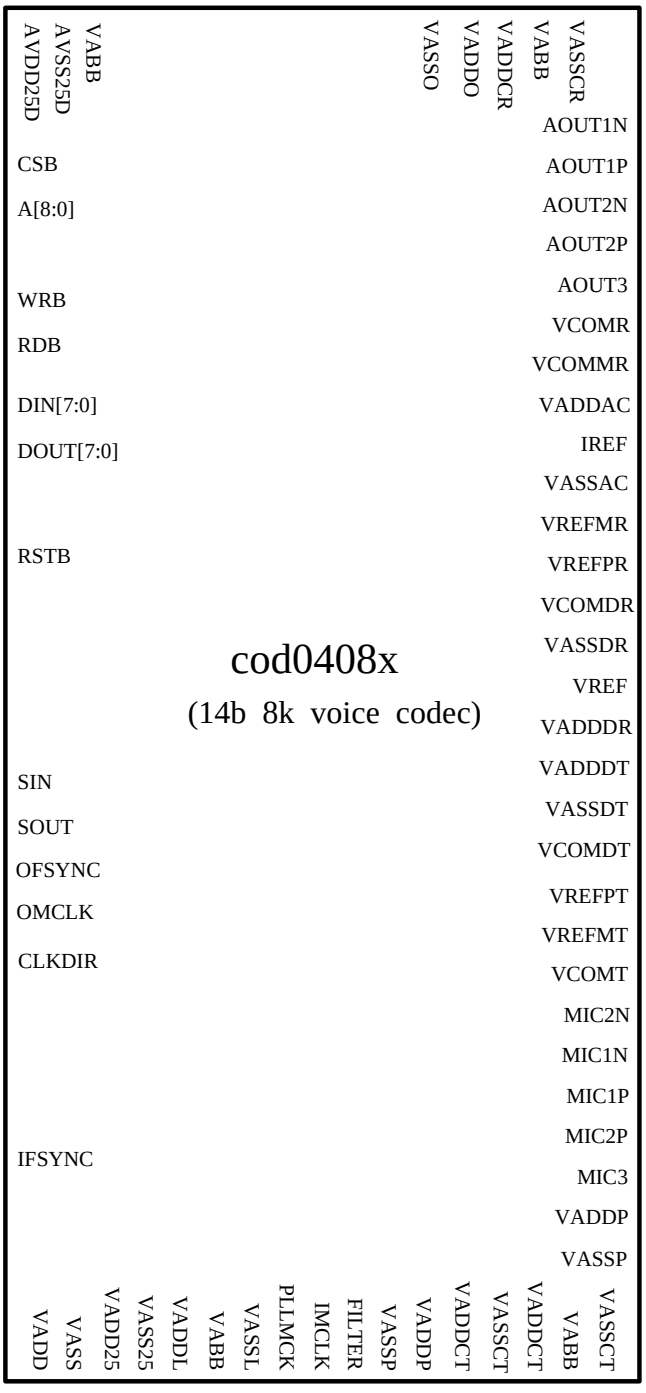
down/up is controlled by the Power Management Register(0D1H).

The above figure illustrates one example procedure a complete power down/up of COD0408X_R1. From normal operation sequential writes to the Power Management Register are preformed to power down/up COD0408X_R1 a piece at a time

CORE EVALUATION GUIDE



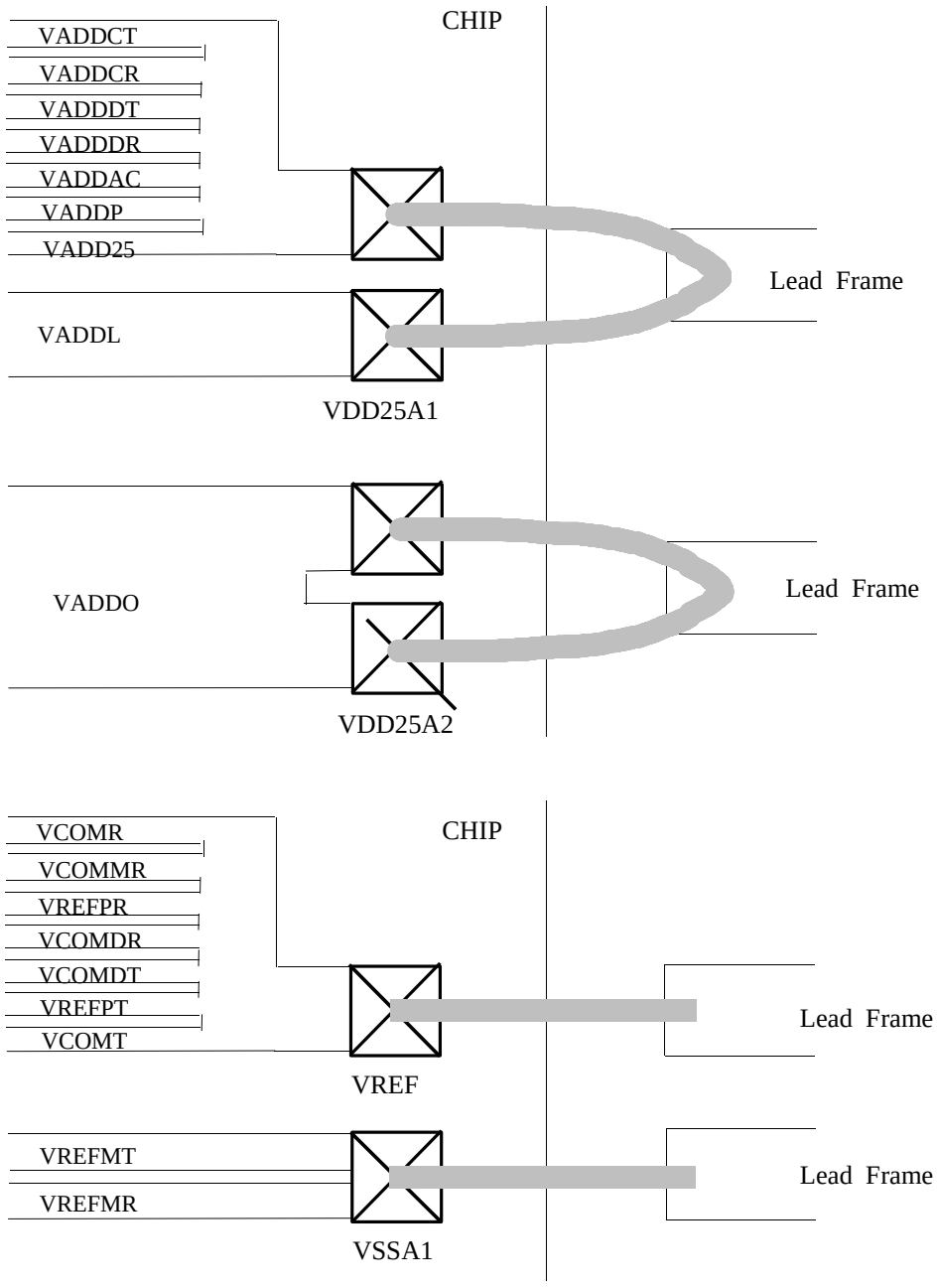
Phantom Cell



Pin Name	Pin Usage	Pin Layout Guide
VDD25A1	External	- Maintain the large width of lines as far as the pads. - Place the port positions to minimize the length of power lines. - Do not merge the analog powers with anoter power from other blocks. - Use good power and ground source on board.
VSSA1	External	
VDD25A2	External	
VSSA2	External	
VDD18A3	External	
VSSA3	External	
MIC1P	External	- Do not overlap with digtal lines. - Maintain the shotest path to pads.
MIC1N	External	
MIC2P	External	
MIC2N	External	
MIC3	External	
AOUT1P	External	
AOUT1N	External	
AOUT2P	External	
AOUT2N	External	
AOUT3	External	
VREF	External	- Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
IREF	External	
FILTER	External	
SOUT	External/ Internal	
SIN	External/ Internal	
IMCLK	External/ Internal	- Separate from all other analog signals
IFSYNC	External/ Internal	
CLKDIR	External/ Internal	
OMCLK	External/ Internal	- Separate from all other analog signals
OFSYNC	External/ Internal	
RSTB	External/ Internal	
CSB	External/ Internal	
WRB	External/ Internal	
RDB	External/ Internal	
A[8:0]	External/ Internal	
D[7:0]	External/ Internal	
PLLMCLK	External	

Layout Guide

* VDD25A1: VADDCT,VADDCR,VADDDT,VADDDR,VADDAC,VADDP,VADD25,VADDL
  (All Analog power are tied to VDD25A1)
* VSSA1: VASSCT,VASSCR,VASSDT,VASSDR,VASSAC,VASSP,VASS25,VASSL,VABB
  (All Analog Ground are tied to VSSA1)
* VDD25A2 = VADDO , VSSA2 = VASSO
* VADD connect to CDMA Power , VASS connect to CDMA Ground
* VCOMR, VCOMMR, VREFPR, VCOMDR, VCOMDT, VREFPT, VCOMT are tied to VREF
* VREFMR, VREFMT are tied to Analog Ground VSSA1



FEEDBACK REQUEST

It should be quite helpful to our CODEC core development if you specify your system requirements on CODEC in the following characteristic checking table and fill out the additional questions.
We appreciate your interest in our products. Thank you very much.

Could you explain external/internal pin configurations as required?

Specially requested function list :

1. What is your signal band to use, 3.6KHz? 4KHz? or 4.8KHz?
2. What is your analog in/output signal voltage swing? and what kind of format do your want as analog signal in/ouput: single or differential format? If you can, Please let us know, what is your exact in/output signal spec.
3. What is your minimum S/N+D spec?
4. Do you want linear phase characteristic or you don't care on digital filter spec?
5. Could you give us exact design spec of speech codec? (For example, A-law, μ-law and so on.)

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1..0	99.8.	Original version published	
Ver 1.1	Apr 2002	1. Phantom and layout guide added	