STANDARD MICROSYSTEMS CORPORATION

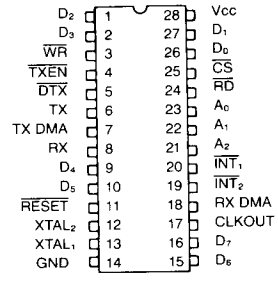
COM52C50
PRELIMINARY

TWINAX Interface Circuit (TIC)

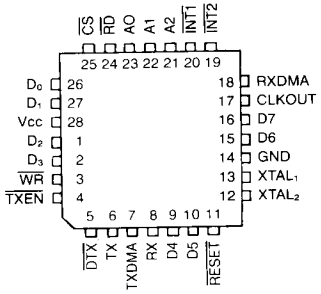
FEATURES

- ☐ Conforms to IBM® 5250 Standard used in IBM System /36 and /38.
- ☐ Operates at 1Mbps Data Rate
- ☐ Transmits and Receives Manchester II Encoded Data
- ☐ On Chip Odd or Even Parity Generation and Checking
- ☐ Programmable Interframe Zero Bit Insertion
- ☐ Handles Multi Byte and Single Byte Transfers
- ☐ Multiple Address Select Register Allows for Up to 7 Node Address Emulation
- ☐ Programmable Extended TX Enable
- ☐ Internal/External Loopback Capability for Self Test Diagnostics
- ☐ On Board Predistortion Circuitry
- ☐ Low Power CMOS
- ☐ On Board Crystal Oscillator Simplifies Clock Generation
- ☐ 8 MHz Clock Output for General Use
- ☐ Incorporates a Three Level Receive FIFO to Simplify Processor Interface
- ☐ Compatible with high speed microprocessor with no wait state up to 10 MHz (80186, 68000 etc...)
- ☐ Programmable DMA and Jump Vectoring Interface
- ☐ Independent RX DMA and TX DMA Request Signals
- ☐ Programmable Interrupt Selection
- ☐ 28 Pin Plastic Dual In Line and Chip Carrier Packages
- ☐ Open Drain Output on Interrupt Pins
- ☐ TTL Compatible Inputs and Outputs
- ☐ Single +5v Supply

PIN CONFIGURATION



PACKAGE: 28-pin DIP



PACKAGE: 28-pin PLCC

GENERAL DESCRIPTION

The COM52C50 TWINAX controller is a CMOS device that performs the communications interface to the IBM 5250 TWINAXIAL bus. It interfaces to a general purpose microprocessor on one side and to the IBM 5250 TWINAXIAL bus on the other side. The COM52C50 handles the parallel to serial and serial to parallel conversion of data to and from the TWINAXIAL bus and the encoding and decoding of data in Manchester II format. The COM52C50 consists of a RECEIVE BLOCK, a TRANSMIT BLOCK, and CONTROL circuitry. The Receive and Transmit sections of the COM52C50 are separate and may be used independent of one another. The COM52C50 generates and detects the bit sync, frame sync, parity, and the fill zero bit patterns according to the IBM 5250 standard.

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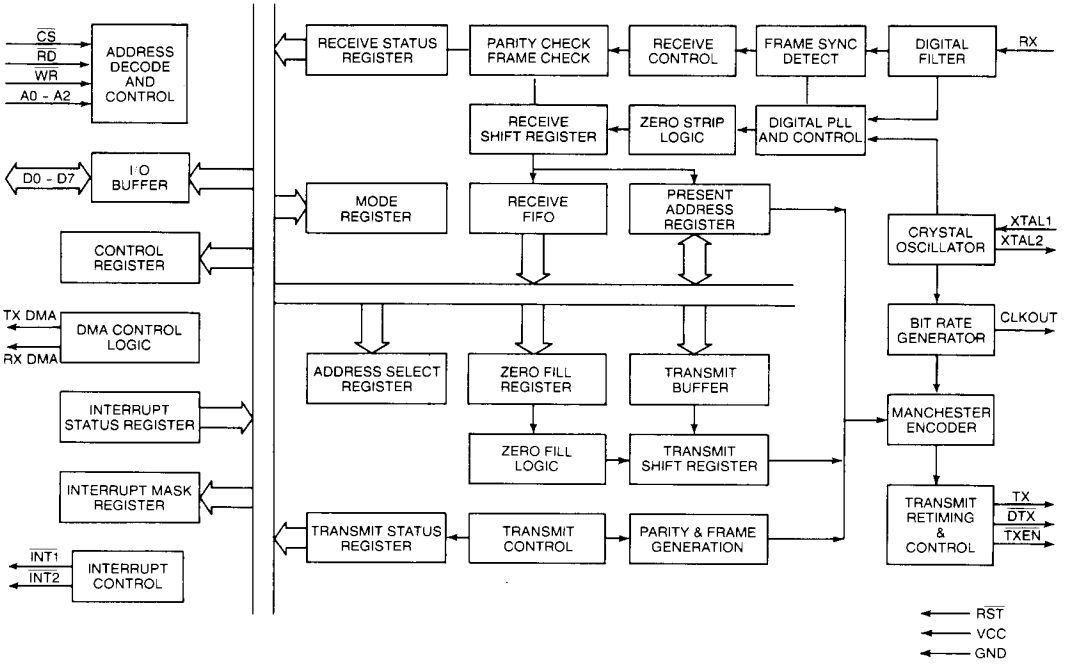


Fig. 1—COM52C50 INTERNAL BLOCK DIAGRAM

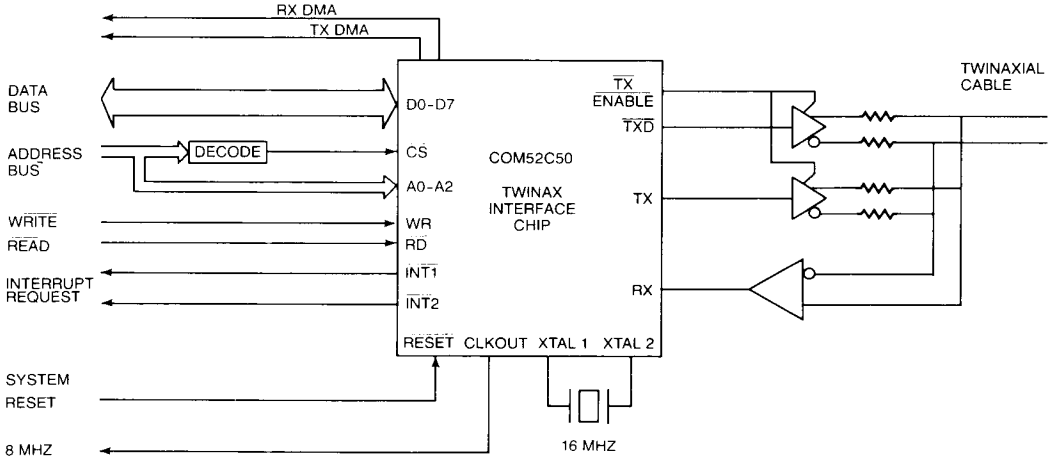


Fig. 2—TYPICAL COM52C50 INTERFACE

TABLE 1 - COM52C50 TWINAX DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1, 2, 9, 10, 15, 16, 26, 27	Bidirectional Data Bus	D_0-D_7	An 8 bit DATA BUS is used to interface the COM52C50 to the processor Data Bus.
3	Write Data Strobe	$\overline{WR}$	A low pulse on this input (when $\overline{CS}$ is low) enables the COM52C50 to accept the data or control information from the DATA BUS into the COM52C50.
4	TX Enable	$\overline{TX\ EN}$	This output is active low when the transmit data is valid. It is used to enable the external TX driver circuitry.
5	Delayed TX	$\overline{DTX}$	Delayed $\overline{TX}$ Manchester encoded.
6	TX Data	TX	Transmit data Manchester encoded.
7	TX Buffer	TX DMA	The TX Buffer Empty signal is used as a transmit DMA request.
8	RX Data	RX	This input accepts the receive Manchester II encoded bit stream.
11	Reset	$\overline{RST}$	This pin resets the COM52C50 to a known state. In addition, it disables the TX and puts an inactive state on the interrupt lines.
12 13	Crystal 2 Crystal 1	$XTAL_2$ $XTAL_1$	An external 16 MHz crystal is connected to these two pins. If an external 16 MHz TTL clock is used, it should be connected to $XTAL_1$ with a 390 ohm pullup resistor; $XTAL_2$ must be left floating.
14	Ground	GND	Ground
17	Clock Out	CLKOUT	This is a divide by two of the $XTAL_1$, 16 MHz input clock. It has a 50/50 duty cycle and can be used as a clock input to the host microprocessor.
18	RX Buffer	RX DMA	The RX Buffer Full signal is used as a receive DMA request.
19	Error Related Interrupt	$\overline{INT_2}$	This active low, open drain output provides the interrupt signal for error related operations.
20	Data Related Interrupt	$\overline{INT_1}$	This active low, open drain output provides the interrupt signal for data related operations.
21 22 23	Register Address Select	A_2 A_1 A_0	During processor to COM52C50 communications, these inputs are used to indicate which internal register will be selected for access by the processor.
24	Read Data Strobe	$\overline{RD}$	A low pulse on this input (when $\overline{CS}$ is low) enables the COM52C50 to place the data or status information on the DATA BUS.
25	Chip Select	$\overline{CS}$	A low level on this input enables the COM52C50 for reading and writing by the processor. When $\overline{CS}$ is high, the DATA BUS is in high impedance and the $\overline{WR}$ and $\overline{RD}$ will have no effect on the chip.
28	Power Supply	Vcc	+5V Power Supply.

FUNCTIONAL DESCRIPTION

RECEIVE BLOCK

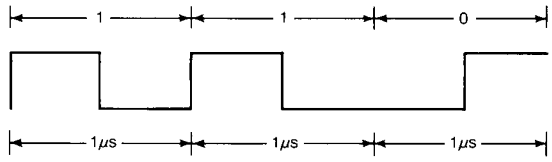
The COM52C50 recovers frames that conform to the IBM 5250 protocol. It also checks the received frame for proper sync, parity and trailing zeros. The RX input is sampled at 8 times the bit rate. The receive logic is brought into synchronization during bit and frame synchronization patterns. The internal receive clock is adjusted after each RX transition to compensate for bit jitter and distortion in the received data signal. In addition to the Receive Shift Register, the Receive block incorporates a two level First-in-First-out (FIFO) buffer. At the start of a message, the host microprocessor is alerted by handshake signals like Line Idle, Frame Sync Detect, Poll Command Detect, and Address Match. Thereafter, the RX Buffer Full signal informs the host microprocessor of the availability of received data. The end of a receive message is marked by either the detection of 1) End Of Message sequence 2) Line Idle or 3) Receive Error.

TRANSMIT BLOCK

The COM52C50 transmits data frames that conform to the IBM 5250 protocol. The transmit block consists of an 8 bit data buffer register, a present address register, 16 bit parallel to serial shift register, and parity generation logic. A transmit operation is initiated by loading the transmit buffer register. The transmitted frame will consist of the sync bit, the 8 bits loaded by the host microprocessor into the buffer register, the present address from the PRESENT ADDRESS REGISTER, or the (111) end of message code if the last frame is being transmitted, followed by a parity and three zero fill bits. After the host microprocessor loads the transmit buffer register, the TRANSMIT BUFFER EMPTY bit in the status register will become inactive. After a transfer of a data frame from the buffer register to the shift, register is accomplished, the TRANSMIT BUFFER EMPTY bit in the INTERRUPT AND TRANSMIT STATUS REGISTER becomes active.

BIT STREAM

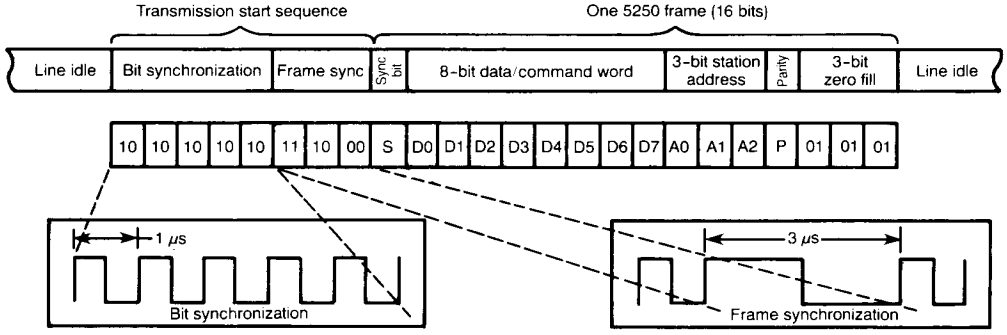
The bit stream is serially transmitted to (or received from) the System Unit at a transmission bit rate of 1 Mbps (±2%). Therefore, 1 microsecond is required for each bit, and 16 microseconds are required for each frame. All information between a station and the System Unit is transmitted on the twinaxial cable. The COM52C50 provides the transmitted serial data in Manchester encoded format where a "1" (one) bit is represented by a half bit cell of logical high followed by a half bit cell of logical low, and a 0 (zero) bit is represented by a half bit cell of logical low followed by a half bit cell of logical high. In addition, the COM52C50 provides a Delayed Transmit Data signal which is delayed by 1/4 of a bit time to simplify the interface to the external driver circuitry.



A message contains a bit sync pattern, a frame sync pattern, and a frame. The bit sync and the frame sync patterns establish synchronization between the station and the System Unit, and are transmitted prior to transmission of the first frame.

TABLE 2 - IBM 5250 FRAME FORMAT

The frame format for command and data to and from the IBM 5250 attachment is a fixed 16 bit frame. Only 13 bits contain information. The general format is as follows:



BIT	DESCRIPTION
0-2	These bits are always 0.
3	This is designated as the parity bit and will be set to ensure even parity in each frame.
4-6	These are the physical station address. Valid addresses are 000 to 110, and 111 is the end of message delimiter for the cable. A frame containing a 111 station address causes the station to ignore all following cable activity until a bit and frame synchronization is detected following a line turnaround. In addition, if only one frame is sent from the system unit, these bits represent the station address. If only one frame is sent from the work station, these bits are set to 111.
7-14	These bits contain command or data information. They represent a data byte or a status byte from the station, or they represent a data byte or a command from the system unit.
15	This is the sync bit. It is the first bit on the line and it is always set to 1.

RESETTING THE COM52C50

The COM52C50 must be reset on power up. This is accomplished by either of two methods: Hardware Reset or Software Reset.

Hardware Reset:

On the COM52C50 a $\overline{\text{RESET}}$ pin is dedicated to allow resetting of the device by applying a low level on the $\overline{\text{RST}}$ pin. The $\overline{\text{RESET}}$ signal should have a minimum duration of 1μs.

Software Reset:

The chip will also be reset when the Software Reset bit in the Control Register is asserted. The host microprocessor asserts Software Reset by writing a "zero" in bit 0 of the Control Register. To take the COM52C50 out of reset, the host microprocessor should write a "one" in bit 0 of the Control Register. Writes to the Control Register bit 0 should be spaced such that the Internal Reset signal has a minimum duration of 1μs.

Upon reset, all of the internal registers of the COM52C50 will be cleared. In addition, the COM52C50 enters an idle state in which it can neither transmit nor receive data. To disable undesired interrupts, the Interrupt Mask Register is set to 00 and the Status Registers bits are all inactive.

INITIALIZING THE COM52C50

Following RESET, the COM52C50 should be initialized by writing a valid bit pattern to the Interrupt Mask Register, the Mode Register, the Station Address Select Register. At this point, the Control Register can be used to enable Receive and Transmit.

TABLE 3 - REGISTER DECODE & TRUTH TABLE FOR INTERNAL REGISTER SELECT

ADDRESS	A2	A1	A0	$\overline{RD}$	$\overline{WR}$		
00	0	0	0	1	0	Mode Register	W
	0	0	0	0	1	Not Used	R
01	0	0	1	1	0	Interrupt Mask Register	W
	0	0	1	0	1	Interrupt Status Register	R
02	0	1	0	1	0	Address Select Register	W
	0	1	0	0	1	RX Status Register	R
03	0	1	1	1	0	Control Register	W
	0	1	1	0	1	RX Buffer	R
04	1	0	0	1	0	Zero Fill	W
	1	0	0	0	1	Not Used	R
05	1	0	1	1	0	Present Address Register	W
	1	0	1	0	1	Present Address Register	R
06	1	1	0	1	0	TX Buffer	W
	1	1	0	0	1	TX Status Register	R
07	1	1	1	1	0	TX Buffer EOM	W
	1	1	1	0	1	TX Status Register	R

REGISTER DESCRIPTIONS

RX BUFFER

This is the second level of a two byte deep Receive FIFO where the COM52C50 Receive Block provides new data and the microprocessor reads it. This register contains the 8 bit information field of an IBM5250 frame (bits 14-7). It is read by the host microprocessor after each frame reception which is indicated by the RX Buffer Full bit. This is an 8 bit read only register.

TX BUFFER

This register contains the 8 bit information field of an IBM5250 frame (bits 14-7). It is written to by the host microprocessor and contains the information to be sent out in the next frame. This is an 8 bit write only register.

ZERO FILL REGISTER

This eight bit register is loaded by the host microprocessor and contains the number of zero bits that should be filled between two frames. The host microprocessor would read a Set Mode Command and find out how many zero bytes must be padded on the next reply and then convert it to bits and write it to this register. The COM52C50 takes care of inserting the programmed number of zero bits between two frames. Up to 255 zero bits may be inserted in between frames. If no zero bit fill is required, this register should be cleared by writing a zero. The host microprocessor may not write to this register during data transmission. This register is cleared following RESET.

INTERRUPT MASK REGISTER

This is an 8 bit write only register which is loaded by the host microprocessor. This register controls interrupt generation on both the $\overline{INT1}$ and $\overline{INT2}$ interrupt pins. The most significant 5 bits enable the generation of $\overline{INT1}$, the least significant 3 bits enable the generation of $\overline{INT2}$.

$\overline{INT1}$

A logical one in a particular bit position will enable the corresponding bit in the Interrupt Status Register (bits 7-3) to cause an interrupt when it is set.

$\overline{INT2}$

A logical one in a bits (2-1-0) will enable bits (7-6-5) in the RX Status Register to cause an $\overline{INT2}$ interrupt when it is set.

Upon Reset, this register is cleared to all zeros thereby disabling interrupts. This is an 8 bit write only register.

ADDRESS SELECT REGISTER

This is an eight bit Write Only Register that controls address bit recognition of any of the seven possible node addresses. A node may emulate more than one address at a time by programming a "one" in the corresponding bit of the Address Register.

A "one" in any one or more of the Address Select bits allows the COM52C50 to respond to that group of addresses.

D7	D6	D5	D4	D3	D2	D1	D0
ONE	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Examples:

Emulate one address: (3)	1	0	0	0	1	0	0	0
Emulate four addresses: (6-4-3-0)	1	1	0	1	1	0	0	1
Emulate All Addresses: (6-5-4-3-2-1-0)	1	1	1	1	1	1	1	1

TABLE 4 - REGISTER DIAGRAMS

READ REGISTERS

ADDRESS	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00	**Not Used**								
01	**Interrupt Status Register**	frame sync detect	address match	poll command detect	RX buffer full	TX buffer empty	RX overrun error	RX biphase error	RX parity error
		← generate interrupt 1 →						← generate RX error →	
02	**RX Status Register**	RX Errors	line idle detect	end of message detect	RX buffer full	A2	A1	A0	zero
		← generate interrupt 2 →							
03	**RX Buffer**	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0
04	**Not Used**								
05	**Present Address Register**	zero	zero	zero	zero	zero	A2	A1	A0
06	**TX Status Register**	zero	zero	zero	zero	zero	TX underrun	TX buffer empty	zero
07	**TX Status Register**	zero	zero	zero	zero	zero	TX underrun	TX buffer empty	zero

WRITE REGISTERS

ADDRESS	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00	**Mode Register**	Test mode	auto EOM 111	.25μs 16μs TX en.	Test mode	TX parity	RX parity	internal external loop	loop / norm
01	**Interrupt Mask Register**	frame sync detect	address match	poll command detect	RX buffer full	TX buffer empty	RX errors	line idle detect	end of message detect
		← Interrupt 1 Mask →						← Interrupt 2 Mask →	
02	**Address Select Register**	one	A6	A5	A4	A3	A2	A1	A0
03	**Control Register**	reset errors	zero	disable biphase	enable TX DMA	enable RX DMA	enable TX	enable RX	software reset
04	**Zero Fill Register**	D7	D6	D5	D4	D3	D2	D1	D0
05	**Present Address Register**	zero	zero	zero	zero	zero	A2	A1	A0
06	**TX Buffer**	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0
07	**TX Buffer EOM**	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

PRESENT ADDRESS REGISTER

This register holds the present address information of the first frame following frame sync. It is used to convey the address information to the host microprocessor and has the address field information on all outgoing frames. This register is loaded by the Receive Block with the address information from the first frame following frame sync detect. This register can also be written to by the host microprocessor prior to initiating a Transmit sequence. The contents of this register are fed to the address compare logic which compares the Present Address to the Address Select Register. If a valid compare is detected, the Address Match bit in the Interrupt Status Register is set.

During a receive session, the contents of this register are valid only after the RX Buffer Full bit is set "one".

This is an eight bit read/write register.

TABLE 5—COM52C50 INTERRUPT STATUS REGISTER (BITS 0-7)

This is an eight bit register that can be read by the host microprocessor. The Interrupt Status Register is cleared following software or hardware reset. The bits in this register are used to indicate the following information:

BIT	DESCRIPTION
0	**RX PARITY ERROR** Signals the microprocessor that the frame received contained an incorrect number of binary "1" bits. This bit is set when the received frame has an incorrect parity bit and parity is enabled. This bit is cleared by: a. clearing RX Enable in the Control Register. b. setting Reset Errors in the Control Register. c. asserting internal RESET. d. asserting external hardware Reset.
1	**RX BIPHASE ERROR** Signals the microprocessor that a bit within a received frame has violated Biphase Manchester code (i.e. the two half bit cells of a bit were not complements). This bit is set when a Biphase error occurs during bits 0-15 of a frame. This bit is cleared by: a. clearing RX Enable in the Control Register. b. setting Reset Errors in the Control Register. c. asserting internal RESET. d. asserting external hardware Reset.
2	**RX OVERRUN ERROR** Signals the microprocessor that an Overrun condition has occured. This bit is set when a byte stored in the Receive Holding Register is overwritten with a new byte from the Receive Shift Register before the microprocessor has read the Receive Holding Register. This bit is cleared by: a. clearing RX Enable in the Control Register. b. setting Reset Errors in the Control Register. c. asserting Internal RESET. d. asserting External Hardware Reset. e. Frame Sync Detect going active.
3	**TX BUFFER EMPTY** Signals the processor that the Transmit Character Buffer is empty and that the COM52C50 can accept a new character for transmission. This bit is set when a character has been loaded from the Transmit Holding Register to the Transmit Shift Register. This bit is cleared by: a. writing to the Transmit Buffer Register b. clearing TX Enable in the Control Register c. asserting internal RESET. d. asserting external hardware Reset. This bit is initially set when the transmitter logic is enabled by setting the TXenable bit in the Control Register (also TX BUFFER is empty because of reset). Data can be overwritten if a consecutive write is performed while TX buffer empty is zero.
4	**RX BUFFER FULL** Signals the processor that a completed character is present in the Receive Buffer Register for transfer to the processor. This bit is set when a character has been loaded from the receive deserialization logic to the Receive Holding Register. This bit is cleared by: a. reading the Receive Holding Register b. clearing RX Enable in the Control register c. Frame Sync Detect going active d. asserting internal RESET. e. asserting external hardware Reset.

TABLE 5—COM52C50 INTERRUPT STATUS REGISTER (BITS 0-7) CONTINUED

BIT	DESCRIPTION
5	**POLL COMMAND DETECTED** Signals the microprocessor that the command in the Receive Holding Register is a POLL command. (xxx10000) This bit is set when the first frame following Frame Sync has the binary 10000 pattern in the least significant 5 bits of the data section. This bit is cleared by: a. reading the RX Buffer Register when RX Buffer Full is set. b. Frame Sync Detect going active. c. asserting internal RESET. d. asserting external hardware Reset.
6	**ADDRESS MATCH** Signals the microprocessor that a match has occured between the address field of the first frame following Frame Sync and any bit within the Address Select Register. This bit is set after a valid compare has occured between the address field of the first frame following frame sync and any bit of the Address Select Register. This bit is cleared by: a. reading the RX Buffer Register when RX Buffer Full is set. b. Frame Sync Detect going active. c. asserting internal RESET. d. asserting external hardware Reset.
7	**FRAME SYNC DETECTED** Signals the microprocessor that a Frame Sync has been detected on the RX pin of the COM52C50. The Frame Sync detect circuitry checks for one "1" bit (10 half bit) followed by a three half bit times of ones followed by a three half bit times of zeros (111000). This bit is set when a Valid Frame Sync pattern is detected. This bit is cleared by: a. reading the Interrupt Status Register. b. Line Idle going active. c. asserting internal RESET. d. asserting external hardware Reset.

RESETTING OF INTERRUPTS

The $\overline{INT1}$ and $\overline{INT2}$ signals feature an automatic interrupt acknowledge that will take interrupt away when the proper action is taken by the processor. The following describes how each of the eight interrupting conditions get cleared.

When the interrupt is caused by:	The interrupt is cleared by:
Frame Sync Detect	Reading the Interrupt Status Register twice Line Idle going active Internal Reset External Reset
Address Match	Frame Sync Detect Reading the RX Buffer Register when the RX Buffer is full Internal Reset External Reset
Poll Command Detect	Frame Sync Detect Reading the RX Buffer Register when RX Buffer is full Internal Reset External Reset
RX Buffer Full	Clearing the RX Enable bit Reading the RX Buffer Register when the RX Buffer is full Internal Reset External Reset
TX Buffer Empty	Writing to the TX Buffer Register Clearing the TX ENable bit Internal Reset External Reset
RX Errors	Asserting Reset Errots Clearing RX Enable Internal Reset External Reset
Line Idle Detect	Reading the RX Status Register twice Internal Reset External Reset
End of Message (EOM) Detect	Reading the RX Status Register twice Internal Reset External Reset

TABLE 6—COM52C50 RX STATUS REGISTER (BITS 0-7)

This is an eight bit register that can be read by the host microprocessor. The bits in this register are used to indicate the following information:

BIT	DESCRIPTION
0	**FIXED ZERO**
1-3	**PRESENT ADDRESS BIT 0-1-2** These three bits hold the value of the Present Address. They are the same as the bits 1, 2, 3, of the Present Address Register.
4	**RX BUFFER FULL** Signals the processor that a completed character is present in the Receive Buffer Register for transfer to the processor. This bit is set when a character has been loaded from the receive deserialization logic to the Receive Buffer Register. This bit is cleared by: a. reading the Receive Buffer Register b. clearing RX Enable in the Control register c. Frame Sync Detect going active d. asserting internal RESET e. asserting external hardware RESET
5	**LAST FRAME/End Of Message (EOM)** Signals the microprocessor that a "1 1 1" pattern has been detected in the address field of an incoming frame. This bit is propagated through the RX FIFO logic and it corresponds to the data byte immediately available to the processor. This bit is set when the 3 bit address field of a frame gets a match with a constant "1 1 1" pattern. This bit is cleared by: a. Frame Sync Detect going active. b. clearing RX Enable in the Control Register. c. asserting internal RESET. d. asserting external hardware RESET
6	**LINE IDLE** Signals the microprocessor that the RX line has not seen a transition for the past 3μs time interval. This can be used by the microprocessor to learn that the RX line is idle. This bit is set when the RX line remains idle for a 3 microseconds duration. This bit is cleared by: a. activity on the RX line. b. clearing RX Enable in the Control Register c. asserting Internal RESET. d. asserting External Hardware Reset.
7	**RX ERRORS** Signals the microprocessor that a Receive Error condition has occured. This bit is set when any one or both of the Interrupt Status Register bits 0 and 1 are set. This bit is cleared by: a. asserting Reset Errors in the Control Register b. clearing RX Enable in the Control Register. c. asserting Internal Software RESET. d. asserting External Hardware RESET.

TABLE 7—COM52C50 TX STATUS REGISTER (BITS 0-7)

BIT	DESCRIPTION
0	**Fixed at Zero**
1	**TX BUFFER EMPTY** Signals the processor that the Transmit Buffer Register is empty and that the COM52C50 can accept a new character for transmission. This bit is set when a character has been loaded from the Transmit Buffer Register to the Transmit Shift Register. This bit is cleared by: a. writing to the Transmit Buffer Register b. clearing TX Enable in the Control Register c. asserting internal software RESET. d. asserting external hardware RESET. This bit is initially set when the transmitter logic is enabled by setting the TXenable bit in the Control Register. Data can be overwritten if a consecutive write is performed while TX buffer empty is "zero".
2	**TX UNDERRUN ERROR** Signals the microprocessor that an Underrun condition has occured. This bit is set when, during a transmission process, the microprocessor writes to the TX Holding Register after the TX Shift Register has already shifted its last bit out. This bit is cleared by: a. clearing TX Enable in the Control Register. b. setting Reset Errors in the Control Register. c. asserting Internal RESET. d. asserting External Hardware RESET.
3-7	These bits are fixed zeros.
The TX Status Register is cleared following software or hardware reset.	

TABLE 8—COM52C50 CONTROL REGISTER (BITS 0-7)

The Control Register is an eight bit write only register that is used by the microprocessor to control the COM52C50. Following External Reset all bits of the Control Register are cleared to "zero" except for the Software Reset bit. Internal Reset does not affect any of the Control Register bits. The bits of the Control Register are defined as follows:

BIT	DESCRIPTION
0	**SOFTWARE RESET** This bit is used by the microprocessor to reset the COM52C50 via a software command. When this bit is cleared, Internal Reset is asserted and the COM52C50 is reset. This bit should be set to "one" during normal operations.
1	**ENABLE RECEIVE** This bit is used by the microprocessor to enable the Receive Logic in the COM52C50 to function. When this bit is cleared, the RX BUFFER FULL bit in the Status Register will be disabled. This bit should be set to "one" during normal operations.
2	**ENABLE TRANSMIT** Data transmission cannot take place via the COM52C50 unless this bit is set to logic "one". When this bit is reset (disabled), transmission will be disabled only after the previously written data has been transmitted. (This simply disables loading of the TX Buffer Register).
3	**ENABLE RX DMA** This bit, when set, will enable the RX DMA handshake signal on the COM52C50. When this bit is cleared, the RX DMA signal on the COM52C50 is kept low.
4	**ENABLE TX DMA** This bit, when set, will enable the TX DMA handshake signal on the COM52C50. When this bit is cleared, the TX DMA signal is kept low.
5	**DISABLE BIPHASE ERRORS** This bit, when set, will disable the detection of biphase errors in the receive block. This bit is cleared upon power up and biphase error detection is enabled.
6	**NOT USED—MUST BE ZERO**
7	**RESET ERRORS** This bit, when set, will clear the Receive Error Status bits in the Interrupt Status Register (Parity, Biphase, Overrun). As a result of this, the RX Error bit in the RX Status Register will be cleared. Reset Errors also resets the TX Underrun status bit in the TX Status Register. No latch is provided in the Control Register for saving the state of this bit; therefore there is no need for clearing it.

THE COM52C50 ON CHIP CRYSTAL OSCILLATOR

The COM52C50 incorporates an on chip crystal oscillator. A 16 MHZ parallel resonant crystal is connected to the XTAL1 and the XTAL2 pins of the COM52C50 along with a 1.0 MOhm resistor across the crystal and two 22pf capacitors from each node of the crystal to ground. (see figure 18, CONNECTION DIAGRAM FOR PARALLEL RESONANT CRYSTAL)

A TTL clock can also be used to supply the clock signal to the COM52C50. This is done by supplying a TTL level clock to the XTAL1 pin of the COM52C50 along with a 390 ohm resistor from the XTAL1 pin to Vcc. The XTAL2 pin should not be connected when an external clock is supplied. (see figure 19, RECOMMENDED EXTERNAL TTL CLOCK CONNECTION)

DMA OPERATION

The COM52C50 features two independent DMA Request signals. These signals are provided to allow the COM52C50 to interface to one or two channels of a DMA controller such as that of the 80188 and the 80186. Each of the RX DMA and TX DMA request signals can be individually enabled via software commands in the Control Register. DMA interface is most useful when moving blocks of data following an activate read or an activate write command.

RX DMA

Following an active read command, the host microprocessor would initialize the RX DMA channel and enable RX DMA by writing a one in the Control Register bit 3. The COM52C50 will automatically generate the RX DMA Request signal as soon as a received frame is moved from the Receiver Shift Register to the Receiver FIFO. At this time, the DMA channel will initiate a Read Receive Buffer cycle which in turn will be used as an automatic DMA Acknowledgment. When a new frame arrives and is ready to be read by the DMA channel, the COM52C50 will assert the RX DMA Request signal and inform the DMA channel of the availability of the next word. The Receiver FIFO will be in use during DMA operations. This gives the DMA channel a maximum of three frame times for DMA latency. On the average, however, the DMA channel must be able to keep up with the COM52C50 byte rate.

TX DMA

When transmitting blocks of data, the host microprocessor would initialize the TX DMA channel and enable TX DMA by writing a one in the Control Register bit 4. The COM52C50 will automatically generate the TX DMA Request signal when the TX Buffer is empty. When the DMA channel performs a write cycle to the COM52C50 TX Buffer, the TX DMA Request signal will be inactive until the TX Buffer becomes empty again. After writing the last data frame to the TX Buffer, the host microprocessor can disable the TX DMA Request signal by writing to the Control Register.

TABLE 9—COM52C50 MODE REGISTER DESCRIPTION (BITS 0-7)

BIT	DESCRIPTION
0	**NORMAL/LOOPBACK MODE** This bit when set will put the COM52C50 in loopback mode. When in loopback mode, bit 1 of the Mode Register specifies Internal or External loopback modes. 0 NORMAL OPERATION 1 LOOPBACK MODE
1	**EXTERNAL/INTERNAL LOOPBACK** This bit specifies External or Internal loopback Modes. When bit 0 of the Mode Register specifies normal mode of operation, this bit is a don't care. 0 EXTERNAL LOOPBACK 1 INTERNAL LOOPBACK
2	**EVEN/ODD RX PARITY** This bit specifies Even or Odd parity for the receive section of the COM52C50. 0 EVEN RX PARITY 1 ODD RX PARITY
3	**EVEN/ODD TX PARITY** This bit specifies Even or Odd parity for the transmit section of the COM52C50. 0 EVEN TX PARITY 1 ODD TX PARITY
4	**NORMAL/TEST MODE** This bit when set puts the COM52C50 in a VLSI test mode. This bit is cleared upon Reset and should be cleared for normal operation. 0 NORMAL OPERATION 1 TEST MODE
5	**TX ENABLE 250ns/16μs** This bit controls the amount of time the Transmit Enable Signal will remain active after the last TX bit is shifted out. When set to "zero", the TX Enable signal goes inactive after 250ns following the last TX data bit. When set to "one", the TX Enable signal goes inactive after 16μs following the last TX data bit. This can be used to drive the Twinax Cable after a transmission in order to reduce line reflection effect. 0 TX enable 250ns 1 TX enable 16μs
6	**EOM/Auto 111** This bit determines if Automatic 111 address should be inserted on a transmitted message upon transmitter underrun. When this bit is a "zero", the microprocessor has to write to TX Buffer EOM to force a 111 address on the last frame of transmitted data. 0 EOM 111 1 Auto 111
7	**NORMAL/TEST MODE** This bit when set puts the COM52C50 in a VLSI test mode. This bit is cleared upon Reset and should be cleared for normal operation. 0 NORMAL OPERATION 1 TEST MODE

Following RESET, the mode register will be cleared to all "zero's" and the default Mode Setting will be:

BIT 0 - 0 NORMAL OPERATION
BIT 1 - 0 EXTERNAL LOOPBACK
BIT 2 - 0 EVEN RX PARITY
BIT 3 - 0 EVEN TX PARITY
BIT 4 - 0 NORMAL OPERATION
BIT 5 - 0 TX ENABLE .250
BIT 6 - 0 EOM 111
BIT 7 - 0 NORMAL OPERATION

ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... -55 to 150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... V_{cc} + 0.3V
Negative Voltage on any pin, with respect to ground ..... -0.3V
Maximum V_{cc} ..... +7.0V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or any other condition above those indicated in the operational sections of this specifications is not implied.

NOTE: When powering this device from the laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

TABLE 11-ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, Vcc = +5V ±5%.)

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

FIG. NO.	PARAMETER	SYMBOL	MIN	TYP*	MAX	UNITS	COMMENTS
	DC CHARACTERISTICS						
	LOW INPUT VOLTAGE	$V_{IL\ 1}$			0.8	V	Except TLL Input Clock
	HIGH INPUT VOLTAGE	$V_{IH\ 1}$	2.0			V	Except TTL Input Clock
	LOW INPUT VOLTAGE	$V_{IL\ 2}$			1.0	V	TTL Clock Input
	HIGH INPUT VOLTAGE	$V_{IH\ 2}$	Vcc-0.5V			V	TTL Clock Input
	LOW OUTPUT VOLTAGE	$V_{OL\ 1}$			0.4	V	I_{OL} = 3.5ma
	HIGH OUTPUT VOLTAGE	$V_{OH\ 1}$	2.4			V	I_{OH} = 200μa
	LOW OUTPUT VOLTAGE	$V_{OL\ 2}$			3.0	V	For Clock Output
	HIGH OUTPUT VOLTAGE	$V_{OH\ 2}$	3.0			V	For Clock Output
	INPUT LEAKAGE CURRENT	I_L		±10		μA	
	INPUT CAPACITANCE	C_{IN}		25		pF	
	POWER SUPPLY CURRENT	I_{CC}		20	30	mA	

FIG. NO.	PARAMETER	SYMBOL	MIN	TYP*	MAX	UNITS	COMMENTS
	AC CHARACTERISTICS						
	WRITE CYCLE						
Fig. 3	Address Setup Time	t_1	50			ns	
Fig. 3	Address Hold Time	t_2	0			ns	
Fig. 3	$\overline{WR}$ Pulse Width	t_3	150			ns	
Fig. 3	Data Setup Time	t_4	75			ns	
Fig. 3	Data Hold Time	t_5	10			ns	
	READ CYCLE						
Fig. 4	Address Setup Time	t_6	50			ns	
Fig. 4	Address Hold Time	t_7	0			ns	
Fig. 4	$\overline{RD}$ Pulse Width	t_8	150			ns	
Fig. 4	T_{zx}	t_9	0		80	ns	
Fig. 4	T_{xz}	t_{10}	0		80	ns	
Fig. 5	READ WRITE INTERVAL	t_{13}	100			ns	
	INTERRUPT ACKNOWLEDGE TIMING						
Fig. 6	Read Int. Status Reg. to INT inactive	t_{14}		300		ns	
	DMA ACKNOWLEDGE TIMING						
Fig. 7	Read RX Buffer to PXDMA inactive	t_{15}		200		ns	
Fig. 8	Write TX Buffer to TXDMA inactive	t_{16}		200		ns	

FIG. NO.	SYMBOL PARAMETER	SYMBOL	MIN.	TYP*	MAX	UNITS	COMMENTS
	TTL CLOCK INPUT TIMING						
Fig. 9	Input Clock fall time	t_{20}			10	ns	
Fig. 9	Input Clock rise time	t_{21}			10	ns	
Fig. 9	Input Clock high time	t_{22}	20			ns	Vcc-1.0V
Fig. 9	Input Clock low time	t_{23}	20			ns	@0.6 V
Fig. 9	Input Clock period	t_{24}		62.5		ns	@1.5 V
	CLOCK OUT TIMING						
Fig. 10	Clock Out fall time	t_{25}			10	ns	@50pF max
Fig. 10	Clock Out rise time	t_{26}			10	ns	@50pF max
Fig. 10	Clock Out high time	t_{27}	55			ns	@50pF max
Fig. 10	Clock Out low time	t_{28}	55			ns	@50pF max
Fig. 10	Clock Out period	t_{29}		125		ns	@50pf max
	TX DATA TIMING						
Fig. 11	$\overline{WR}$ to tx Buffer $\overline{TX\ ENABLE}$	t_{30}		1500		ns	
Fig. 11	$\overline{TX\ ENABLE}$ active to TX DELAY	t_{31}		250		ns	
Fig. 11	$\overline{DTX}$ to $\overline{TX\ ENABLE}$ inactive	t_{32}		250		ns	
Fig. 11	TX to $\overline{DTX}$ delay	t_{33}		250		ns	
Fig. 11	TX, $\overline{DTX}$ half bit cell	t_{34}		500		ns	
Fig. 11	TX, $\overline{DTX}$ full bit cell	t_{35}		1000		ns	
Fig. 11	TX, $\overline{DTX}$ rise time				10	ns	
	TX, $\overline{DTX}$ fall time				10	ns	
	RX DATA TIMING						
	RX half bit cell pulse width			500		ns	(Jitter Tolerance ±20%)
	RX bit cell pulse width			1000		ns	
	RESET TIMING						
Fig. 12	Internal Reset pulse width	t_{40}	1.0			μs	
Fig. 13	External Reset pulse width	t_{41}	1.0			μs	
	Input Clock Frequency			16		MHZ	

*ALL TYPICAL VALUES ARE AT 25°C AND Vcc = 5.0 V

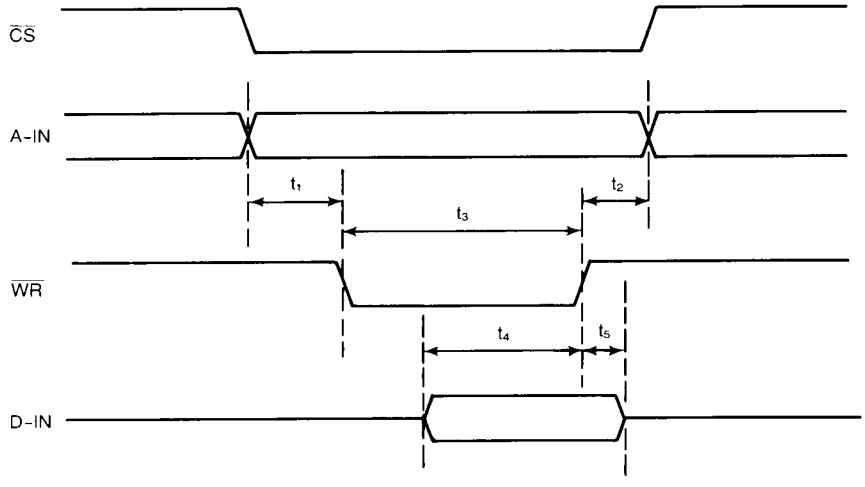


Fig. 3—PROCESSOR WRITE COM52C50 CYCLE

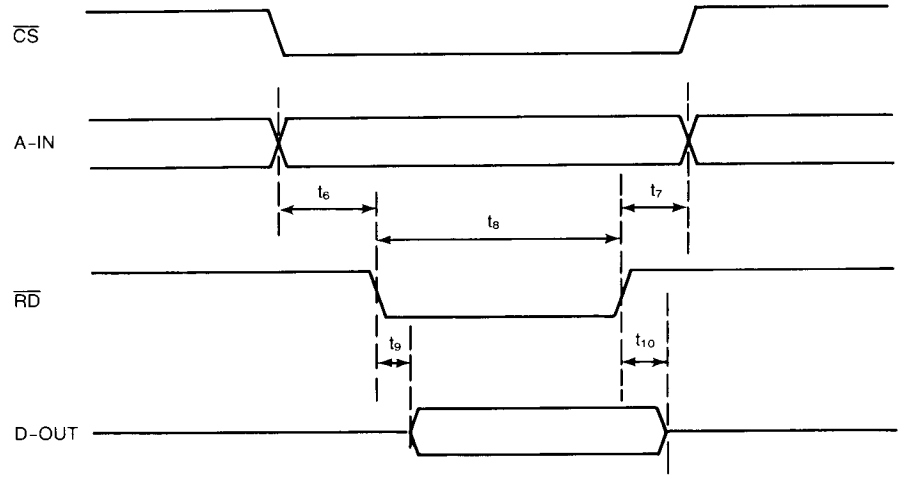


Fig.4—PROCESSOR READ COM52C50 CYCLE

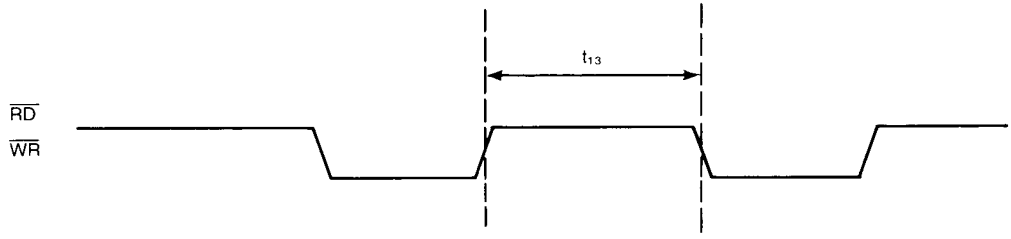


Fig. 5—PROCESSOR ACCESS COM52C50 REPETITION

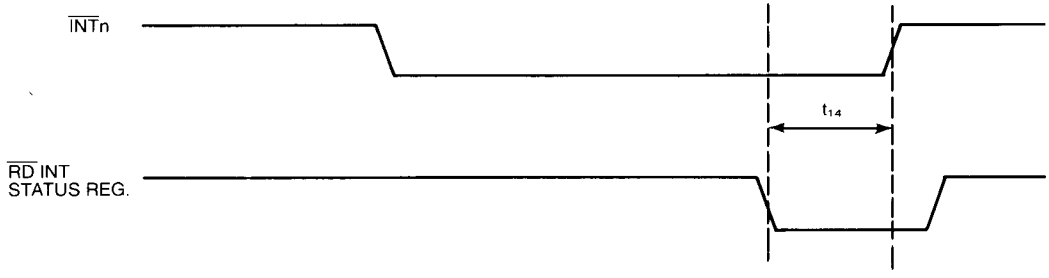


Fig. 6—INTERRUPT ACKNOWLEDGE TIMING

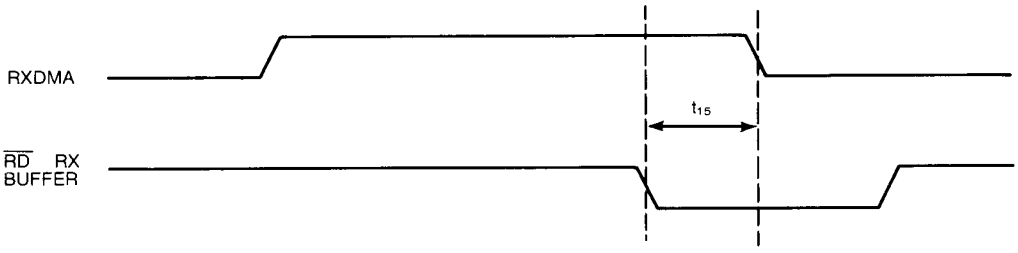


Fig. 7—RX DMA ACKNOWLEDGE TIMING

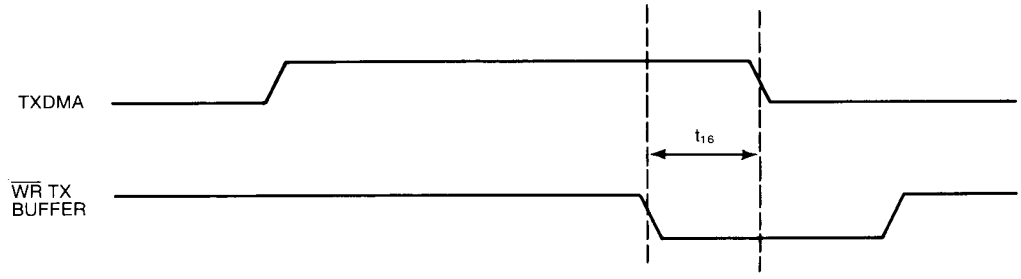


Fig. 8—TX DMA ACKNOWLEDGE TIMING

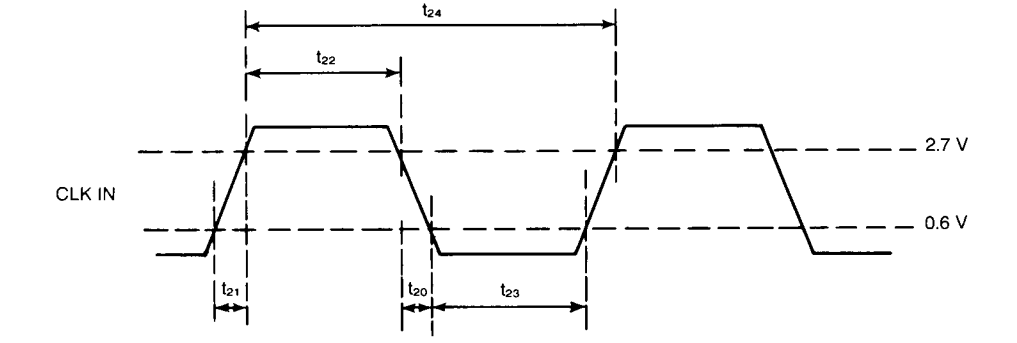


Fig. 9—TTL INPUT CLOCK TIMING

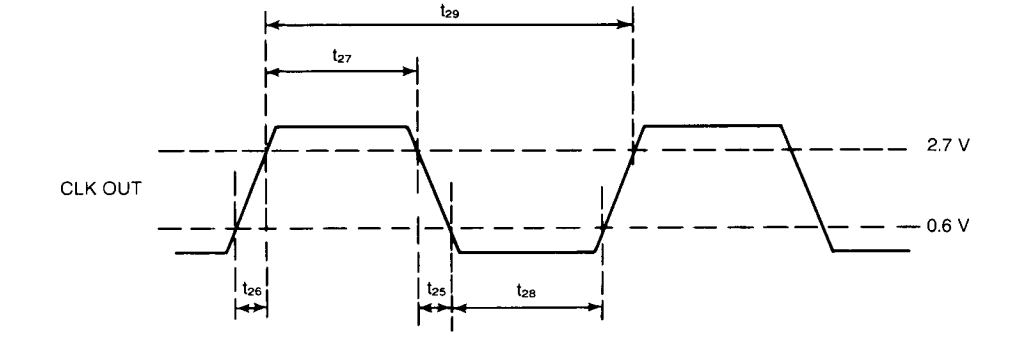


Fig. 10—8 MHZ CLOCK OUT TIMING

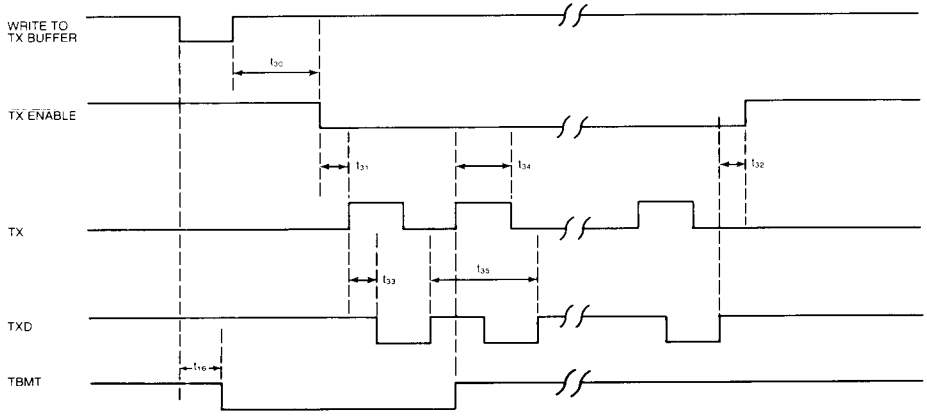


Fig. 11—TX, DTX, TX ENABLE TIMING

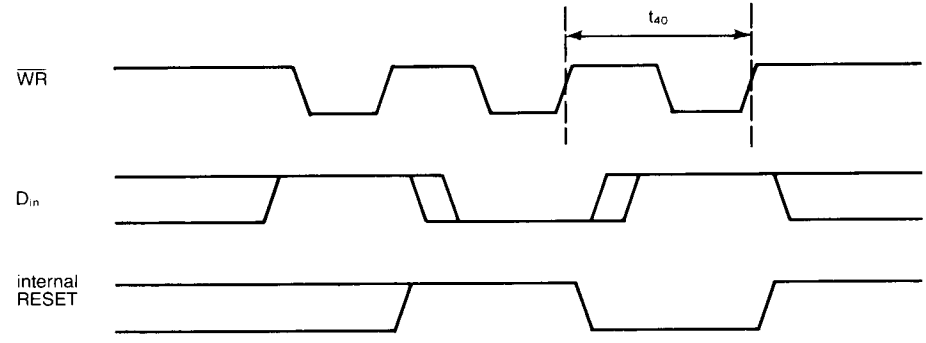


Fig. 12—INTERNAL RESET TIMING

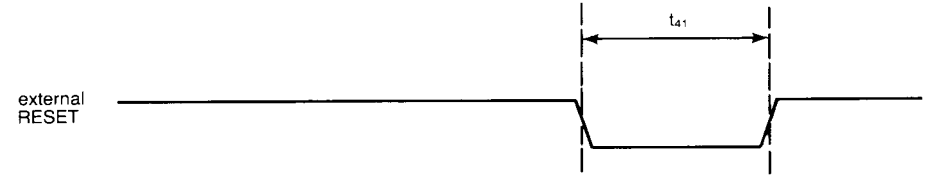


Fig. 13—EXTERNAL RESET TIMING

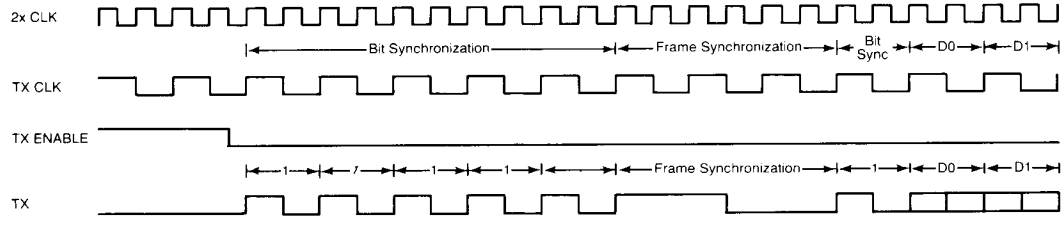


Fig. 14—COM52C50 TRANSMIT START TIMING

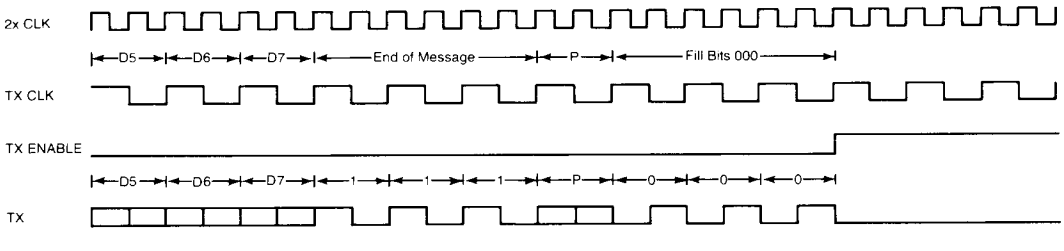


Fig. 15—COM52C50 TRANSMIT END TIMING

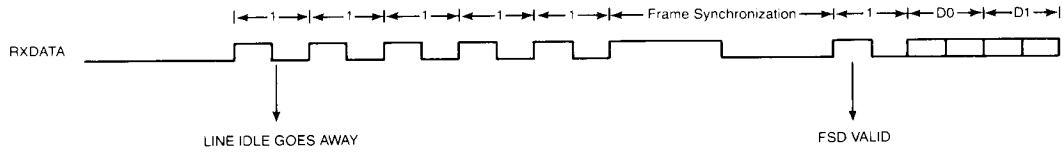


Fig. 16—COM52C50 RECEIVE START TIMING

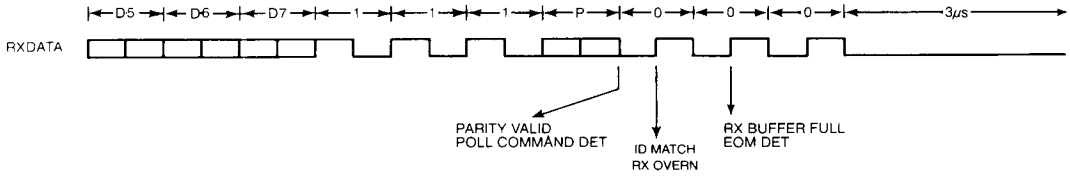


Fig. 17—COM52C50 RECEIVE END TIMING

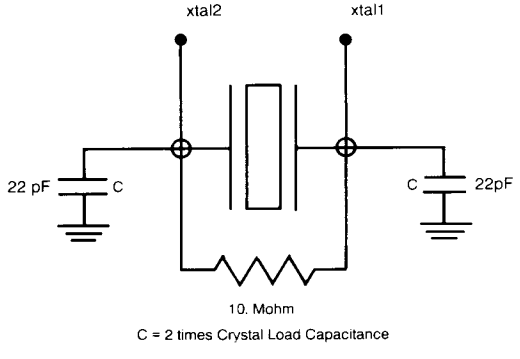


Fig. 18—CONNECTION DIAGRAM FOR PARALLEL RESONANT CRYSTAL

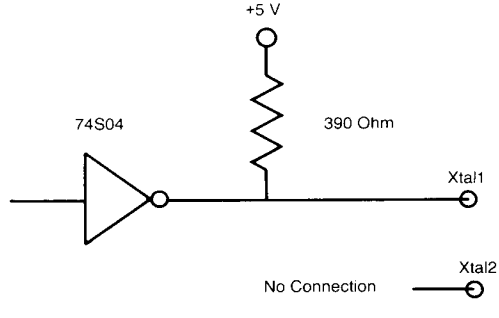


Fig. 19—RECOMMENDED EXTERNAL TTL CLOCK CONNECTION