National Semiconductor

COP498/COP398 Low Power CMOS RAM and Timer (RAT™) COP499/COP399 Low Power CMOS Memory

General Description

The COP498/398 Low Power CMOS RAM and Timer (RAT) and the COP499/399 Memory are peripheral members of the COPS™ family, fabricated using low power CMOS technology. These devices provide external data storage and/or timing, and are accessed via the simple MICROWIRE™ serial interface. Each device contains 256 bits of read/write memory organized into 4 registers of 64 bits each; each register can be serially loaded or read by a COPS controller.

The COP498/398 also contain a crystal-based timer for timekeeping purposes, and can provide a "wake-up" signal to turn on a COPS controller. Hence, these devices are ideal for applications requiring very low power drain in a standby mode, while maintaining a real-time clock (e.g., electronically-tuned automobile radio). Power is minimized by cycling controller power off for periods of time when no processing is required.

The COP499/399 contain circuitry that enables the user to turn a controller on and off while maintaining the integrity of the memory.

A COP400 series N-channel microcontroller coupled with a COP498 (or 499) RAM/Timer offers a user the low-power advantages of an all CMOS system and the low-cost advantage of an NMOS system. This type of system is ideally suited to a wide variety of automotive and instrumentation applications.

Features

- Low power dissipation
- Quiescent current = 40 nA typical (25°C, V_{CC} = 3.0V)
- Low cost
- Single supply operation (2.4V–5.5V)
- CMOS-compatible I/O
- 4 x 64 serial read/write memory
- Crystal-based selectable timer—2.097152 MHz or 32.768 kHz (COP498/398)
- Software selectable 1 Hz or 16 Hz "wake-up" signal for COPS controller (COP498/398)
- External override to "wake-up" controller
- Compatible with all COP400 processors (processor $V_{CC} \leq 9.5V$)
- MICROWIRE-compatible serial I/O
- Memory protection with write enable and write disable instructions
- 14-pin Dual-In-Line package (COP498/398) or 8-pin Dual-In-Line package (COP499/399)

Block Diagram

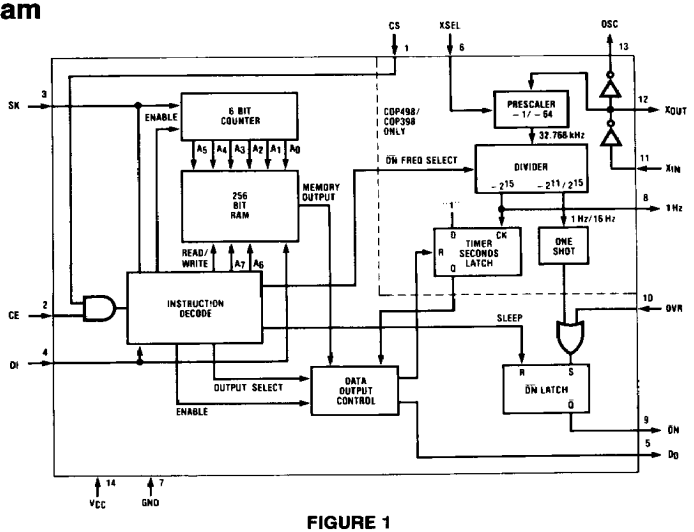

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FIGURE 1

Absolute Maximum Ratings

Voltage relative to GND	
At XSEL, 1 Hz, X_{IN}, X_{OUT}, DO	−0.3V to V_{CC} +0.3V
At all other pins	−0.3V to 10V
Maximum V_{CC} Voltage	6.5V
Total Sink Current Allowed	15 mA
Total Source Current Allowed	10 mA
Ambient Operating Temperature	
COP398/COP399	−40°C to +85°C
COP498/COP499	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
Power Dissipation	50 mW

Note: *"Absolute maximum ratings" indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not insured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

COP398/COP399: −40°C ≤ T_A ≤ +85°C unless otherwise specified.

COP498/COP499: 0°C ≤ T_A ≤ +70°C unless other wise specified.

Parameter	Conditions	Min	Max	Units
Operating Voltage	COP498/COP499	2.4	5.5	V
	COP398/COP399	3.0	5.5	V
Quiescent Current	All inputs at GND			
	T_A = 25°C, V_{CC} = 3.0V		1.0	μA
	T_A = 25°C, V_{CC} = 5.0V		3.0	μA
	T_A = 25°C, V_{CC} = 5.5V		6.0	μA
	T_A = 70°C, V_{CC} = 3.0V		4.0	μA
	T_A = 70°C, V_{CC} = 5.0V		10	μA
	T_A = 70°C, V_{CC} = 5.5V		20	μA
(COP398/COP399 only)	T_A = 85°C, V_{CC} = 3.0V		8.0	μA
	T_A = 85°C, V_{CC} = 5.0V		16	μA
	T_A = 85°C, V_{CC} = 5.5V		30	μA
COP498/COP398				
Standby Current (sleep mode)	V_{CC} = Min., Osc. = 2.097 MHz		200	μA
(running with crystal	V_{CC} = Max., Osc. = 2.097 MHz		700	μA
	V_{CC} = Min., Osc. = 32.768 kHz		20	μA
	V_{CC} = Max., Osc. = 32.768 kHz		100	μA
Operating Current	SK = 250 kHz square wave			
	V_{CC} = Min., Osc. = 2.097 MHz		300	μA
	V_{CC} = Max., Osc. = 2.097 MHz		920	μA
	V_{CC} = Min., Osc. = 32.768 kHz		120	μA
	V_{CC} = Max., Osc. = 32.768 kHz		320	μA
COP499/COP399 Operating Current	SK = 250 kHz square wave			
	V_{CC} = 2.4V for COP498/COP499		100	μA
	V_{CC} = 3.0V for COP398/COP399		140	μA
	V_{CC} = Max.		250	μA
Input Voltage Levels				
CE Input	(Schmitt Trigger Input)			
Logic High (V_{IH})		0.8V_{CC}		V
Logic Low (V_{IL})			0.4V_{CC}	V
OVR Input	(Schmitt Trigger Input)			
Logic High (V_{IH})		0.8V_{CC}		V
Logic Low (V_{IL})			0.2V_{CC}	V
All Other Inputs				
Logic High (V_{IH})		0.7V_{CC}		V
Logic Low (V_{IL})			0.3V_{CC}	V
Output Voltage Levels—DO, 1 Hz				
CMOS Operation				
Logic High (V_{OH})	I_{OH} = −10 μA	V_{CC}−0.1		V
Logic Low (V_{OL})	I_{OL} = 10 μA		0.1	V

DC Electrical Characteristics (Continued)

Parameter	Conditions	Min	Max	Units
Input Leakage Current	COP498/COP499, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	−1.0	+1.0	μA
	COP398/COP399, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	−2.0	+2.0	μA
TRI-STATE®, Open Drain	COP498/COP499, $V_H = V_{CC}$, $V_L = 0V$	−2.5	+2.5	μA
Leakage Current	COP398/COP399, $V_H = V_{CC}$, $V_L = 0V$	−5.0	+5.0	μA
Output Current Levels	$V_{CC} = 4.5V$			
Sink Current				
OSC	$V_{OL} = 0.4V$	0.5		mA
$\overline{ON}$	$V_{OL} = 1.5V$	1.5	8.5	mA
X_{OUT}	XSEL = 1, $X_{IN} = 4.5V$, $V_{OL} = 1.0V$	0.25		mA
X_{OUT}	XSEL = 0, $X_{IN} = 4.5V$, $V_{OL} = 2.0V$	8.0		μA
1 Hz, DO	$V_{OL} = 0.8V$	0.8		mA
Source Current				
$\overline{ON}$	$V_{OH} = 1.0V$	60		μA
X_{OUT}	XSEL = 1, $X_{IN} = 0V$, $V_{OH} = 3.0V$	0.27		mA
X_{OUT}	XSEL = 0, $X_{IN} = 0V$, $V_{OH} = 3.0V$	10		μA
1 Hz, DO	$V_{OH} = 2.0V$	0.4		mA

AC Electrical Characteristics

COP398/COP399: $-40°C \leq T_A \leq +85°C$ unless otherwise specified.

COP498/COP499: $0°C \leq T_A \leq +70°C$ unless otherwise specified.

Parameter	Conditions	Min	Max	Units
COP Interface				
SK Frequency	CS = 1, CE = 1 COP498/COP499	4.096	250	kHz
	CS = 1, CE = 1 COP398/COP399	8.192	250	kHz
SK Duty Cycle	SK frequency ≥ 25 kHz	25	75	%
	SK frequency = 4.096 kHz	48	52	%
Inputs				
CS				
t_{CSS}		0.2		μs
t_{CSH}		0		μs
DI				
t_{SETUP}		0.4		μs
t_{HOLD}		0.4		μs
Output				
DO	$C_L = 100$ pF, $4.5V \leq V_{CC} \leq 5.5V$,			
t_{pd1}, t_{pd0}	$V_{OUT} = 1.5V$		2.0	μs
t_{pd1}, t_{pd0}	$C_L = 50$ pF, V_{CC} = Min.,			
	$V_{OUT} = 1.5V$		2.4	μs
Crystal Osc. Frequency	XSEL = 1		2.1	MHz
	XSEL = 0		65	kHz

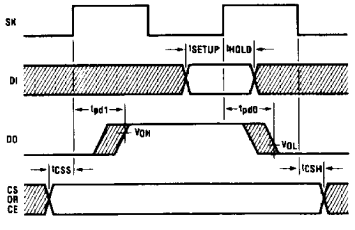

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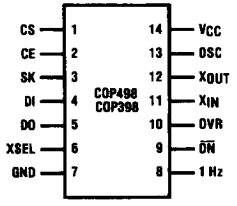
FIGURE 2. Synchronous Data Timing

Connection Diagrams

Dual-In-Line Package



Top View

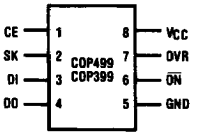


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FIGURE 3

Order Number COP398N, COP498N, COP399N, or COP499N
See NS Package Number N08E or N14A

Pin Descriptions

Pin	Description
CS	Chip Select
CE	Chip Enable
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
XSEL	Crystal Option Select
X_{IN}	Crystal Oscillator Input
X_{OUT}	Crystal Oscillator Output

Pin	Description
1 Hz	1 Hz Square Wave Output
$\overline{ON}$	Active Low Wake-Up Signal to COPS Controller
OVR	External Override Wake-Up for COPS Controller
OSC	Open Drain Oscillator Output
V_{CC}	Power Supply
GND	Ground

COP398 and COP399 are extended temperature devices (−40°C to +85°C) of COP498 and COP499 (0°C to 70°C) respectively, with all other functional and electrical characteristics being the same. Therefore, no further attempt will be made to distinguish between COP498 and COP398 or between COP499 and COP399. Unless otherwise specified, the following descriptions will apply to both COP498 and COP499, and they will be known as the device.

INSTRUCTION SET

COP498 has six instructions as indicated in *Figure 4.* Note that the MSB of any given instruction is a "1". This bit is properly viewed as a start bit in the interface sequence. The lower 4 bits of the instruction contain the command for the device. One of the instructions (TSEC) should not be used in COP499 as it serves no purpose.

Instruction	Opcode	Comments
	MSB	
WRITE	1 s 1 r_1 r_0	s = $\overline{ON}$ (wake up signal) frequency select 1 = 16 Hz, 0 = 1 Hz (s selection for COP498 only) (s = 0 for COP499)
READ	1 1 0 r_1 r_0	r_1, r_0 = register number (00, 01, 10, 11)
WREN	1 0 0 1 1	Write enable
WRDS	1 0 0 0 0	Write disable
TSEC	1 0 0 1 0	Test timer seconds latch (COP498 only)
SLEEP	1 0 0 0 1	Put COPS controller to sleep ($\overline{ON}$ high)

FIGURE 4. Instruction Set

Functional Description

A block diagram of COP498 and COP499 is given in *Figure 1.* Positive logic is used. When a bit is set to the higher voltage it is a logic "1"; when a bit is reset to the lower voltage it is a logic "0". The COP498 can execute six instructions: READ (from any one of 4 registers in memory); WRITE (to any one of 4 registers in memory); WREN (write enable); WRDS (write disable); TSEC (test and reset timer seconds latch); and SLEEP (drive $\overline{ON}$ signal high to turn off COPS controller). The COP499 can execute all the above instructions except TSEC. All communications with the device are via the serial MICROWIRE interface. Both CS and CE (CE only in COP499) must be high to enable the device. The device must be deselected between instructions — either CS and/or CE must go low to insure proper operation. The deselecting of the device resets the counters and serial input register.

READ/WRITE MEMORY

The device has 256 bits of read/write memory. The memory is organized as 4 registers of 64 bits each. The data is accessed serially through the Data input (DI) and Data Output (DO) pins. SK is the clock signal for data and instructions.

The memory address register can be conceived of as two registers: one two bits long and loaded directly from the instruction; the other six bits long and incremented by 1 with each SK pulse as long as the chip is selected. The two bit register does not change during the execution of a given instruction. The six bit register is reset to zero while the device is deselected. When counting, the six bit register wraps around from its maximum value back to zero. Thus memory locations are addressed relative to the number of SK pulses after the chip is selected.

Functional Description (Continued)

The READ instruction will select one of the 4 registers (the register being identified in the instruction opcode as indicated in *Figure 4*) and output the contents of that register to the DO pin until the device is deselected. Note that data output from the device, as a result of a READ instruction, continues as long as the device is selected and clocks are provided. Reading more than 64 bits will cause rereading of some bits as the memory address register wraps around from the maximum value back to zero.

The WRITE instruction selects one of the 4 registers (the register being identified in the instruction opcode as indicated in *Figure 4*) and takes the data from the DI pin and stores that data into the memory register until the device is deselected. The write Operation continues as long as the device is selected and clocks are provided. Thus writing more than 64 bits will cause a portion of the data to be overwritten.

TIMER (COP498 ONLY)

With the XSEL pin tied high (V_{CC}), the timer is a 21 stage counter which can divide a 2.097152 MHz signal down to 1 Hz. This creates the 1 Hz signal output. With XSEL tied low (ground), the timer is a 15 stage counter which divides a 32.768 kHz signal down to create the 1 Hz signal output. The rising edge of the 1 Hz signal is used internally to set the timer seconds latch. A wake-up signal is generated at the $\overline{ON}$ output. This signal can be used to turn a COPS controller on. The wake-up rate is software selectable and may be either 1 Hz or 16 Hz. A bit in the WRITE instruction controls this wake-up rate (see *Figure 4*). By means of the SLEEP instruction a COPS controller may cause the $\overline{ON}$ signal to go high thereby providing a means for the controller to safely turn itself off.

An override capability is present whereby the $\overline{ON}$ pin may be prevented from going high. A "1" level at the OVR pin will force $\overline{ON}$ to go low (or stay low) thereby causing the controller to turn on or remain on. $\overline{ON}$ will remain low, and the controller on, as long as the OVR pin is high. To preserve timekeeping when using the override feature, a timer seconds latch is provided. This latch is set by the rising edge of the 1 Hz signal and is read and reset by the TSEC instruction. The timer seconds latch is primarily intended for use when the override feature is implemented. However, it does provide a convenient one second timer which is software testable over a common serial port.

SYSTEM CONSIDERATIONS

When the COPS processor is being turned on and off, during the power supply transition between ground and operating voltage, some pulses may occur at the output pins of the processor. By using the WRDS and WREN instructions, together with the higher "1" level of the CE pin, accidental writing into the memory may be prevented. This is done by disabling the write operation before going to sleep and enabling the write operation when the COPS processor starts execution. A WRDS instruction is automatically executed if the SLEEP instruction causes $\overline{ON}$ to go high turning off the COPS processor. Furthermore, WREN instruction is disabled as long as $\overline{ON}$ remains high.

The XSEL pin, which identifies the timer counter length, should be tied to either V_{CC} or ground depending on the crystal input. For proper operation, the state of XSEL should not be changed while the device is in operation. If the oscillator and timer features are not used, the X_{IN} pin should be connected to the GND pin and XSEL tied to V_{CC}. If the override feature is not used the OVR pin should be connected to the GND pin.

The device is in a static mode when either the CS or CE pin is low. However, the device is in a dynamic mode when both CS and CE are high and at least one high level has been detected at SK while both pins are high. Because of this, a minimum frequency is specified for the SK clock. This minimum frequency really translates to maximum on and off times for the SK clock. As the SK clock slows down, the duty cycle must get closer to 50%. For best operation, the user should regard the maximum on and off times for the SK clock as about 122 μs (61 μs for COP398/COP399).

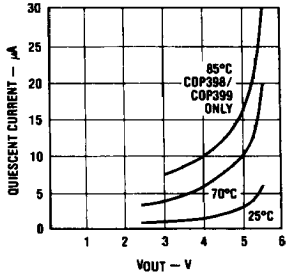
COPS CONTROLLER TO COP498/COP499 HARDWARE INTERFACE

If the COPS controller is operating with a 4 μs instruction cycle time, a 47k resistor should be connected between SK and V_{CC} to speed up the rise time of the SK clock. If the override feature is used in COP498, the override signal should be connected to the OVR pin of the COP498 and an input of the COPS controller. This is simply to provide a means for the controller to know if it was turned on by override or normal timeout. The override signal should be free of noise. In systems where the COPS controller is operating with V_{CC} greater than 6 volts, SI and the override input on the controller should have high impedance, standard TTL level input options selected. To minimize current drain in the controller, the override input to the controller should always use the high impedance option.

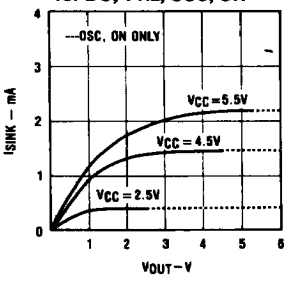
Figure 6a illustrates the COP498 interface in a system with supply voltage less than 6 volts. The COPS controller can either be turned on by the timer or an external signal. A PNP transistor, controlled by the $\overline{ON}$ signal of the COP498, is used to gate the power to the COPS controller. A 0.05 μF capacitor is connected across the supply pins of the controller to reduce voltage variations due to current spikes. It is not recommended to use large capacitance values here as problems can be introduced if the power supply fall time is too long. The switched supply fall time should be kept to about ten instruction cycles of the COPS processor. Resistor R2, between the $\overline{ON}$ pin of the COP498 and the base of the transistor, is used to limit current. Resistor R1, between the base and emitter of the transistor, is used to turn the transistor off when $\overline{ON}$ is high. The CE pin of the COP498 is tied to the V_{CC} pin of the controller. This guarantees that the controller is at its full operating voltage before the COP498 can be accessed. When turned on, the PNP transistor should be saturated in order to minimize the voltage drop across it. The system power supply, which here is V_{CC} to the COP498, must be high enough to insure that the controller V_{CC} — which is the system supply less the voltage drop across the PNP transistor — is high enough to be recognized as a logic "1" at the CE input of the COP498. It is also desirable to have all input signals to the COP498 as close as possible to the COP498 supply levels to eliminate any static power drain which could significantly increase standby and operating current.

Typical Performance Curves

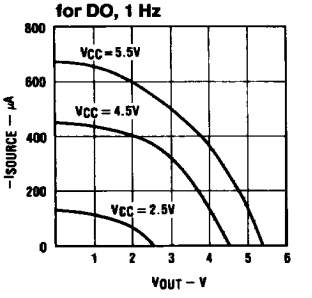
Maximum Quiescent Current COP498/499/398/399



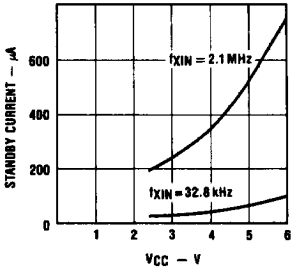
Minimum Sink Current for DO, 1 Hz, OSC, $\overline{ON}$



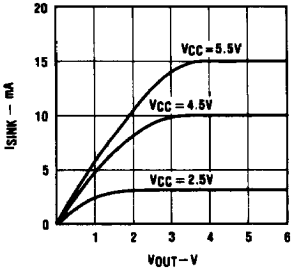
Minimum Source Current for DO, 1 Hz



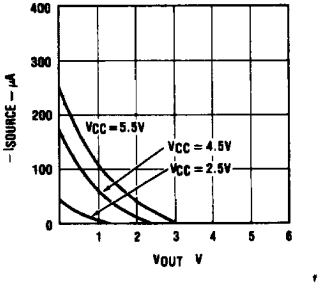
Maximum Standby Current for COP498/398



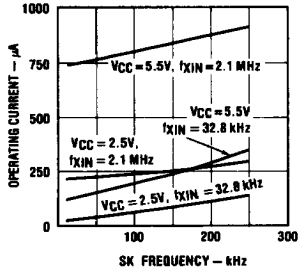
Maximum Sink Current for $\overline{ON}$



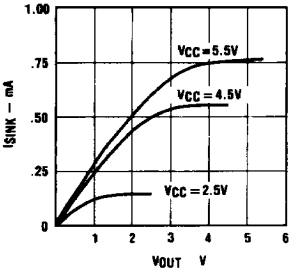
Minimum Source Current for $\overline{ON}$



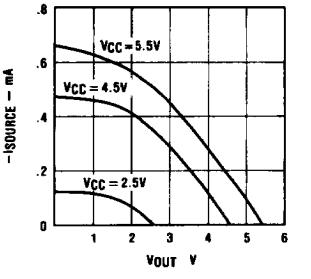
Maximum COP498/398 Operating Current



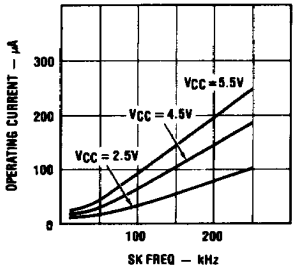
X_{OUT} Minimum Sink Current with XSEL = 1



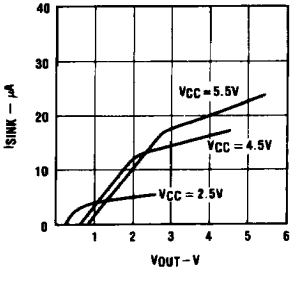
X_{OUT} Minimum Source Current with XSEL = 1



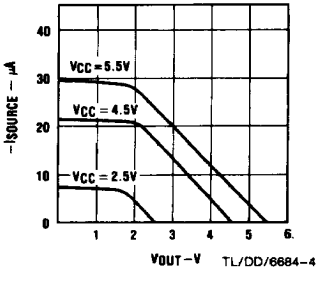
Maximum COP499/399 Operating Current



X_{OUT} Minimum Sink Current with XSEL = 0



X_{OUT} Minimum Source Current with XSEL = 0



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Functional Description (Continued)

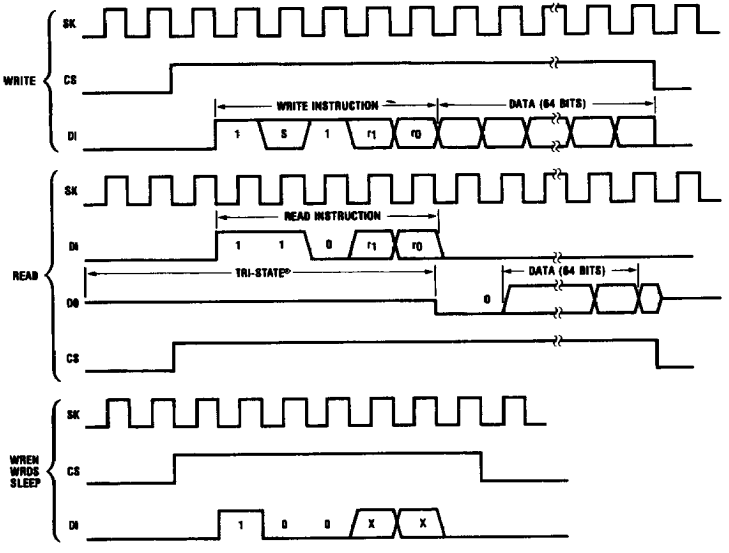

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FIGURE 5a. Instruction Timing

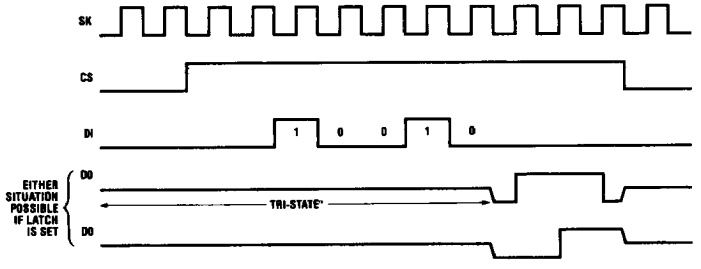

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FIGURE 5b. TSEC Instruction Timing

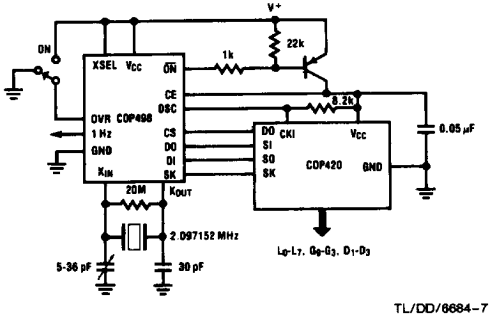

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FIGURE 6a. COP498-COP420 Interface

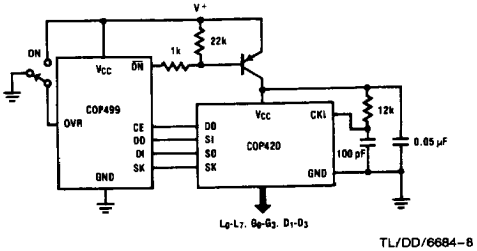

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FIGURE 6b. COP499-COP420 Interface

Functional Description (Continued)

Figure 6b illustrates the COP499 interface in a system with a supply voltage less than 6 volts. The COPS processor is being turned on by a switch (or an external signal) connected to the OVR pin.

Figure 7 illustrates a COP498 interface in a system with a supply voltage greater than 6 volts. In such a system, the COP498 cannot be connected directly across the system supply. The power to the COP498 is derived from the system supply by means of a standard zener diode arrangement. A zener diode with a breakdown of about 5 volts is recommended. A capacitor is connected across the COP498 supply pins to reduce voltage variations due to current spikes and to supply extra current when the COP498 is in active operation. Here it is assumed that the COP498 is in standby mode, i.e., deselected, most of the time and is active, selected, for a short period (less than 100 SK periods).

The zener diode series resistor R3 should be selected to meet the current requirements of the zener diode and the standby current of the device. The primary purpose of the zener diode is to place an upper limit on the value of V_{CC} to the device. This insures that V_{CC} to the device will not exceed the specified maximum value. Since the device will operate from 2.5V to 6.0V, the choice of zener diode and series resistor is not critical.

Note that the user may generate the two supply voltages in any manner compatible with system requirements.

Because the COPS controller and the device have different operating voltages, the high impedance standard TTL level input should be selected on the COPS controller for SI and any other input to the controller from the device.

SAMPLE SYSTEM CURRENT DRAIN CALCULATION

Suppose a 5V system consists of a COP420 and a COP498 with a 32.768 kHz crystal. The COP420 is being turned on once a second. Assume that the COP420 need 10 ms for internal reset and 10 ms to update all the necessary information, then the COP420 will be turned on for 20 ms every second, i.e., a duty cycle of 2%; and the COP498 will be in operating mode for at most 10 ms, i.e., a duty cycle of less than 1%. Because of the short duty cycle, it is further assumed that the COP498 current drain will be that of standby current, about 75 μA at 5V. The current drain through the base of the switching transistor that turns on the COP420 can be estimated by the voltage drop across the current limiting resistor and in this case is assumed to be 3.5 mA.

COP498 current drain = 75 μA
COP420 current drain = 0.02 × 25 mA = 500 μA
Switching transistor base current = 0.02 × 3.5 mA = 70 μA
Total system current drain = 500 + 70 + 75 μA = 645 μA

The result shows that it is possible to achieve the low cost of NMOS and low power dissipation of CMOS simultaneously with a system consisting of a COP498 and a COPS processor.

COPS CONTROLLER — COP498/398 SOFTWARE INTERFACE

Figure 8 shows a typical flow chart for a COP498 or COP499 interface to a COPS microcontroller system. This flow chart also illustrates the override feature. Since the override feature is being used, the first step is to inquire the device if it is necessary to increment the time. It is assumed that timekeeping is a necessary part of the application. This interrogation of the device is accomplished by means of the TSEC instruction which dumps the contents of the timer seconds latch to the serial output port and resets the latch. If the latch was set, the time must be incremented. This is accomplished by reading the appropriate memory register into the controller, incrementing the time and writing the register back out to the device. The next step is to check for the override signal. If it is present a special override routine may be performed. If no override is present, the controller

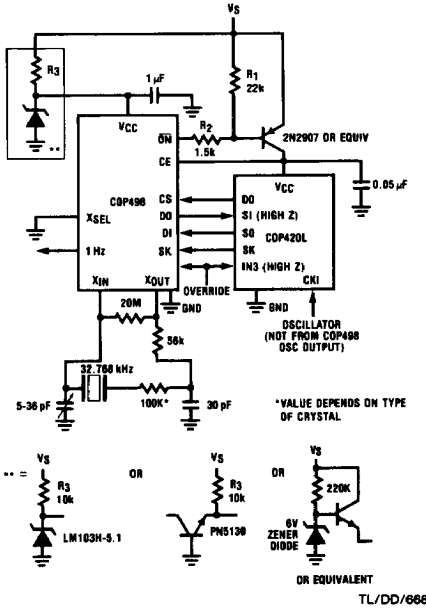

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FIGURE 7. COP498-COP420L Interface with V_S = 9V and 32.768 kHz Crystal

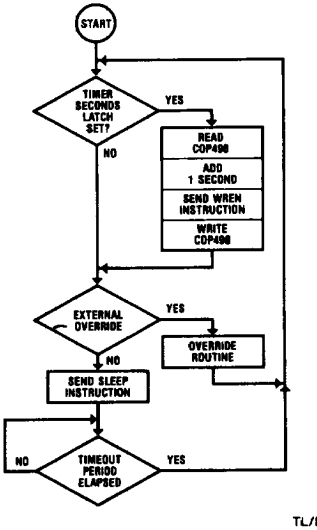

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FIGURE 8. Typical COP498 Interface Flowchart

Functional Description (Continued)

turns itself off by sending a SLEEP command to the device. After sending the SLEEP command, the controller goes into a loop to wait for power to go off. In the event the controller is turned back on by the override signal before the voltage has dropped, the loop has a time limit which, when exceeded, causes the controller to jump to the beginning of the program and start again. If the override feature is not used there is no need to test the timer seconds latch nor to test for the override signal. Without the override, the controller can only be turned on by the COP498 if the time out period has elapsed. Note also that the timer features continue to operate regardless of the state of the override signal. The override signal, when high, merely forces the $\overline{ON}$ pin to go low. The operation of the rest of the chip is in no way affected by the override signal.

GENERAL CODE FOR SOFTWARE INTERFACE

The code in *Figure 9a* is recommended for interfacing the device to any COPS controller other than COP410L/COP411L. The code in *Figure 9b* is the recommended interface code for COP410L/COP411L. The code is written as subroutines and the code uses one level of subroutine internally. It is apparent from the code that the software interface is somewhat different for the READ and WRITE instructions than for the rest of the instructions. The routine labelled SETUP is assumed to be in page 2 of the ROM. The rest of the code may be located anywhere in program memory subject to the usual programming rules of COPS microcontrollers. The lower four bits of the instruction opcode are assumed to be located in RAM location COMAND, which is chosen as location 3,15. Data I/O uses register 2. The controller-COP498/499 interface is assumed to be as in *Figure 6* or *Figure 7*. It is assumed that the SIO register in the COPS controller is enabled as serial I/O prior to entry to these routines.

```
WRITE:    JSRP   SETUP
RW:       LD
          XAS              ; READ/WRITE DATA
          XIS
          JP     RW
          OBD              ; DISABLE THE COP498/499 (B=0)
          JP     FINISH
READ:     JSRP   SETUP
          NOP              ; NEED A TOTAL OF 5 SK CLOCK DELAYS (5 NOP'S)
          NOP              ; UNTIL DATA OUT IS VALID AT SIO REGISTER
          NOP
          NOP
          NOP
          JP     RW
INSTRT:   JSRP   SETUP     ; ROUTINE FOR THE REST OF THE INSTRUCTIONS
          NOP
          NOP              ; DELAYS TO INSURE PROPER TIMING
FINISH:   CLRA
          RC
          OBD              ; DESELECT THE COP498/499 (B=0)
          XAS              ; TURN OFF THE CLOCK
          RET
          . PAGE 2
SETUP:    LBI    COMMAND   ; POINT TO LOCATION WHERE COMMAND STORED
          CLRA
          SC
          XAS              ; TURN ON SK CLOCK
          OBD              ; ENABLE THE COP498/499 (B=15)
          CLRA
          XAS              ; MAKE SURE NO INVALID DATA SENT
          CLRA
          AISC   1         ; SET UP START BIT
          SC
          XAS              ; SEND START BIT MSD OF INSTRUCTION
          LD               ; FETCH COMMAND TO A
          NOP
          NOP              ; MAINTAIN PROPER TIMING
          XAS              ; SEND COMMAND
          LBI    2,0       ; POINT TO READ/WRITE REGISTER
          RET              ; RETURN TO MAIN ROUTINE
```

FIGURE 9a. Software Interface to COP498/COP499 for COPS Controllers Other Than COP410L/COP411L

Functional Description (Continued)

```
WRITE:  JSRP   SETUP
RW1:    XAS                  ; SEND COMMAND
RW2:    LD
        XDS                  ; POSITION Bd PROPERLY
RW:     LD
        XAS
        XIS
        JP     RW
        OBD                  ; DISABLE THE COP498/499 (B=0)
        JP     FINISH
READ:   JSRP   SETUP
        XAS                  ; SEND READ COMMAND
        NOP                  ; DELAY FOR DATA VALID
        NOP
        NOP
        NOP
        NOP
        JP     RW2
INSTRT: JSRP   SETUP         ; ROUTINE FOR REST OF INSTRUCTIONS
        XAS                  ; SEND INSTRUCTION
        NOP
        NOP
        NOP                  ; DELAY FOR INSTRUCTION ACCEPT
        NOP
FINISH: CLRA
        RC
        OBD                  ; DESELECT THE COP498/499
        XAS                  ; TURN OFF THE CLOCK
        RET
        . PAGE 2
SETUP:  LBI    COMMAND
        CLRA
        SC
        XAS                  ; TURN ON SK CLOCK
        OBD                   ENABLE THE COP498/COP499 (B=15)
        CLRA
        XAS                  ; MAKE SURE NO INVALID DATA SENT
        CLRA
        AISC   1
        SC
        XAS                  ; SEND START BIT-MSD OF INSTRUCTION
        LD                   ; FETCH INSTRUCTION
        LBI    2,9
        RET
```

FIGURE 9b. COP410L/COP411L Software Interface to COP498/COP499

The code in *Figure 9a* will read or write 64 bits at a time. Note that in the COP410L/411L the code in *Figure 9b* will read or write 32 bits at a time. The code of *Figure 10* is recommended if the user wishes to work in blocks of 64 bits with the COP410L/411L. Only the code which is different from that shown in *Figure 9b* is shown in *Figure 10.*

The routine in *Figure 10* will read/write into registers 2 and 1 in the COP410L/411L. *Figure 10* illustrates the preferred method of achieving full utilization of the device memory when the COP410L/411L is the contoller. Remember that all the other routines are as shown in *Figure 9B. Figure 10* illustrates only that code that must be changed to achieve full usage of the device memory when using the COP410L/411L.

GENERAL NOTES

1. For complete safety in all cases it is recommended that the SK clock be turned off after the device has been deselected since the device is dynamic when it is enabled, If the clock is turned off while the device is selected, special care must be given to the SK timing characteristics. In no case should the clock be turned off while the device is selected if the SK period is greater than about 50 μs.

Functional Description (Continued)

```
WRITE: JSRP   SETUP       ; INITIALIZE, SEE FIGURE 9B
RW1:   XAS                ; SEND COMMAND
RW2:   LD                 ; POSITION Bd
       XDS
RW:    LD
       XAS
       X      3           ; USE REGISTERS 2 AND 1
       LD
       NOP
       XAS
       XIS    3
       JP     RW
       OBD                ; DESELECT THE COP498/499
       JP     FINISH
```

FIGURE 10. COP410L/411L-COP498/499 Special Routine

2. The device does not become dynamic until both CS and CE are high and at least one high level is seen at the SK input. Thus the device may be safely enabled prior to turning on the clock as long as SK is low when the device is enabled.
3. The device must be deselected between instructions. Failure to do so will yield improper operation. The device relies on the select lines changing state in order to clear internal registers. Only one of the select lines on the COP498 needs to go low between instructions.
4. The user must insure that a WREN (write enable) instruction has been performed in order to write to the device memory. The WREN command need be given only once unless the SLEEP feature is used. If $\overline{ON}$ goes high as a result of a SLEEP command, a write disable is automatically performed in order to provide maximum protection to the device memory while the COPS controller is powering up and powering down. As long as $\overline{ON}$ remains high, WRITE and WREN instructions are disabled. Thus when the COPS controller wakes up after previously issuing a SLEEP command, a WREN instruction is required before data can be written to the device.
5. The six bit section of the RAM address register will increment whenever there are clock pulses present when the CS and CE pins are high. Thus the user can position the RAM address register if he wishes by selecting the device, holding the DI pin low and supplying the appropriate number of clocks. Then, without deselecting the device, the user would send the instruction and read or write data. Although possible, this technique is not recommended as it is fairly involved.
6. When using the TSEC command in COP498 with the code as given in *Figure 9,* the master program should test for the accumulator greater than 1 to determine if the timer seconds latch was set. Note again, test for greater than 1; do not test for greater than zero.

NOTE ON MICROWIRE INTERFACE

If the device is connected to a MICROWIRE interface containing other circuits whose DO (data output) pins may produce a signal swing higher than V_{CC} of the device, some protection is needed on the DO pin of the device. This happens when the DO pins of several peripherals powered by different voltages are connected together; e.g., a COP452 at 4.5V with a COP499 at 2.4V. When the DO pin of COP498/499 is externally driven above its power supply voltage, a current will flow into it and this current must be limited to 1 mA. As an example we have two COP452s with a COP420L operating at 4.5V and a COP499 operating at 2.4V. When enabled, the DO pin of a COP452 may swing higher than 2.4V, the power supply voltage of the COP499. One way to limit the current is to use a current limiting resistor of 2 kΩ between the DO pins of the COP452 and the COP499. NOTE: the SI pin of the COPS processor MUST BE A Hi-Z INPUT. Two configurations are possible as shown in *Figure 11.* Note that the resistor between DO and SI will give extra RC delay to the signal going from the DO pin to the SI pin of the COPS processor. Connection B is preferred because the DO signal from COP499 has nearly a whole SK cycle to become valid at SI input before the signal is read by the processor. When a ROMless COPS processor (COP401L/COP402/COP404L) is used for emulation, the circuit shown in *Figure 12* may be used to simulate a Hi-Z input for the SI pin.

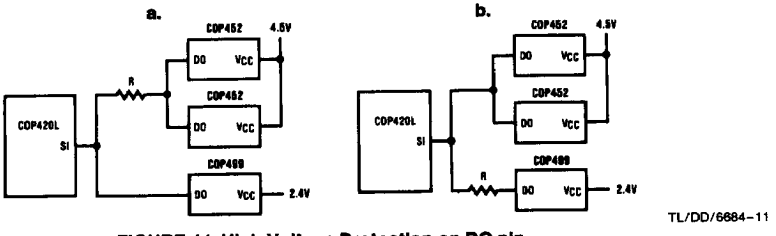

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FIGURE 11. High Voltage Protection on DO pin

Functional Description (Continued)

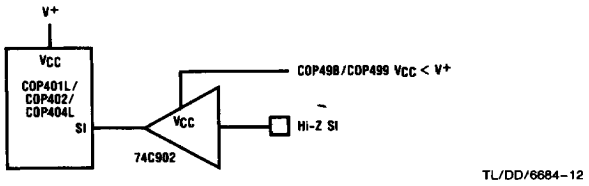

FIGURE 12. Simulating Hi-Z SI Input on ROMless Processors