

SUBMINATURE MONOLITHIC TVS ARRAYS

APPLICATIONS

- ✓ Ethernet - 10 Base T
- ✓ Cellular Phones
- ✓ Handheld Electronics
- ✓ FireWire & USB Interfaces

IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns

FEATURES

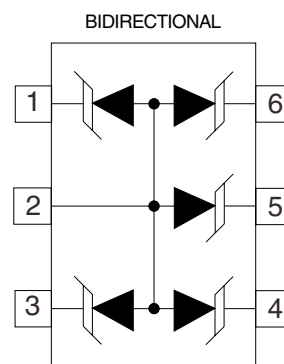
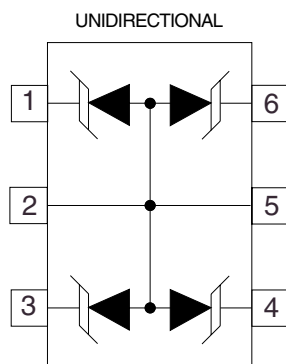
- ✓ ESD Protection > 25 kilovolts
- ✓ 200 Watts Peak Pulse Power per Line ($t_p = 8/20\mu s$)
- ✓ Low Clamping Voltage
- ✓ Available in Four Voltage Types Ranging from 5V to 24V
- ✓ Up to Four (4) Lines of Bidirectional and Five (5) Lines of Unidirectional Protection
- ✓ Low Leakage Current

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SOT-23-6
- ✓ Weight 0.6 grams (Approximate)
- ✓ Flammability Rating UL 94V-0
- ✓ 8mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Marking Code & Pin One Defined By DOT on Top of Package



CIRCUIT DIAGRAMS



DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	200	Watts
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER (See Notes 1, 2 & 3)	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ $I_p = 1A$ V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ 8/20 μs V_C @ I_{PP}	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D μA	TYPICAL CAPACITANCE 0V @ 1 MHz C_1 pF
CP05	QRH	5.0	6.0	9.8	11.8V @ 17.0A	20	70
CP05C	QRL	5.0	6.0	9.8	11.8V @ 17.0A	20	70
CP12	QRI	12.0	13.3	19	28.3V @ 7.0A	1	50
CP12C	QRM	12.0	13.3	19	28.3V @ 7.0A	1	50
CP15	QRJ	15.0	16.7	24	45.0V @ 5.0A	1	30
CP15C	QRN	15.0	16.7	24	45.0V @ 5.0A	1	30
CP24	QRK	24.0	26.7	43	65.0V @ 3.0A	1	25
CP24C	QRO	24.0	26.7	43	65.0V @ 3.0A	1	25

Note 1: Part numbers with an additional "C" suffix are bidirectional devices, i.e., CP05C.

Note 2: *Unidirectional Only:* Test between pin 1 to 2 or 5, 4 to 2 or 5, 6 to 2 or 5, 3 to 2 or 5.

Note 3: *Bidirectional Only:* Test between pin 5 to 1 or 3 or 4 or 6. Electrical characteristics apply in both directions.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

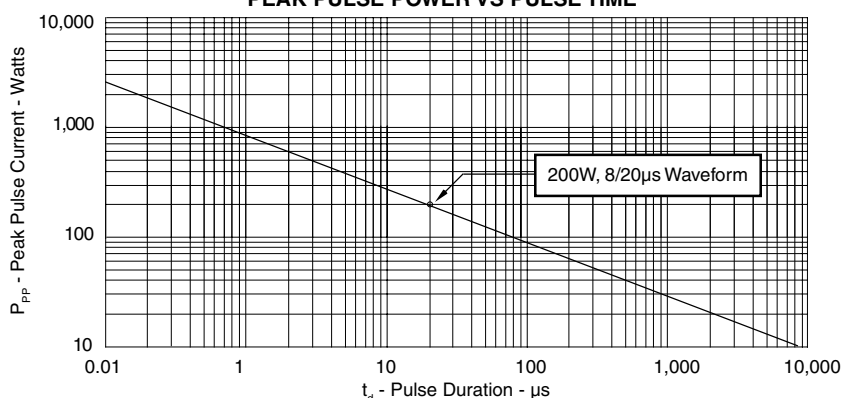
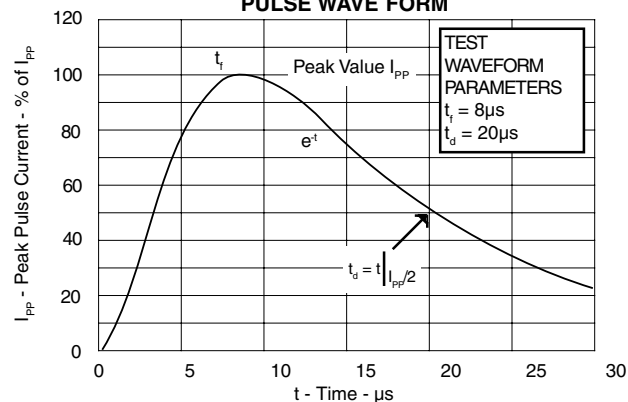
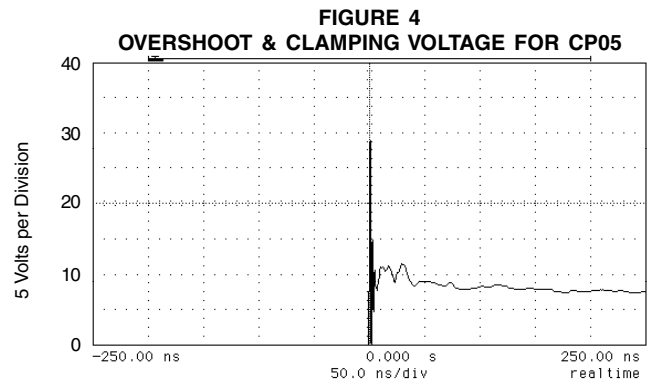
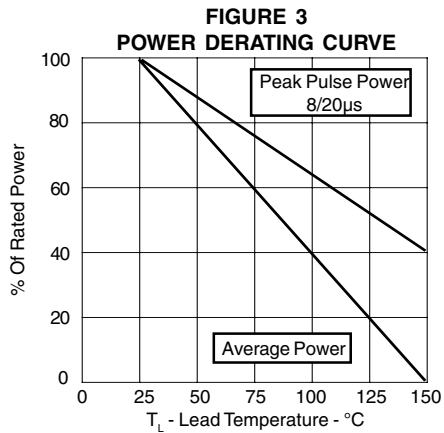


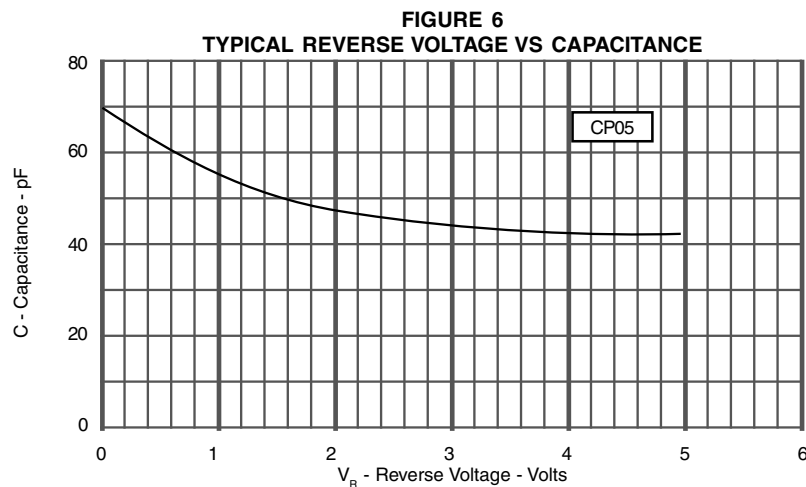
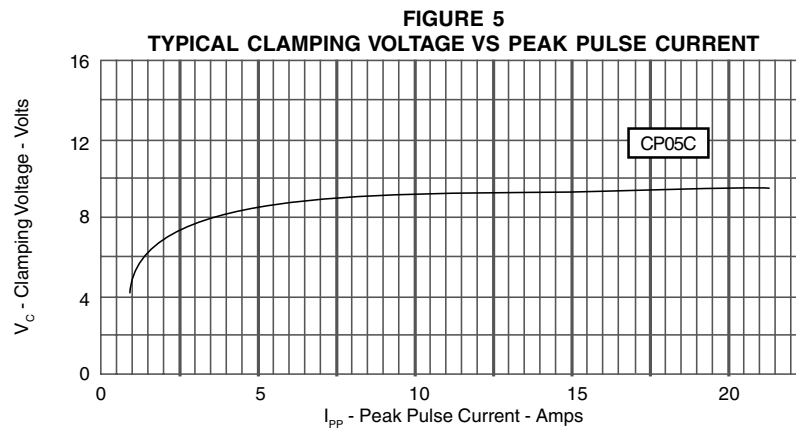
FIGURE 2
PULSE WAVE FORM



GRAPHS



ESD Test Pulse: 25 kilovolt, 1/30ns (waveshape)



APPLICATION NOTES

The CP Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD (> 25kV) or EFT. This product series provides both unidirectional and bidirectional protection, with a surge capability of 200 Watts P_{PP} per line for an 8/20 μ s waveform.

UNIDIRECTIONAL COMMON MODE CONFIGURATION (Figure 1)

The CP Series provides up to four (4) lines of protection in a common mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 1.
- ✓ Line 2 is connected to Pin 3.
- ✓ Line 3 is connected to Pin 4.
- ✓ Line 4 is connected to Pin 6.
- ✓ Pin 5 is connected to ground.
- ✓ Pin 2 is not connected.

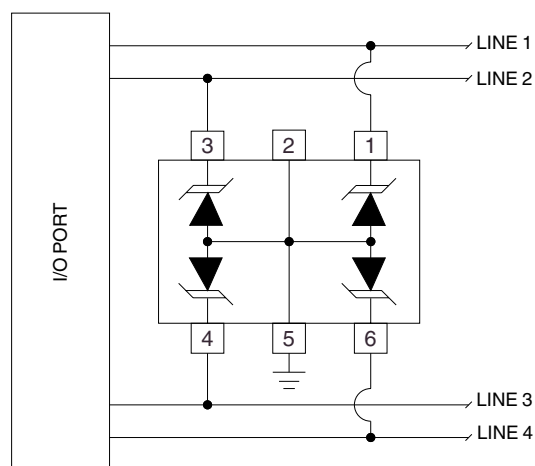


Figure 1 - Unidirectional Configuration Common-Mode I/O Port Protection

BIDIRECTIONAL COMMON MODE CONFIGURATION (Figure 2)

The CPxxC Series provides up to four (4) lines of protection in a common mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 1.
- ✓ Line 2 is connected to Pin 3.
- ✓ Line 3 is connected to Pin 4.
- ✓ Line 4 is connected to Pin 5.
- ✓ Pin 6 is connected to ground.
- ✓ Pin 2 is not connected.

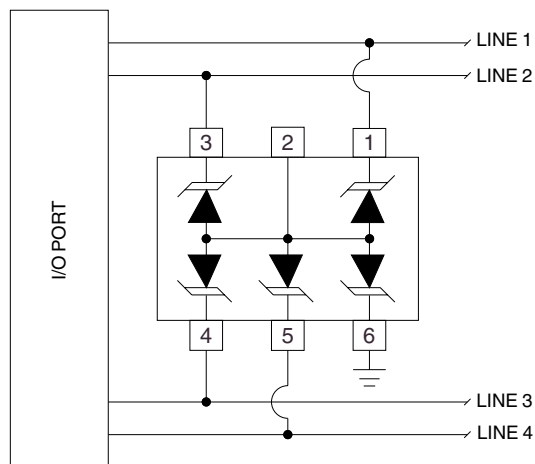


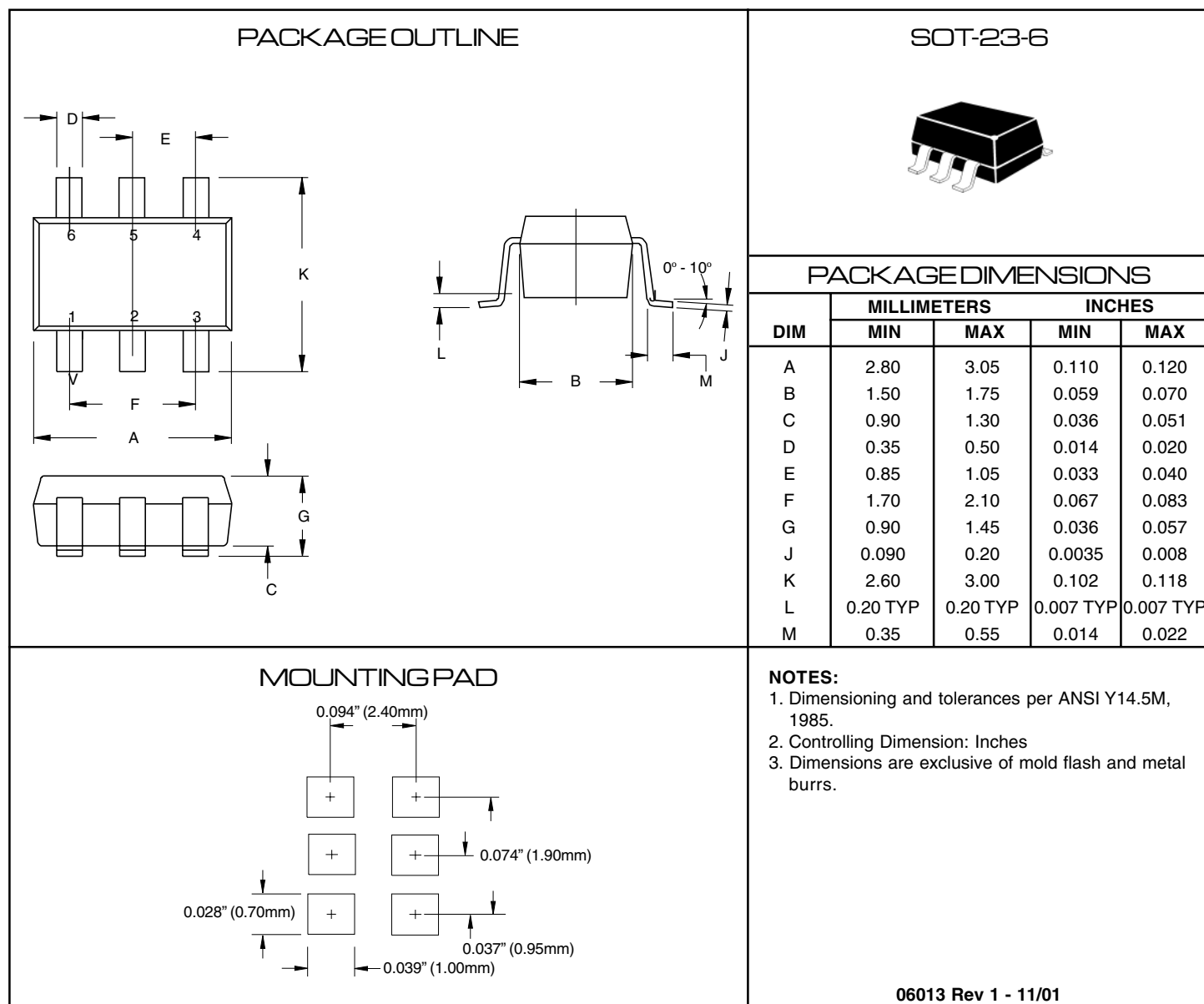
Figure 2 - Bidirectional Configuration Common-Mode I/O Port Protection

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

PACKAGE OUTLINE & DIMENSIONS



TAPE & REEL ORDERING INFORMATION:

Surface mount product is taped and reeled in accordance with EIA-481.
Suffix -T7: 7 Inch Reel - 3000 pieces per reel (i.e., CP05-T7).

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