

PERFORMANCE PROGRAMMABLE GATE ARRAY (PPGA) SERIES

T-46-19-11

- High performance field programmable gate array
- Performance levels comparable to 1.2 - 1.5 μ m CMOS mask-programmable gate arrays.
- True gate array architecture
 - Transistor-level interconnect programmability
 - Gate array macro library
 - Gate array design methodology
- Field programmability based on a unique and proprietary low-impedance antifuse technology
- Four independent clock trees minimize internal clock skew to less than 1.3 μ s
- Efficient memory block implementation
- Built-In IEEE 1149.1 (JTAG) interface
- Automatic or interactive place and route capability for maximum flexibility to fine tune performance and increase gate use
- Design Macrocell library support for popular CAE tools:
 - Mentor Graphics
 - Cadence Verilog
 - ViewLogic
 - Synopsys

DESCRIPTION

With the Performance Programmable Gate Array (PPGA) Series, system designers now have the flexibility to perform the following: experiment with design ideas quickly without having to commit to customized gate arrays; move finished designs into production with little delay; and, when necessary, migrate easily to mask-programmable gate arrays.

Most importantly, the PPGA Series architecture is supported by CAE tools that are compatible with established gate array architecture and design methodologies. This enables design engineers to use familiar gate array tools for schematic entry, synthesis, simulation, timing analysis, and automatic test pattern generation (ATPG).

PPGA PRODUCT LINE

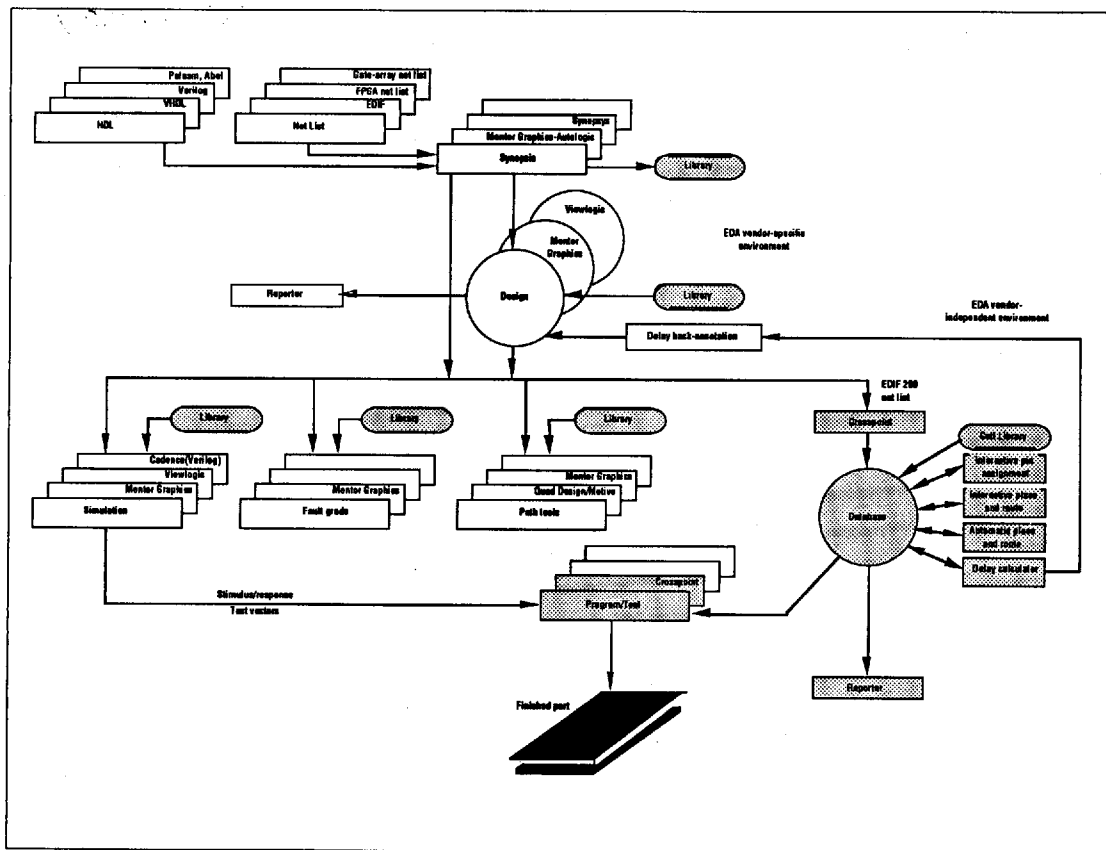
						Package Options				
Part Number	Available Gates	Usable Gates	TPT Count	RLT Count	Max I/O Pads	Quad Flat Packs		PG		
						160	208	155	223	299
CP20420	4,245	2,500 – 3,400	3584	896	130	■		■		
CP20840	8,421	5,100 – 6,700	6696	1674	180	■	■		■	
CP21200	12,125	7,200 – 9,700	9504	2376	219		■		■	
CP21600	16,171	9,600 – 13,000	12,672	3168	250		■			■
CP22000	20,260	12,000 – 16,200	15,876	3969	270		■			■



Means Quality, Service and Speed

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Performance Field Programmable Gate Array circuit designs are supported with popular third-party design tools that are common to mask-programmed gate-array design methodologies. The shaded regions represent the libraries and tools sold and supported by Performance Semiconductor.