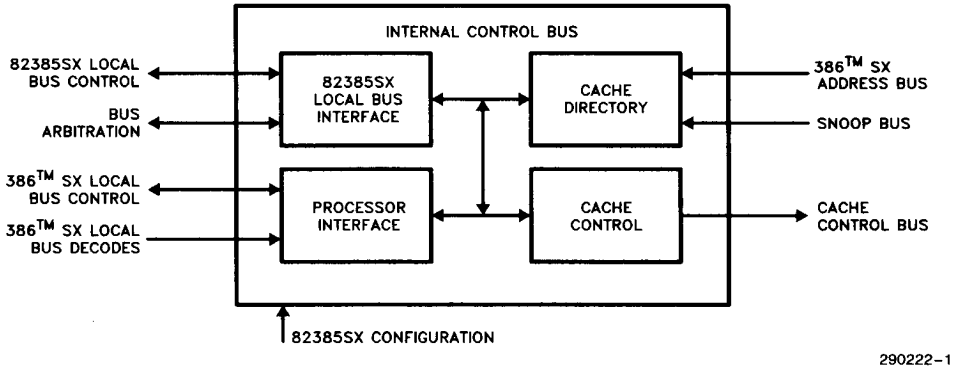
82385SX
HIGH PERFORMANCE CACHE CONTROLLER

- **Improves 386™ SX System Performance**
  - **— Reduces Average CPU Wait States to Nearly Zero**
  - **— Zero Wait State Read Hit**
  - **— Zero Wait State Posted Memory Writes**
  - **— Allows Other Masters to Access the System Bus More Readily**
- **Hit Rates up to 99%**
- **Optimized as 386 SX Companion**
  - **— Simple 386 SX Interface**
  - **— Part of Intel386™-Based Compute Engine Including 387™ SX Math Coprocessor and 82370 Integrated System Peripheral**
  - **— 16 MHz and 20 MHz Operation**
- **Software Transparent**
- **Synchronous Dual Bus Architecture**
  - **— Bus Watching Maintains Cache Coherency**
- **Maps Full 386 SX Address Space**
- **Flexible Cache Mapping Policies**
  - **— Direct Mapped or 2-Way Set Associative Cache Organization**
  - **— Supports Non-Cacheable Memory Space**
  - **— Unified Cache for Code and Data**
- **Integrates Cache Directory and Cache Management Logic**
- **High Speed CHMOS Technology**
  - **— 132-Pin PGA and 132-Lead PQFP**

The 82385SX Cache Controller is a high performance peripheral for Intel's 386™ SX Microprocessor. It stores a copy of frequently accessed code and data from main memory in a zero wait state local cache memory. The 82385SX allows the 386 SX Microprocessor to run near its full potential by reducing the average number of CPU wait states to nearly zero. The dual bus architecture of the 82385SX allows other masters to access system resources while the 386 SX CPU operates locally out of its cache. In this situation, the 82385SX's "bus watching" mechanism preserves cache coherency by monitoring the system bus address lines at no cost to system or local throughput.

The 82385SX is completely software transparent, protecting the integrity of system software. High performance and board space savings are achieved because the 82385SX integrates a cache directory and all cache management logic on one chip.

5



290222-1

82385SX Internal Block Diagram

Intel386™, 386™, 386™ SX, and 387™ SX are trademarks of Intel Corporation.

November 1991
Order Number: 290222-003

CONTENTS

CONTENTS

CONTENTS

CONTENTS

5

1.0 82385SX FUNCTIONAL OVERVIEW

The 82385SX Cache Controller is a high performance peripheral for Intel's 386™ SX microprocessor. This chapter provides an overview of the 82385SX, and of the basic architecture and operation of a 386 SX CPU/82385SX system.

1.1 82385SX Overview

The main function of a cache memory system is to provide fast local storage for frequently accessed code and data. The cache system intercepts 386 SX memory references to see if the required data resides in the cache. If the data resides in the cache (a hit), it is returned to the 386 SX without incurring wait states. If the data is not cached (a miss), the reference is forwarded to the system and the data retrieved from main memory. An efficient cache will yield a high "hit rate" (the ratio of cache hits to total 386 SX accesses), such that the majority of accesses are serviced with zero wait states. The net effect is that the wait states incurred in a relatively infrequent miss are averaged over a large number of accesses, resulting in an average of nearly zero wait states per access. Since cache hits are serviced locally, a processor operating out of its local cache has a much lower "bus utilization" which reduces system bus bandwidth requirements, making more bandwidth available to other bus masters.

The 82385SX Cache Controller integrates a cache directory and all cache management logic required to support an external 16 kbyte cache. The cache directory structure is such that the entire physical address range of the 386 SX is mapped into the cache. Provision is made to allow areas of memory to be set aside as non-cacheable. The user has two cache organization options: direct mapped and 2-way set associative. Both provide the high hit rates necessary to make a large, relatively slow main memory array look like fast, zero wait state memory to the 386 SX.

A good hit rate is an essential ingredient of a successful cache implementation. Hit rate is the measure of how efficient a cache is in maintaining a copy of the most frequently requested code and data. However, efficiency is not the only factor for performance consideration. Just as essential are sound cache management policies. These policies refer to the handling of 386 SX writes, preservation of cache coherency, and ease of system design. The 82385SX's "posted write" capability allows the majority of 386 SX writes, including most non-cacheable cycles, to run with zero wait states, and the 82385SX's "bus watching" mechanism preserves cache coherency with no impact on system performance. Physically, the 82385SX ties directly to the 386 SX with virtually no external logic.

1.2 System Overview I: Bus Structure

A good grasp of bus structure of a 386 SX CPU/82385SX system is essential in understanding both the 82385SX and its role in a 386 SX system. The following is a description of this structure.

1.2.1 386™ SX LOCAL BUS/82385SX LOCAL BUS/SYSTEM BUS

Figure 1-1 depicts the bus structure of a typical 386 SX system. The "386 SX Local Bus" consists of the physical 386 SX address, data, and control busses. The local address and data busses are buffered and/or latched to become the "system" address and data busses. The local control bus is decoded by bus control logic to generate the various system bus read and write commands.

The addition of an 82385SX Cache Controller causes a separation of the 386 SX bus into two distinct busses: the actual 386 SX local bus and the "82385SX Local Bus" (Figure 1-2). The 82385SX local bus is designed to look like the front end of a 386 SX by providing 82385SX local bus equivalents to all appropriate 386 SX signals. The system ties to this "386 SX-like" front end just as it would to an actual 386 SX. The 386 SX simply sees a fast system bus, and the system sees a 386 SX front end with low bus bandwidth requirements. The cache subsystem is transparent to both. Note that the 82385SX local bus is not simply a buffered version of the 386 SX bus, but rather is distinct from, and able to operate in parallel with the 386 SX bus. Other masters residing on either the 82385SX local bus or system bus are free to manage system resources while the 386 SX operates out of its cache.

1.2.2 BUS ARBITRATION

The 82385SX presents the "386 SX-like" interface which is called the 82385SX local bus. Whereas the 386 SX provides a Hold Request/ Hold Acknowledge bus arbitration mechanism via its HOLD and HLDA pins, the 82385SX provides an equivalent mechanism via its BHOLD and BHLDA pins. (These signals are described in Section 3.7.) When another master requests the 82385SX local bus, it issues the request to the 82385SX via BHOLD. Typically, at the end of the current 82385SX local bus cycle, the 82385SX will release the 82385SX local bus and acknowledge the request via BHLDA. The 386 SX is of course free to continue operating on the 386 SX local bus while another master owns the 82385SX local bus.

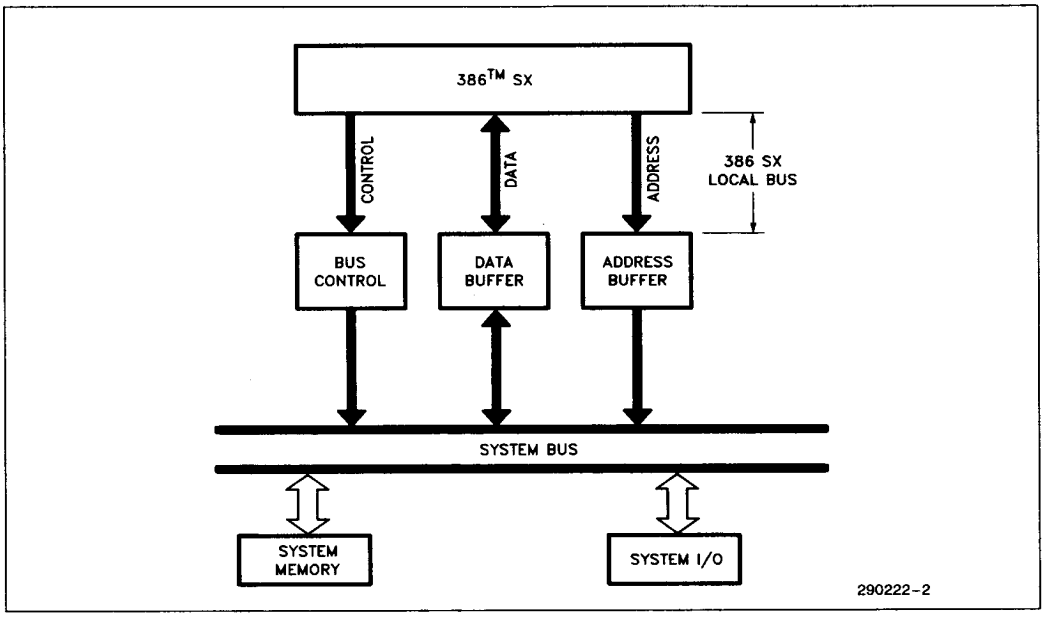


Figure 1-1. 386™ SX System Bus Structure

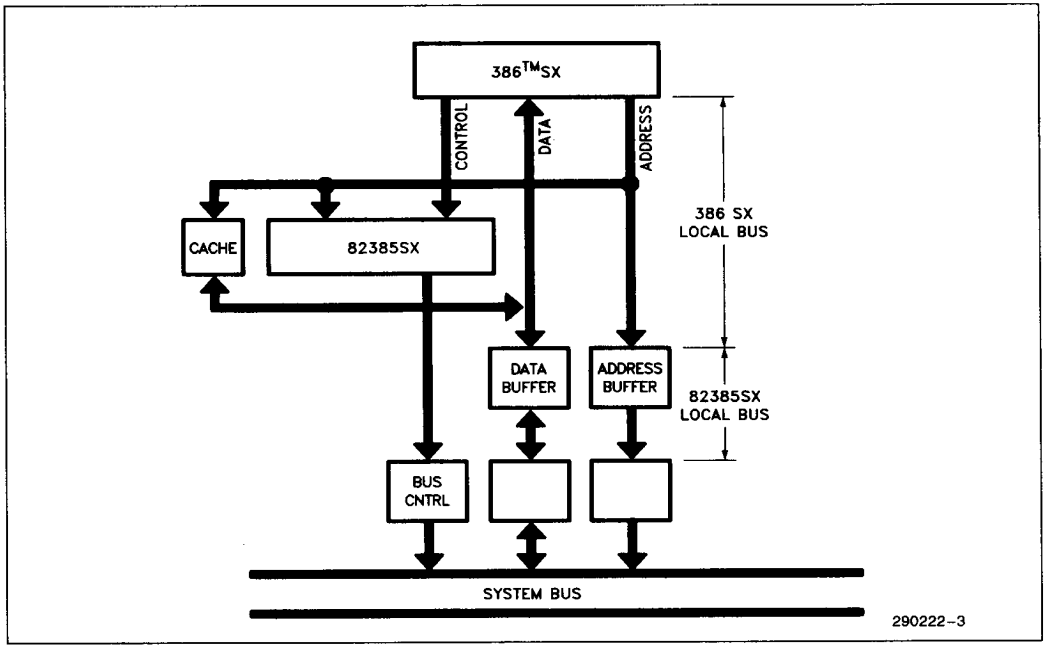


Figure 1-2. 386™ SX and 82385SX System Bus Structure

5

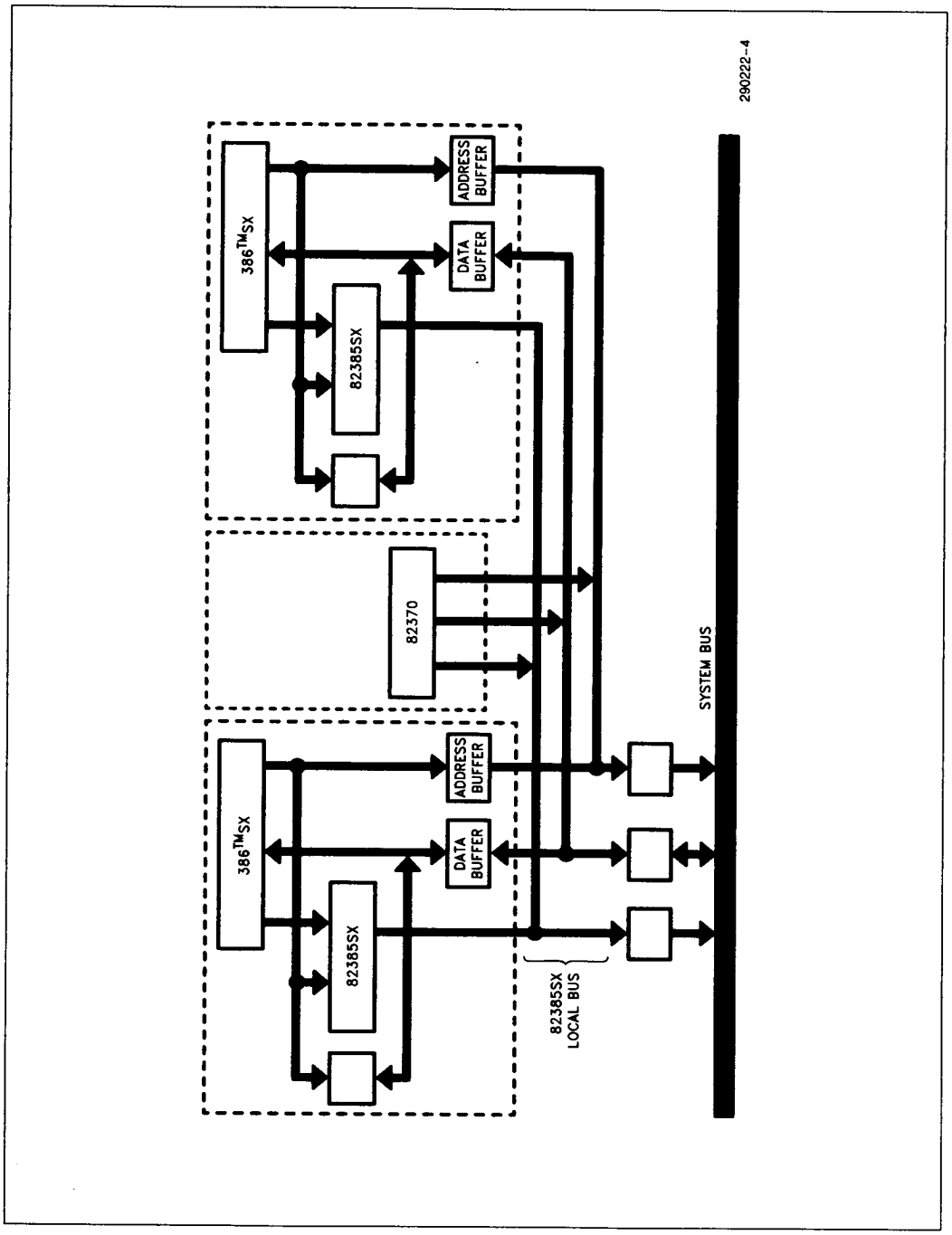


Figure 1-3. Multi-Master/Multi-Cache Environment

1.2.3 MASTER/SLAVE OPERATION

The above 82385SX local bus arbitration discussion is true when the 82385SX is programmed for "Master" mode operation. The user can, however, configure the 82385SX for "Slave" mode operation. (Programming is done via a hardware strap option.) The roles of BHOLD and BHLDA are reversed for an 82385SX in slave mode; BHOLD becomes an output indicating a request to control the bus, and BHLDA becomes an input indicating that a request has been granted. An 82385SX programmed in slave mode drives the 82385SX local bus only when it has requested and subsequently been granted bus control. This allows multiple 386 SX CPU/82385SX subsystems to reside on the same 82385SX local bus (Figure 1-3).

1.2.4 CACHE COHERENCY

Ideally, a cache contains a copy of the most heavily used portions of main memory. To maintain cache "coherency" is to make sure that this local copy is identical to main memory. In a system where multiple masters can access the same memory, there is always a risk that one master will alter the contents of a memory location that is duplicated in the local cache of another master. (The cache is said to contain "stale" data.) One rather restrictive solution is to not allow cache subsystems to cache shared memory. Another simple solution is to flush the cache anytime another master writes to system memory. However, this can seriously degrade system performance as excessive cache flushing will reduce the hit rate of what may otherwise be a highly efficient cache.

The 82385SX preserves cache coherency via "bus watching" (also called snooping), a technique that neither impacts performance nor restricts memory mapping. An 82385SX that is not currently bus master monitors system bus cycles, and when a write cycle by another master is detected (a snoop), the system address is sampled and used to see if the referenced location is duplicated in the cache. If so (a snoop hit), the corresponding cache entry is invalidated, which will force the 386 SX to fetch the up-to-date data from main memory the next time it accesses this modified location. Figure 1-4 depicts the general form of bus watching.

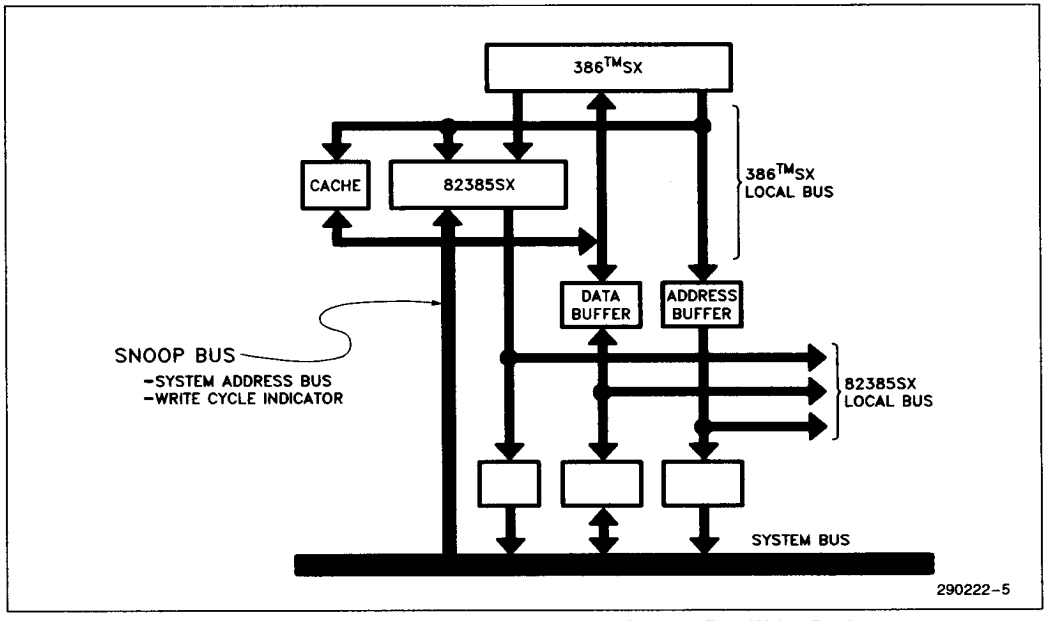


Figure 1-4. 82385SX Bus Watching—Monitor System Bus Write Cycles

5

1.3 System Overview II: Basic Operation

This discussion is an overview of the basic operation of a 386 SX CPU/82385SX system. Items discussed include the 82385SX's response to all 386 SX cycles, including interrupt acknowledges, halts, and shutdowns. Also discussed are non-cacheable and local accesses.

1.3.1 386™ SX MEMORY CODE AND DATA READ CYCLES

1.3.1.1 Read Hits

When the 386 SX initiates a memory code or data read cycle, the 82385SX compares the high order bits of the 386 SX address bus with the appropriate addresses (tags) stored in its on-chip directory. (The directory structure is described in Section 2.1.1) If the 82385SX determines that the requested data is in the cache, it issues the appropriate control signals that direct the cache to drive the requested data onto the 386 SX data bus, where it is read by the 386 SX. The 82385SX terminates the 386 SX cycle without inserting any wait states.

1.3.1.2 Read Misses

If the 82385SX determines that the requested data is not in the cache, the request is forwarded to the 82385SX local bus and the data retrieved from main memory. As the data returns from main memory, it is directed to the 386 SX and also written into the cache. Concurrently, the 82385SX updates the cache directory such that the next time this particular piece of information is requested by the 386 SX, the 82385SX will find it in the cache and return it with zero wait states.

The basic unit of transfer between main memory and cache memory in a cache subsystem is called the line size. In an 82385SX system, the line size is one 16-bit word. During a read miss, both 82385SX local bus byte enables are active. This insures that the 16-bit entry is written into the cache. (The 386 SX simply ignores what it did not request.) In any other type of 386 SX cycle that is forwarded to the 82385SX local bus, the logic levels of the 386 SX byte enables are duplicated on the 82385SX local bus.

The 82385SX does not actively fetch main memory data independently of the 386 SX. The 82385SX is essentially a passive device which only monitors the address bus and activates control signals. The read miss is the only mechanism by which main memory data is copied into the cache and validated in the cache directory.

In an isolated read miss, the number of wait states seen by the 386 SX is that required by the system memory to respond with data plus the cache comparison cycle (hit/miss decision). The cache system must determine that the cycle is a miss before it can begin the system memory access. However, since misses most often occur consecutively, the 82385SX will begin 386 SX address pipelined cycles to effectively "hide" the comparison cycle beyond the first miss (refer to Section 4.1.3).

The 82385SX can execute a memory access on the 82385SX local bus only if it currently owns the bus. If not, an 82385SX in master mode will run the cycle after the current master releases the bus. An 82385SX in slave mode will issue a hold request, and will run the cycle as soon as the request is acknowledged. (This is true for any read or write cycle that needs to run on the 82385SX local bus.)

1.3.2 386™ SX MEMORY WRITE CYCLES

The 82385SX's "posted write" capability allows the majority of 386 SX memory write cycles to run with zero wait states. The primary memory update policy implemented in a posted write is the traditional cache "write through" technique, which implies that main memory is always updated in any memory write cycle. If the referenced location also happens to reside in the cache (a write hit), the cache is updated as well.

Beyond this, a posted write latches the 386 SX address, data, and cycle definition signals, and the 386 SX local bus is terminated without any wait states, even though the corresponding 82385SX local bus cycle is not yet completed, or perhaps not even started. A posted write is possible because the 82385SX's bus state machine, which is almost identical to the 386 SX bus state machine, is able to run 82385SX local bus cycles independently of the 386 SX. The only time the 386 SX sees write cycle wait states is when a previously latched (posted) write has not yet been completed on the 82385SX local bus or during an I/O write (which is not posted). An 386 SX write can be posted even if the 82385SX does not currently own the 82385SX local bus. In this case, an 82385SX in master mode will run the cycle as soon as the current master releases the bus, and an 82385SX in slave mode will request the bus and run the cycle when the request is acknowledged. The 386 SX is free to continue operating out of its cache (on the 386 SX local bus) during this time.

1.3.3 NON-CACHEABLE CYCLES

Non-cacheable cycles fall into one of two categories: cycles decoded as non-cacheable, and cycles

that are by default non-cacheable according to the 82385SX's design. All non-cacheable cycles are forwarded to the 82385SX local bus. Non-cacheable cycles have no effect on the cache or cache directory.

The 82385SX allows the system designer to define areas of main memory as non-cacheable. The 386 SX address bus is decoded and the decode output is connected to the 82385SX's non-cacheable access (NCA#) input. This decoding is done in the first 386 SX bus state in which the non-cacheable cycle address becomes available. Non-cacheable read cycles resemble cacheable read miss cycles, except that the cache and cache directory are unaffected. NCA# defined non-cacheable writes, like most writes, are posted.

The 82385SX defines certain cycles as non-cacheable without using its non-cacheable access input. These include I/O cycles, interrupt acknowledge cycles, and halt/shutdown cycles. I/O reads and interrupt acknowledge cycles execute as any other non-cacheable read. I/O write cycles are not posted. The 386 SX is not allowed to continue until a ready signal is returned from the system. Halt/Shutdown cycles are posted. During a halt/shutdown condition, the 82385SX local bus duplicates the behavior of the 386 SX, including the ability to recognize and respond to a BHOLD request. (The 82385SX's bus watching mechanism is functional in this condition.)

1.3.4 386™ SX LOCAL BUS CYCLES

386 SX Local Bus Cycles are accesses to resources on the 386 SX local bus other than to the 82385SX itself. The 82385SX simply ignores these accesses: they are neither forwarded to the system nor do they affect the cache. The designer sets aside memory and/or I/O space for local resources by decoding the 386 SX address bus and feeding the decode to the 82385SX's local bus access (LBA#) input. The designer can also decode the 386 SX cycle definition signals to keep specific 386 SX cycles from being forwarded to the system. For example, a multiprocessor design may wish to capture and remedy a 386 SX shutdown locally without having it detected by the rest of the system. Note that in such a design, the local shutdown cycle must be terminated by local bus control logic. The 387 SX Math Coprocessor is considered a 386 SX local bus resource, but it need not be decoded as such by the user since the 82385SX is able to internally recognize 387 SX accesses via the M/IO# and A23 pins.

1.3.5 SUMMARY OF 82385SX RESPONSE TO ALL 386™ SX CYCLES

Table 1-1 summarizes the 82385SX response to all 386 SX bus cycles, as conditioned by whether or not the cycle is decoded as local or non-cacheable. The table describes the impact of each cycle on the cache and on the cache directory, and whether or not the cycle is forwarded to the 82385SX local bus. Whenever the 82385SX local bus is marked "IDLE", it implies that this bus is available to other masters.

1.3.6 BUS WATCHING

As previously discussed, the 82385SX "qualifies" a 386 SX bus cycle in the first bus state in which the address and cycle definition signals of the cycle become available. The cycle is qualified as read or write, cacheable or non-cacheable, etc. Cacheable cycles are further classified as hit or miss according to the results of the cache comparison, which accesses the 82385SX directory and compares the appropriate directory location (tag) to the current 386 SX address. If the cycle turns out to be non-cacheable or a 386 SX local bus access, the hit/miss decision is ignored. The cycle qualification requires one 386 SX state. Since the fastest 386 SX access is two states, the second state can be used for bus watching.

When the 82385SX does not own the system bus, it monitors system bus cycles. If another master writes into main memory, the 82385SX latches the system address and executes a cache look-up to see if the altered main memory location resides in the cache. If so (a snoop hit), the cache entry is marked invalid in the cache directory. Since the directory is at most only being used every other state to qualify 386 SX accesses, snoop look-ups are interleaved between 386 SX local bus look-ups. The cache directory is time multiplexed between the 386 SX address and the latched system address. The result is that all snoops are caught and serviced without slowing down the 386 SX, even when running zero wait state hits on the 386 SX local bus.

1.3.7 CACHE FLUSH

The 82385SX offers a cache flush input. When activated, this signal causes the 82385SX to invalidate all data which had previously been cached. Specifically, all tag valid bits are cleared. (Refer to the 82385SX directory structure in Section 2.1.1.) There-

Table 1-1. 82385SX Response to 386™ SX Cycles

386 SX Bus Cycle Definition					82385SX Response when Decoded as Cacheable			82385SX Response when Decoded as Non-Cacheable			82385SX Response when Decoded as a 386SX Local Bus Access		
M/IO#	D/C#	W/R#	386 SX Cycle		Cache	Cache Directory	82385SX Local Bus	Cache	Cache Directory	82385SX Local Bus	Cache	Cache Directory	82385SX Local Bus
0	0	0	INT ACK	N/A	—	—	INT ACK	—	—	INT ACK	—	—	IDLE
0	0	1	UNDEFINED	N/A			UNDEFINED			UNDEFINED			IDLE
0	1	0	I/O READ	N/A	—	—	I/O READ	—	—	I/O READ	—	—	IDLE
0	1	1	I/O WRITE	N/A	—	—	I/O WRITE	—	—	I/O WRITE	—	—	IDLE
1	0	0	MEM CODE READ	HIT	CACHE READ	—	IDLE	—	—	MEM CODE READ	—	—	IDLE
				MISS	CACHE WRITE	DATA VALIDATION	MEM CODE READ						
1	0	1	HALT/ SHUTDOWN	N/A	—	—	HALT/ SHUTDOWN	—	—	HALT/ SHUTDOWN	—	—	IDLE
1	1	0	MEM DATA READ	HIT	CACHE READ	—	IDLE	—	—	MEM DATA READ	—	—	IDLE
				MISS	CACHE WRITE	DATA VALIDATION	MEM DATA READ						
1	1	1	MEM DATA WRITE	HIT	CACHE WRITE	—	MEM DATA WRITE	—	—	MEM DATA WRITE	—	—	IDLE
				MISS	—	—	MEM DATA WRITE						

NOTES:
- A dash (—) indicates that the cache and cache directory are unaffected. This table does not reflect how an access affects the LRU bit.
- An "IDLE" 82385SX Local Bus implies that this bus is available to other masters.
- The 82385SX's response to 387™ SX accesses is the same as when decoded as a 386 SX Local Bus Access.
- The only other operations that affect the cache directory are:

1. RESET or Cache Flush—all tag valid bits cleared.
2. Snoop Hit—corresponding line valid bit cleared.

fore, the cache is empty and subsequent cycles are misses until the 386 SX begins repeating the new accesses (hits). The primary use of the FLUSH input is for diagnostics and multi-processor support.

NOTE:
The use of this pin as a coherency mechanism may impact software transparency.

2.0 82385SX CACHE ORGANIZATION

The 82385SX supports two cache organizations: a simple direct mapped organization and a slightly more complex, higher performance two way set associative organization. The choice is made by strapping an 82385SX input (2W/D#) either high or low. This chapter describes the structure and operation of both organizations.

2.1 Direct Mapped Cache

2.1.1 DIRECT MAPPED CACHE STRUCTURE AND TERMINOLOGY

Figure 2-1 depicts the relationship between the 82385SX's internal cache directory, the external cache memory, and the 386 SX's physical address space. The 386 SX address space can conceptually be thought of as cache "pages" each being 8K words (16 Kbytes) deep. The page size matches the cache size. The cache can be further divided into 1024 (0 thru 1023) sets of eight words (8 x 16 bits). Each 16-bit word is called a "line". The unit of transfer between the main memory and cache is one line.

Each block in the external cache has an associated 19-bit entry in the 82385SX's internal cache directory. This entry has three components: a 10-bit "tag", a "tag valid" bit, and eight "line valid" bits. The tag acts as a main memory page number (10 tag bits support 2^{10} pages). For example, if line 9 of page 2 currently resides in the cache, then a binary 2 is stored in the Set 1 tag field. (For any 82385SX direct mapped cache page in main memory, Set 0 consists of lines 0–7, Set 1 consists of lines 8–15, etc. Line 9 is shaded in Figure 2-1.) An important characteristic of a direct mapped cache is that line 9 of any page can only reside in line 9 of the cache. All identical page offsets map to a single cache location.

The data in a cache set is considered valid or invalid depending on the status of its tag valid bit. If clear, the entire set is considered invalid. If true, an individual line within the set is considered valid or invalid depending on the status of its line valid bit.

The 82385SX sees the 386 SX address bus (A1–A23) as partitioned into three fields: a 10-bit "tag"

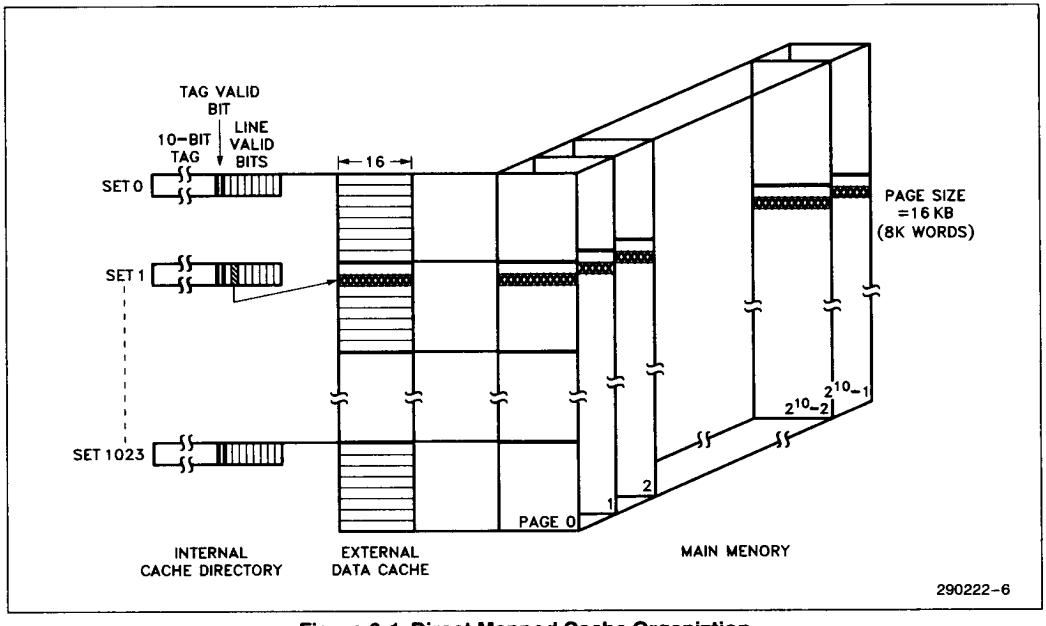


Figure 2-1. Direct Mapped Cache Organiztion

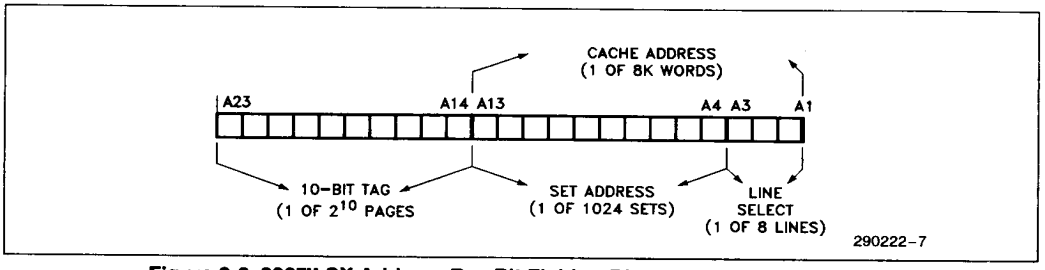


Figure 2-2. 386™ SX Address Bus Bit Fields—Direct Mapped Organization

field (A14–A23), a 10-bit "set address" field (A4–A13), and a 3-bit "line select" field (A1–A3). (See Figure 2-2.) The lower 13 address bits (A1–A13) also serve as the "cache address" which directly selects one of 8K words in the external cache.

2.1.2 DIRECT MAPPED CACHE OPERATION

The following is a description of the interaction between the 386 SX, cache, and cache directory.

2.1.2.1 Read Hits

When the 386 SX initiates a memory read cycle, the 82385SX uses the 10-bit set address to select one of 1024 directory entries, and the 3-bit line select field to select one of eight line valid bits within the entry. The 13-bit cache address selects the corresponding word in the cache. The 82385SX compares the 10-bit tag field (A14–A23 of the 386 SX access) with the tag stored in the selected directory entry. If the tag and upper address bits match, and if both the tag and appropriate line valid bits are set, the result is a hit, and the 82385SX directs the cache to drive the selected word onto the 386 SX data bus. A read hit does not alter the contents of the cache or directory.

2.1.2.2 Read Misses

A read miss can occur in two ways. The first is known as a "line" miss, and occurs when the tag and upper address bits match and the tag valid bit is set, but the line valid bit is clear. The second is called a "tag" miss, and occurs when either the tag and upper address bits do not match, or the tag valid bit is clear. (The line valid bit is a "don't care" in a tag miss.) In both cases, the 82385SX forwards the 386 SX reference to the system, and as the returning data is fed to the 386 SX, it is written into the cache and validated in the cache directory.

In a line miss, the incoming data is validated simply by setting the previously clear line valid bit. In a tag miss, the upper address bits overwrite the previously stored tag, the tag valid bit is set, the appropriate line valid bit is set, and the other seven line valid bits are cleared. Subsequent tag hits with line misses will only set the appropriate line valid bit. (Any data associated with the previous tag is no longer considered resident in the cache.)

2.1.2.3 Other Operations That Affect the Cache and Cache Directory

The other operations that affect the cache and/or directory are write hits, snoop hits, cache flushes, and 82385SX resets. In a write hit, the cache is updated along with main memory, but the directory is unaffected. In a snoop hit, the cache is unaffected, but the affected line is invalidated by clearing its line valid bit in the directory. Both an 82385SX reset and cache flush clear all tag valid bits.

When a 386 SX CPU/82385SX system "wakes up" upon reset, all tag valid bits are clear. At this point, a read miss is the only mechanism by which main memory data is copied into the cache and validated in the cache directory. Assume an early 386 SX code access seeks (for the first time) line 9 of page 2. Since the tag valid bit is clear, the access is a tag miss, and the data is fetched from main memory. Upon return, the data is fed to the 386 SX and simultaneously written into line 9 of the cache. The set directory entry is updated to show this line as valid. Specifically, the tag and appropriate line valid bits are set, the remaining seven line valid bits cleared, and binary 2 written into the tag. Since code is sequential in nature, the 386 SX will likely next want line 10 of page 2, then line 11, and so on. If the 386 SX sequentially fetches the next six lines, these fetches will be line misses, and as each is fetched from main memory and written into the cache, its corresponding line valid bit is set. This is the basic flow of events that fills the cache with valid data. Only after a piece of data has been copied into the cache and validated can it be accessed in a zero wait state read hit. Also, a cache entry must have been validated before it can be subsequently altered by a write hit, or invalidated by a snoop hit.

An extreme example of "trashing" is if line 9 of page two is an instruction to jump to line 9 of page one, which is an instruction to jump back to line 9 of page two. Trashing results from the direct mapped cache characteristic that all identical page offsets map to a single cache location. In this example, the page one access overwrites the cached page two data, and the page two access overwrites the cached page one data. As long as the code jumps back and forth the hit rate is zero. This is of course an extreme case. The effect of trashing is that a direct mapped cache exhibits a slightly reduced overall hit rate as compared to a set associative cache of the same size.

2.2 Two Way Set Associative Cache

2.2.1 TWO WAY SET ASSOCIATIVE CACHE STRUCTURE AND TERMINOLOGY

Figure 2-3 illustrates the relationship between the directory, cache, and 386 SX address space. Whereas the direct mapped cache is organized as one bank of 8K words, the two way set associative cache is organized as two banks (A and B) of 4K words each. The page size is halved, and the number of pages doubled. (Note the extra tag bit.) The cache now has 512 sets in each bank. (Two banks times 512 sets gives a total of 1024. The structure can be thought of as two half-sized direct mapped caches in parallel.) The performance advantage over a direct mapped cache is that all identical page offsets map to two cache locations instead of one, reducing the potential for thrashing. The 82385SX's partitioning of the 386 SX address bus is depicted in Figure 2-4.

2.2.2 LRU REPLACEMENT ALGORITHM

The two way set associative directory has an additional feature: the "least recently used" or LRU bit. In the event of a read miss, either bank A or bank B will be updated with new data. The LRU bit flags the candidate for replacement. Statistically, of two blocks of data, the block most recently used is the block most likely to be needed again in the near future. By flagging the least recently used block, the 82385SX ensures that the cache block replaced is the least likely to have data needed by the CPU.

2.2.3 TWO WAY SET ASSOCIATIVE CACHE OPERATION

2.2.3.1 Read Hits

When the 386 SX initiates a memory read cycle, the 82385SX uses the 9-bit set address to select one of 512 sets. The two tags of this set are simultaneously compared with A13–A23, both tag valid bits checked, and both appropriate line valid bits checked. If either comparison produces a hit, the corresponding cache bank is directed to drive the selected word onto the 386 SX data bus. (Note that both banks will never concurrently cache the same main memory location.) If the requested data resides in bank A, the LRU bit is pointed toward B. If B produces the hit, the LRU bit is pointed toward A.

2.2.3.2 Read Misses

As in direct mapped operation, a read miss can be either a line or tag miss. Let's start with a tag miss example. Assume the 386 SX seeks line 9 of page 2, and that neither the A or B directory produces a tag match. Assume also, as indicated in Figure 2-3, that the LRU bit points to A. As the data returns from main memory, it is loaded into offset 9 of bank A. Concurrently, this data is validated by updating the set 1 directory entry for bank A. Specifically, the upper address bits overwite the previous tag, the tag valid bit is set, the appropriate line valid bit is set, and the other seven line valid bits cleared. Since this data is the most recently used, the LRU bit is turned toward B. No change to bank B occurs.

If the next 386 SX request is line 10 of page two, the result will be a line miss. As the data returns from main memory, it will be written into offset 10 of bank A (tag hit/line miss in bank A), and the appropriate line valid bit will be set. A line miss in one bank will cause the LRU bit to point to the other bank. In this example, however, the LRU bit has already been turned toward B.

2.2.3.3 Other Operations That Affect the Cache and Cache Directory

Other operations that affect the cache and cache directory are write hits, snoop hits, cache flushes, and 82385SX resets. A write hit updates the cache along with main memory. If directory A detects the hit, bank A is updated. If directory B detects the hit, bank B is updated. If one bank is updated, the LRU bit is pointed towards the other.

If a snoop hit invalidates an entry, for example, in cache bank A, the corresponding LRU bit is pointed toward A. This insures that invalid data is the prime candidate for replacement in a read miss. Finally, resets and flushes behave just as they do in a direct mapped cache, clearing all tag valid bits.

3.0 82385SX PIN DESCRIPTION

The 82385SX creates the 82385SX local bus, which is a functional 386 SX interface. To facilitate under-

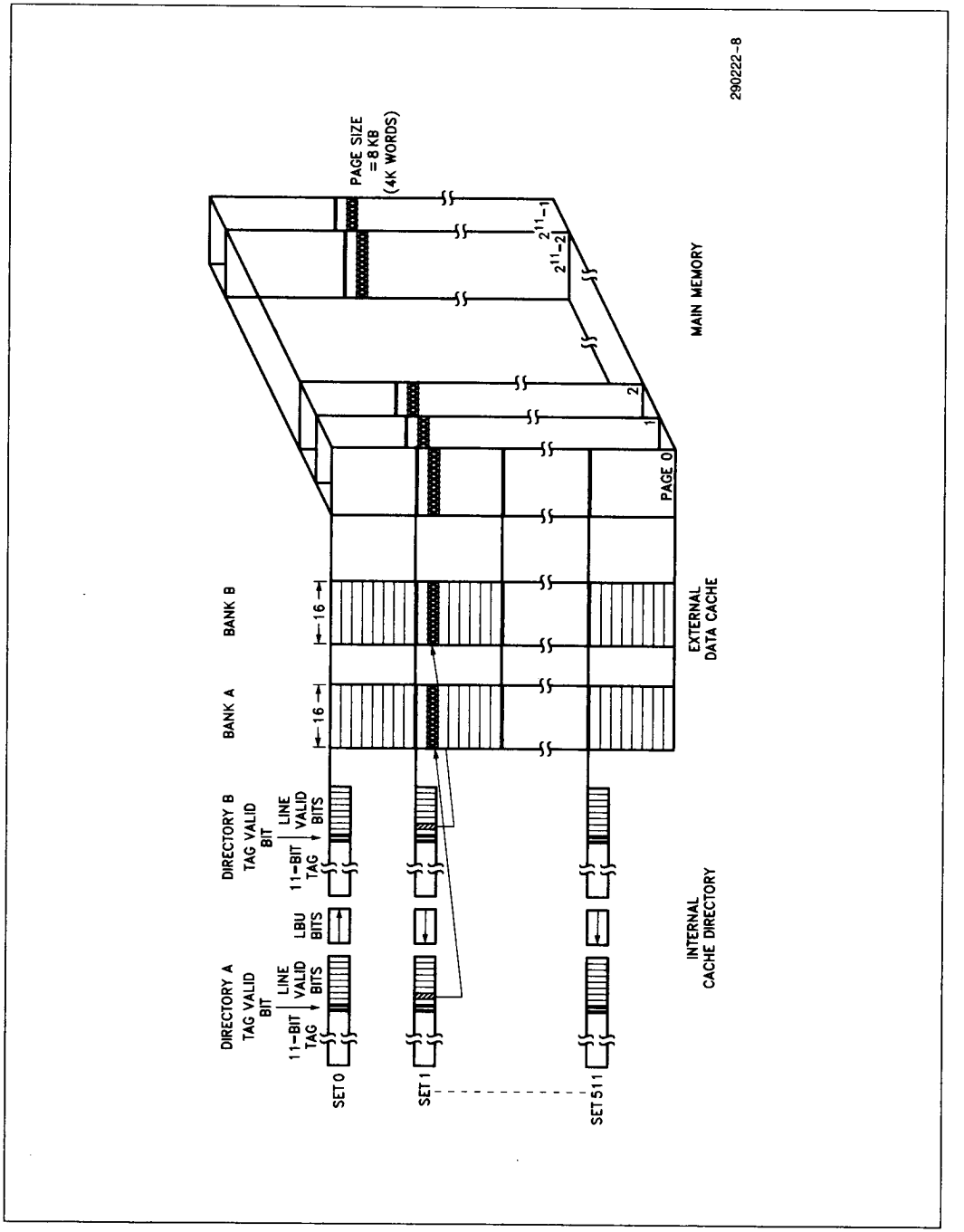


Figure 2-3. Two-Way Set Associative Cache Organization

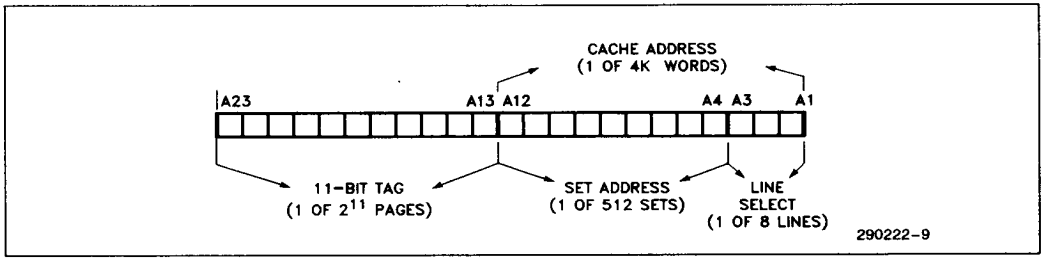


Figure 2-4. 386™ SX Address Bus Bit Fields—Two-Way Set Associative Organization

standing, 82385SX local bus signals go by the same name as their 386 SX equivalents, except that they are preceded by the letter "B". The 82385SX local bus equivalent to ADS# is BADS#, the equivalent to NA# is BNA#, etc. This convention applies to bus states as well. For example, BT1P is the 82385SX local bus state equivalent to the 386 SX T1P state.

3.1 386™ SX CPU/82385SX Interface Signals

These signals form the direct interface between the 386 SX and the 82385SX.

3.1.1 386™ SX CPU/82385SX Clock (CLK2)

CLK2 provides the fundamental timing for a 386 SX CPU/82385SX system, and is driven by the same source that drives the 386 SX CLK2 input. The 82385SX, like the 386 SX, divides CLK2 by two to generate an internal "phase indication" clock. (See Figure 3-1.) The CLK2 period whose rising edge drives the internal clock low is called PHI1, and the CLK2 period that drives the internal clock high is called PHI2. A PHI1–PHI2 combination (in that order) is known as a "T" state, and is the basis for 386 SX bus cycles.

3.1.2 386™ SX CPU/82385SX RESET (RESET)

This input resets the 82385SX, bringing it to an initial known state, and is driven by the same source that drives the 386 SX RESET input. A reset effectively flushes the cache by clearing all cache directory tag valid bits. The falling edge of RESET is synchronized to CLK2, and used by the 82385SX to properly establish the phase of its internal clock. (See Figure 3-2.) Specifically, the second internal phase following the falling edge of RESET is PHI2.

5

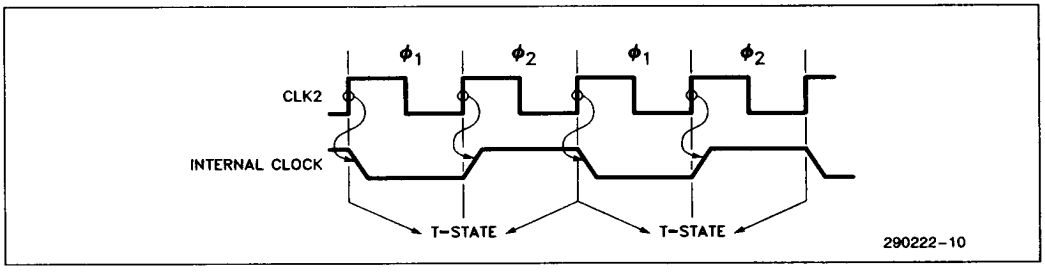


Figure 3-1. CLK2 and Internal Clock

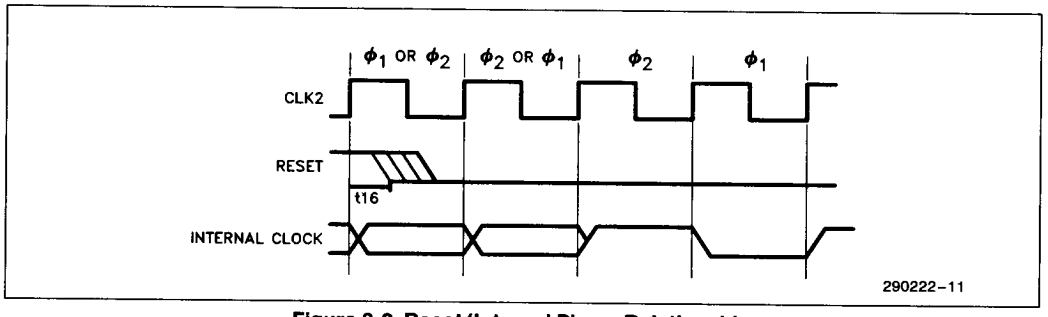


Figure 3-2. Reset/Internal Phase Relationship

3.1.3 386™ SX CPU/82385SX ADDRESS BUS (A1–A23), BYTE ENABLES (BHE#, BLE#), AND CYCLE DEFINITION SIGNALS (M/IO#, D/C#, W/R#, LOCK#)

The 82385SX directly connects to these 386 SX outputs. The 386 SX address bus is used in the cache directory comparison to see if data referenced by 386 SX resides in the cache, and the byte enables inform the 82385SX as to which portions of the data bus are involved in a 386 SX cycle. The cycle definition signals are decoded by the 82385SX to determine the type of cycle the 386 SX is executing.

3.1.4 386™ SX CPU/82385SX ADDRESS STATUS (ADS#) AND READY INPUT (READYI#)

ADS#, a 386 SX output, tells the 82385SX that new address and cycle definition information is available. READYI#, an input to both the 386 SX (via the 386 SX READY# input pin) and 82385SX, indicates the completion of a 386 SX bus cycle. ADS# and READYI# are used to track the 386 SX bus state.

3.1.5 386™ SX NEXT ADDRESS REQUEST (NA#)

This 82385SX output controls 386 SX pipelining. It can be tied directly to the 386 SX NA# input, or it can be logically "AND"ed with other 386 SX local bus next address requests.

3.1.6 READY OUTPUT (READYO#) AND BUS READY ENABLE (BRDYEN#)

The 82385SX directly terminates all but two types of 386 SX bus cycles with its READYO# output. 386 SX local bus cycles must be terminated by the local device being accessed. This includes devices decoded using the 82385SX LBA# signal and 387 accesses. The other cycles not directly terminated by the 82385SX are 82385SX local bus reads, specifically cache read misses and non-cacheable reads. (Recall that the 82385SX forwards and runs such cycles on the 82385SX bus.) In these cycles the signal that terminates the 82385SX local bus access is BREADY# which is gated through to the 386 SX local bus such that the 386 SX and 82385SX local bus cycles are concurrently terminated. BRDYEN# is used to gate the BREADY# signal to the 386 SX.

3.2 Cache Control Signals

These 82385SX outputs control the external 16 KB cache data memory.

3.2.1 CACHE ADDRESS LATCH ENABLE (CALEN)

This signal controls the latch (typically an F or AS series 74373) that resides between the low order 386 SX address bits and the cache SRAM address inputs. (The outputs of this latch are the "cache address" described in the previous chapter.) When CALEN is high the latch is transparent. The falling edge of CALEN latches the current inputs which remain applied to the cache data memory until CALEN returns to an active high state.

3.2.2 CACHE TRANSMIT/RECEIVE (CT/R#)

This signal defines the direction of an optional data transceiver (typically an F or AS series 74245) between the cache and 386 SX data bus. When high, the transceiver is pointed towards the 386 SX local data bus (the SRAMs are output enabled). When low, the transceiver points towards the cache data memory. A transceiver is required if the cache is designed with SRAMs that lack an output enable control. A transceiver may also be desirable in a system that has a heavily loaded 386 SX local data bus. These devices are not necessary when using SRAMs which incorporate an output enable.

3.2.3 CACHE CHIP SELECTS (CS0#, CS1#)

These active low signals tie to the cache SRAM chip selects, and individually enable both bytes of the 16-bit wide cache. CS0# enables D0–D7 and CS1# enables D8–D15. During read hits, both bytes are enabled regardless of whether or not the 386 SX byte enables are active. (The 386 SX ignores what it did not request.) Also, both cache bytes are enabled in a read miss so as to update the cache with a complete line (word). In a write hit, only the cache bytes that correspond to active byte enables are selected. This prevents cache data from being corrupted in a partial word write.

3.2.4 CACHE OUTPUT ENABLES (COEA#, COEB#) AND WRITE ENABLES (CWEA#, CWEB#)

COEA# and COEB# are active low signals which tie to the cache SRAM or Transceiver output enables and respectively enable cache bank A or B. The state of DEFOE# (define cache output enable), an 82385SX configuration input, determines the functional definition of COEA# and COEB#.

If DEFOE# = V_{IL}, in a two-way set associative cache, either COEA# or COEB# is active during read hit cycles only, depending on which bank is selected. In a direct mapped cache, both are activated during read hits, so the designer is free to use either one. This COEx# definition best suits cache SRAMs with output enables.

If DEFOE# = V_{IH}, COEx# is active during a read hit, read miss (cache update) and write hit cycles only. This COEx# definition best suits cache SRAMs without output enables. In such systems, transceivers are needed and their output enables must be active for writing, as well as reading, the cache SRAMs.

CWEA# and CWEB# are active low signals which tie to the cache SRAM write enables, and respectively enable cache bank A or B to receive data from the 386 SX data bus (386 SX write hit or read miss update). In a two-way set associative cache, one or the other is enabled in a read miss or write hit. In a direct mapped cache, both are activated, so the designer is free to use either one.

The various cache configurations supported by the 82385SX are described in Section 4.2.1.

3.3 386™ SX Local Bus Decode Inputs

These 82385SX inputs are generated by decoding the 386 SX address and cycle definition lines. These active low inputs are sampled at the end of the first state in which the address of a new 386 SX cycle becomes available. (T1 or first T2P.)

3.3.1 386™ SX LOCAL BUS ACCESS (LBA#)

This input identifies a 386 SX access as directed to a resource (other than the cache) on the 386 SX local bus. (The 387 SX Math Coprocessor is considered a 386 SX local bus resource, but LBA# need not be generated as the 82385SX internally decodes 387 SX accesses.) The 82385SX simply ignores these cycles. They are neither forwarded to the system nor do they affect the cache or cache directory. Note that LBA# has priority over all other types of cycles. If LBA# is asserted, the cycle is interpreted as a 386 SX local bus access, regardless of the cycle type or status of NCA#. This allows any 386 SX cycle (memory, I/O, interrupt acknowledge, etc.) to be kept on the 386 SX local bus if desired.

3.3.2 NON-CACHEABLE ACCESS (NCA#)

This active low input identifies a 386 SX cycle as non-cacheable. The 82385SX forwards non-cacheable cycles to the 82385SX local bus and runs them. The cache and cache directory are unaffected.

NCA# allows a designer to set aside a portion of main memory as non-cacheable. Potential applications include memory-mapped I/O and systems where multiple masters access dual ported memory via different busses. Another possibility makes use of the 386 SX D/C# output. The 82385SX by default implements a unified code and data cache, but driving NCA# directly by D/C# creates a data only cache. If D/C# is inverted first, the result is a code only cache.

3.4 82385SX Local Bus Interface Signals

The 82385SX presents an "386 SX-like" front end to the system, and the signals discussed in this section are 82385SX local bus equivalents to actual 386 SX signals. These signals are named with respect to their 386 SX counterparts, but with the letter "B" appended to the front.

Note that the 82385SX itself does not have equivalent output signals to the 386 SX data bus (D0–D15) address bus (A1–A23), and cycle definition signals (M/IO#, D/C#, W/R#). The 82385SX data bus (BD0–BD15) is actually the system side of a latching transceiver, and the 82385SX address bus and cycle definition signals (BA1–BA23, BM/IO#, BD/C#,

BW/R#) are the outputs of an edge-triggered latch. The signals that control this data transceiver and address latch are discussed in Section 3.5.

3.4.1 82385SX BUS BYTE ENABLES (BBHE#, BBLE#)

BBHE# and BBLE# are the 82385SX local bus equivalents to the 386 SX byte enables. In a cache read miss, the 82385SX drives both signals low, regardless of whether or not the 386 SX byte enables are active. This insures that a complete line (word) is fetched from main memory for the cache update. In all other 82385SX local bus cycles, the 82385SX duplicates the logic levels of the 386 SX byte enables. The 82385SX tri-states these outputs when it is not the current bus master.

3.4.2 82385SX BUS LOCK (BLOCK#)

BLOCK# is the 82385SX local bus equivalent to the 386 SX LOCK# output, and distinguishes between locked and unlocked cycles. When the 386 SX runs a locked sequence of cycles (and LBA# is negated), the 82385SX forwards and runs the sequence on the 82385SX local bus, regardless of whether any locations referenced in the sequence reside in the cache. A read hit will be run as if it is a read miss, but a write hit will update the cache as well as being completed to system memory. In keeping with 386 SX behavior, the 82385SX does not allow another master to interrupt the sequence. BLOCK# is tri-stated when the 82385SX is not the current bus master.

3.4.3 82385SX BUS ADDRESS STATUS (BADS#)

BADS# is the 82385SSX local bus equivalent of ADS#, and indicates that a valid address (BA1–BA23, BBHE#, BBLE#) and cycle definition (BM/IO#, BW/R#, BD/C#) are available. It is asserted in BT1 and BT2P states, and is tri-stated when the 82385SX does not own the bus.

3.4.4 82385SX BUS READY INPUT (BREADY#)

82385SX local bus cycles are terminated by BREADY#, just as 386 SX cycles are terminated by the 386 SX READY# input. In 82385SX local bus read cycles, BREADY# is gated by BRDYEN# onto the 386 SX local bus, such that it terminates both the 386 SX and 82385SX local bus cycles.

3.4.5 82385SX BUS NEXT ADDRESS REQUEST (BNA#)

BNA# is the 82385SX local bus equivalent to the 386 SX NA# input, and indicates that the system is prepared to accept a pipelined address and cycle definition. If BNA# is asserted and the new cycle information is available, the 82385SX begins a pipelined cycle on the 82385SX local bus.

3.5 82385SX Bus Data Transceiver and Address Latch Control Signals

The 82385SX data bus is the system side of a latching transceiver (typically for F or AS series 74646), and the 82385SX address bus and cycle definition signals are the outputs of an edge-triggered latch (F or AS series 74374). The following is a discussion of the 82385SX outputs that control these devices. An important characteristic of these signals and the devices they control is that they ensure that BD0–BD15, BA1–BA23, BM/IO#, BD/C# and BW/R# reproduce the functionality and timing behavior of their 386 SX equivalents.

3.5.1 LOCAL DATA STROBE (LDSTB), DATA OUTPUT ENABLE (DOE#), AND BUS TRANSMIT/RECEIVE (BT/R#)

These signals control the latching data transceiver. BT/R# defines the transceiver direction. When high, the transceiver drives the 82385SX data bus in write cycles. When low, the transceiver drives the 386 SX data bus in 82385SX local bus read cycles. DOE# enables the transceiver outputs.

The rising edge of LDSTB latches the 386 SX data bus in all write cycles. The interaction of this signal and the latching transceiver is used to perform the 82385SX's posted write capability.

3.5.2 BUS ADDRESS CLOCK PULSE (BACP) AND BUS ADDRESS OUTPUT ENABLE (BAOE#)

These signals control the latch that drives BA1–BA23, BM/IO#, BW/R#, and BD/C#. In any 386 SX cycle that is forwarded to the 82385SX local bus, the rising edge of BACP latches the 386 SX address and cycle definition signals. BAOE# enables the latch outputs when the 82385SX is the current bus master and disables them otherwise.

3.6 Status and Control Signals

3.6.1 CACHE MISS INDICATION (MISS#)

This output accompanies cacheable read and write miss cycles. This signal transitions to its active low state when the 82385SX determines that a cacheable 386 SX access is a miss. Its timing behavior

follows that of the 82385SX local bus cycle definition signals (BM/IO#, BD/C#, BW/R#) so that it becomes available with BADS# in BT1 or the first BT2P. MISS# is floated when the 82385SX does not own the bus, such that multiple 82385SX's can share the same node in multi-cache systems. (As discussed in Chapter 7, this signal also serves a reserved function in testing the 82385SX.)

3.6.2 WRITE BUFFER STATUS (WBS)

The latching data transceiver is also known as the "posted write buffer". WBS indicates that this buffer contains data that has not yet been written to the system even though the 386 SX may have begun its next cycle. It is activated when 386 SX data is latched, and deactivated when the corresponding 82385SX local bus write cycle is completed (BREADY#). (As discussed in Chapter 7, this signal also serves a reserved function in testing the 82385SX.)

WBS can serve several functions. In multi-processor applications, it can act as a coherency mechanism by informing a bus arbiter that it should let a write cycle run on the system bus so that main memory has the latest data. If any other 82385SX cache subsystems are on the bus, they will monitor the cycle via their bus watching mechanisms. Any 82385SX that detects a snoop hit will invalidate the corresponding entry in its local cache.

3.6.3 CACHE FLUSH (FLUSH)

When activated, this signal causes the 82385SX to clear all of its directory tag valid bits, effectively flushing the cache. (As discussed in Chapter 7, this signal also serves a reserved function in testing the 82385SX.) The primary use of the FLUSH input is for diagnostics and multi-processor support. The use of this pin as a coherency mechanism may impact software transparency.

The FLUSH input must be held active for at least 4 CLK (8 CLK2) cycles to complete the flush sequence. If FLUSH is still active after 4 CLK cycles, any accesses to the cache will be misses and the cache will not be updated (since FLUSH is active).

3.7 Bus Arbitration Signals (BHOLD and BHLDA)

In master mode, BHOLD is an input that indicates a request by a slave device for bus ownership. The 82385SX acknowledges this request via its BHLDA output. (These signals function identically to the 386 SX HOLD and HLDA signals.)

The roles of BHOLD and BHLDA are reversed for an 82385SX in slave mode. BHOLD is now an output indicating a request for bus ownership, and BHLDA an input indicating that the request has been granted.

3.8 Coherency (Bus Watching) Support Signals (SA1–SA23, SSTB#, SEN)

These signals form the 82385SX's bus watching interface. The Snoop Address Bus (SA1–SA23) connects to the system address lines if masters reside at both the system and 82385SX local bus levels, or the 82385SX local bus address lines if masters reside only at the 82385SX local bus level. Snoop Strobe (SSTB#) indicates that a valid address is on the snoop address inputs. Snoop Enable (SEN) indicates that the cycle is a write. In a system with masters only at the 82385SX local bus level, SA1–SA23, SSTB#, and SEN can be driven respectively by BA1–BA23, BADS#, and BW/R# without any support circuitry.

3.9 Configuration Inputs (2W/D#, M/S#, DEFOE#)

These signals select the configurations supported by the 82385SX. They are hardware strap options and must not be changed dynamically. 2W/D# (2-Way/Direct Mapped Select) selects a two-way set associative cache when tied high, or a direct mapped cache when tied low. M/S# (Master/Slave Select) chooses between master mode (M/S# high) and slave mode (M/S# low). DEFOE# defines the functionality of the 82385SX cache output enables (COEA# and COEB#). DEFOE# allows the 82385SX to interface to SRAMs with output enables (DEFOE# low) or to SRAMs requiring transceivers (DEFOE# high).

3.10 Reserved Pins (RES)

Some pins on the 82385SX are reserved for internal testing and future cache features. To assure compatibility and functionality, these reserved pins must be configured as shown in Table 3.10.1.

Table 3.10.1. Reserved Pin Connections

PGA Pin Location	PQFP Pin Location	Logic Level
A12	1	High
A13	131	High
B10	7	High
B11	3	High
B12	132	High
C10	4	High
C11	2	High
G13	117	High
H12	110	High
J3	60	High
J14	109	High
K1	58	High
K2	59	High
K3	62	High
L1	61	High
L2	63	High
L3	64	High
L12	100	No Connect
L14	102	High
M13	101	No Connect
N6	75	No Connect
P5	76	No Connect

4.0 386 SX LOCAL BUS INTERFACE

The following is a detailed description of how the 82385SX interfaces to the 386 SX and to 386 SX local bus resources. Items specifically addressed are the interfaces to the 386 SX, the cache SRAMs, and the 387 SX Math Coprocessor.

The many timing diagrams in this and the next chapter provide insight into the dual pipelined bus structure of a 386 SX CPU/82385SX system. It's important to realize, however, that one need not know every possible cycle combination to use the 82385SX. The interface is simple, and the dual bus operation invisible to the 386 SX and system. To facilitate discussion of the timing diagrams, several conventions have been adopted. Refer to Figure 4-2A, and note that 386 SX bus cycles, 386 SX bus states, and 82385SX bus states are identified along the top. All states can be identified by the "frame numbers" along the bottom. The cycles in Figure 4-2A include a cache read hit (CRDH), a cache read miss (CRDM), and a write (WT). WT represents any write, cacheable or not. When necessary to distinguish cacheable writes, a write hit goes by CWTH and a write miss by CWTM. Non-cacheable system reads go by SBRD. Also, it is assumed that system bus pipelining occurs even though the BNA# signal is not shown. When the system pipeline begins is a function of the system bus controller.

386 SX bus cycles can be tracked by ADS# and READYI#, and 82385SX cycles by BADS# and BREADY#. These four signals are thus a natural choice to help track parallel bus activity. Note in the timing diagrams that 386 SX cycles are numbered using ADS# and READYI#, and 82385SX cycles using BADS# and BREADY#. For example, when the address of the first 386 SX cycle becomes available, the corresponding assertion of ADS# is marked "1", and the READYI# pulse that terminates the cycle is marked "1" as well. Whenever a 386 SX cycle is forwarded to the system, its number is forwarded as well so that the corresponding 82385SX bus cycle can be tracked by BADS# and BREADY#.

The "N" value in the timing diagrams is the assumed number of main memory wait states inserted in a non-pipelined 82385SX bus cycle. For example, a non-pipelined access to N = 2 memory requires a total of four bus states, while a pipelined access requires three. (The pipeline advantage effectively hides one main memory wait state.)

4.1 Processor Interface

This section presents the 386 SX CPU/82385SX hardware interface and discusses the interaction and timing of this interface. Also addressed is how to decode the 386 SX address bus to generate the 82385SX inputs LBA# and NCA#. (Recall that LBA# allows memory and/or I/O space to be set aside for 386 SX local bus resources; and NCA# allows system memory to be set aside as non-cacheable.)

4.1.1 HARDWARE INTERFACE

Figure 4-1 is a diagram of a 386 SX CPU/82385SX system, which can be thought of as three distinct interfaces. The first is the 386 SX CPU/82385SX interface (including the Ready Logic). The second is the cache interface, as depicted by the cache control bus in the upper left corner of Figure 4-1. The third is the 82385SX bus interface, which includes both direct connects and signals that control the 74374 address/cycle definition latch and 74646 latching data transceiver. (The 82385SX bus interface is the subject of the next chapter.)

As seen in Figure 4-1, the 386 SX CPU/82385SX interface is a straightforward connection. The only necessary support logic is that required to sum all ready sources.

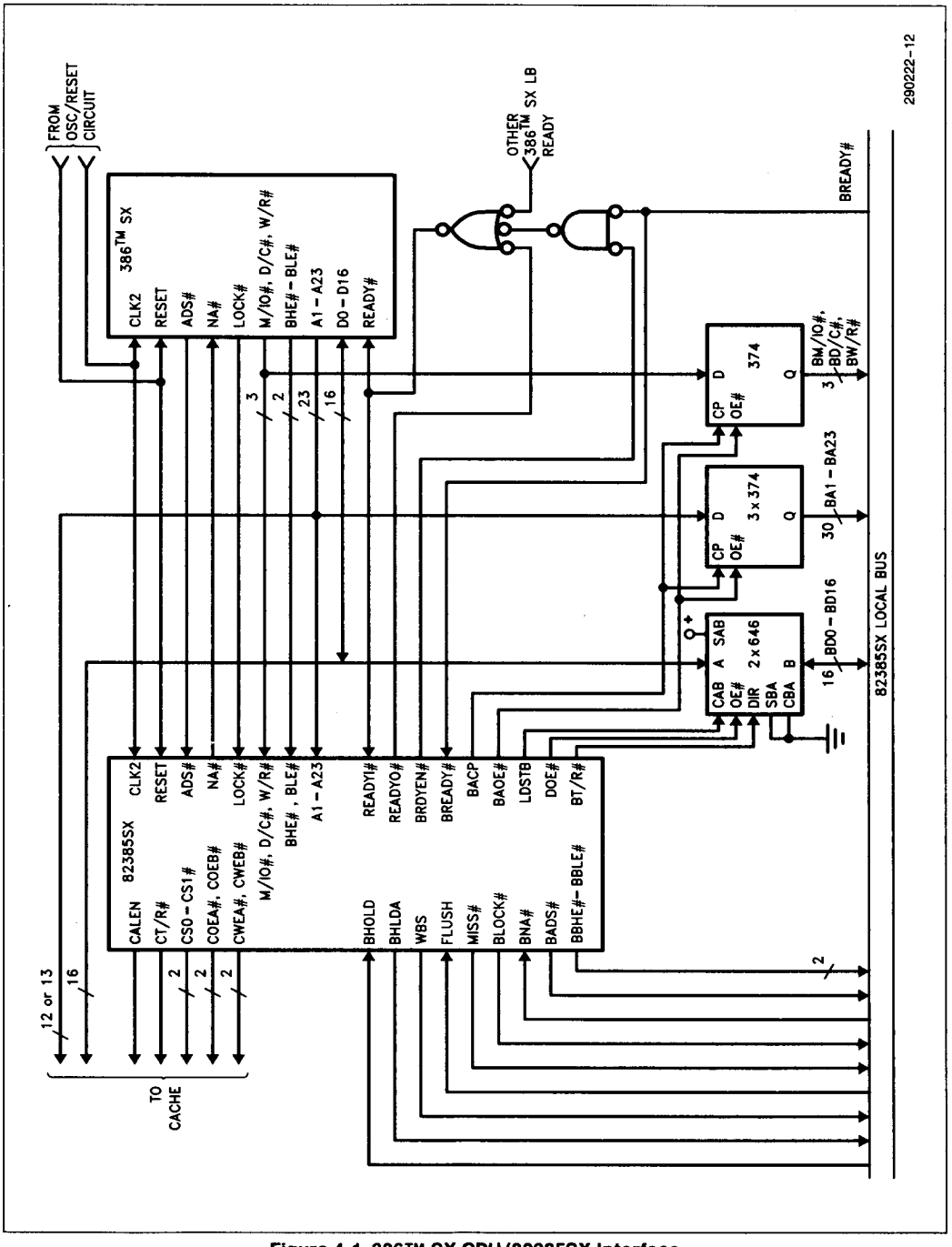


Figure 4-1. 386™ SX CPU/82385SX Interface

5

4.1.2 READY GENERATION

Note in Figure 4-1 that the ready logic consists of two gates. The upper three-input AND gate (shown as a negative logic OR) sums all 386 SX local bus ready sources. One such source is the 82385SX READYO# output, which terminates read hits and posted writes. The output of this gate drives the 386 SX READY# input and is monitored by the 82385SX (via READYI#) to track the 386 SX bus state.

When the 82385SX forwards a 386 SX read cycle to the 82385SX bus (cache read miss or non-cacheable read), it does not directly terminate the cycle via READYO#. Instead, the 386 SX and 82385SX bus cycles are concurrently terminated by a system ready source. This is the purpose of the additional two-input OR gate (negative logic AND) in Figure 4-1. When the 82385SX forwards a read to the 82385SX bus, it asserts BRDYEN# which enables the system ready signal (BREADY#) to directly terminate the 386 SX bus cycle.

Figure 4-2A and 4-2B illustrate the behavior of the signals involved in ready generation. Note in cycle 1 of Figure 4-2A that the 82385SX READYO# directly terminates the hit cycle. In cycle 2, READYO# is not activated. Instead the 82385SX BRDYEN# is activated in BT2, BT2P, or BT2I states such that BREADY# can concurrently terminate the 386 SX and 82385SX bus cycles (frame 6). Cycle 3 is a posted write. The write data becomes available in T1P (frame 7), and the address, data, and cycle definition of the write are latched in T2 (frame 8). The 386 SX cycle is terminated by READYO# in frame 8 with no wait states. The 82385SX, however, sees the write cycle through to completion on the 82385SX bus where it is terminated in frame 10 by BREADY#. In this case, the BREADY# signal is not gated through to the 386 SX. Refer to Figures 4-2A and 4-2B for clarification.

4.1.3 NA# AND 386 SX LOCAL BUS PIPELINING

Cycle 1 of Figure 4-2A is a typical cache read hit. The 386 SX address becomes available in T1, and the 82385SX uses this address to determine if the referenced data resides in the cache. The cache look-up is completed and the cycle qualified as a hit or miss in T1. If the data resides in the cache, the cache is directed to drive the 386 SX data bus, and the 82385SX drives its READYO# output so the cycle can be terminated at the end of the first T2 with no wait states.

Although cycle 2 starts out like cycle 1, at the end of T1 (frame 3), it is qualified as a miss and forwarded to the 82385SX bus. The 82385SX bus cycle begins one state after the 386 SX bus cycle, implying a one wait state overhead associated with cycle 2 due to the look-up. When the 82385SX encounters the miss, it immediately asserts NA#, which puts the 386 SX into pipelined mode. Once in pipelined mode, the 82385SX is able to qualify a 386 SX cycle using the 386 SX pipelined address and control signals. The result is that the cache look-up state is hidden in all but the first of a contiguous sequence of read misses. This is shown in the first two cycles, both read misses, of Figure 4-2B. The CPU sees the look-up state in the first cycle, but not in the second. In fact, the second miss requires a total of only two states, as not only does 386 SX pipelining hide the look-up state, but system pipelining hides one of the main memory wait states. (System level pipelining via BNA# is discussed in the next chapter.) Several characteristics of the 82385SX's pipelining of the 386 SX are as follows:

— The above discussion applies to all system reads, not just cache read misses.

— The 82385SX provides the fastest possible switch to pipelining, T1-T2-T2P. The exception to this is when a system read follows a posted write. In this case, the sequence is T1-T2-T2-T2P. (Refer to cycle 4 of Figure 4-2A.) The number of T2 states is dependent on the number of main memory wait states.

— Refer to the read hit in Figure 4-2A (cycle 1), and note that NA# is actually asserted before the end of T1, before the hit/miss decision is made. This is of no consequence since even though NA# is sampled active in T2, the activation of READYO# in the same T2 renders NA# a "don't care". NA# is asserted in this manner to meet 386 SX timing requirements and to insure the fastest possible switch to pipelined mode.

— All read hits and the majority of writes can be serviced by the 82385SX with zero wait states in non-pipelined mode, and the 82385SX accordingly attempts to run all such cycles in non-pipelined mode. An exception is seen in the hit cycles (cycles 3 and 4) of Figure 4-2B. The 82385SX does not know soon enough that cycle 3 is a hit, and thus sustains the pipeline. The result is that three sequential hits are required before the 386 SX is totally out of pipelined mode. (The three hits look like T1P-T2P, T1P-T2, T1-T2.) Note that this does not occur if the number of main memory wait states is equal to or greater than two.

As far as the design is concerned, NA# is generally tied directly to the 386 SX NA# input. However, other local NA# sources may be logically "AND"ed with the 82385SX NA# output if desired. It is essential, however, that no device other than the 82385SX drive the 386 SX NA# input unless that device re-

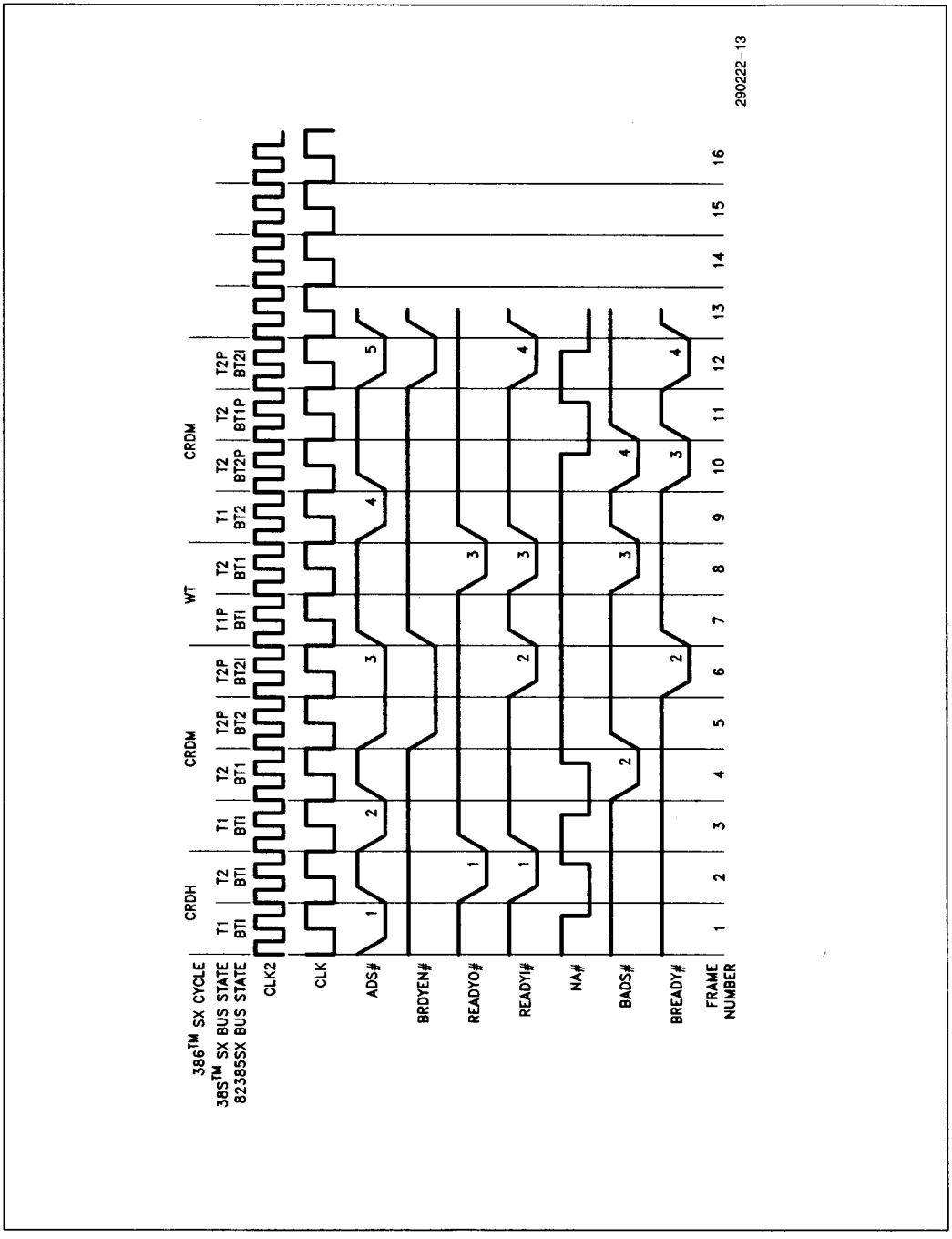


Figure 4-2A. READYO#, BRDYEN#, and NA# (N = 1)

5

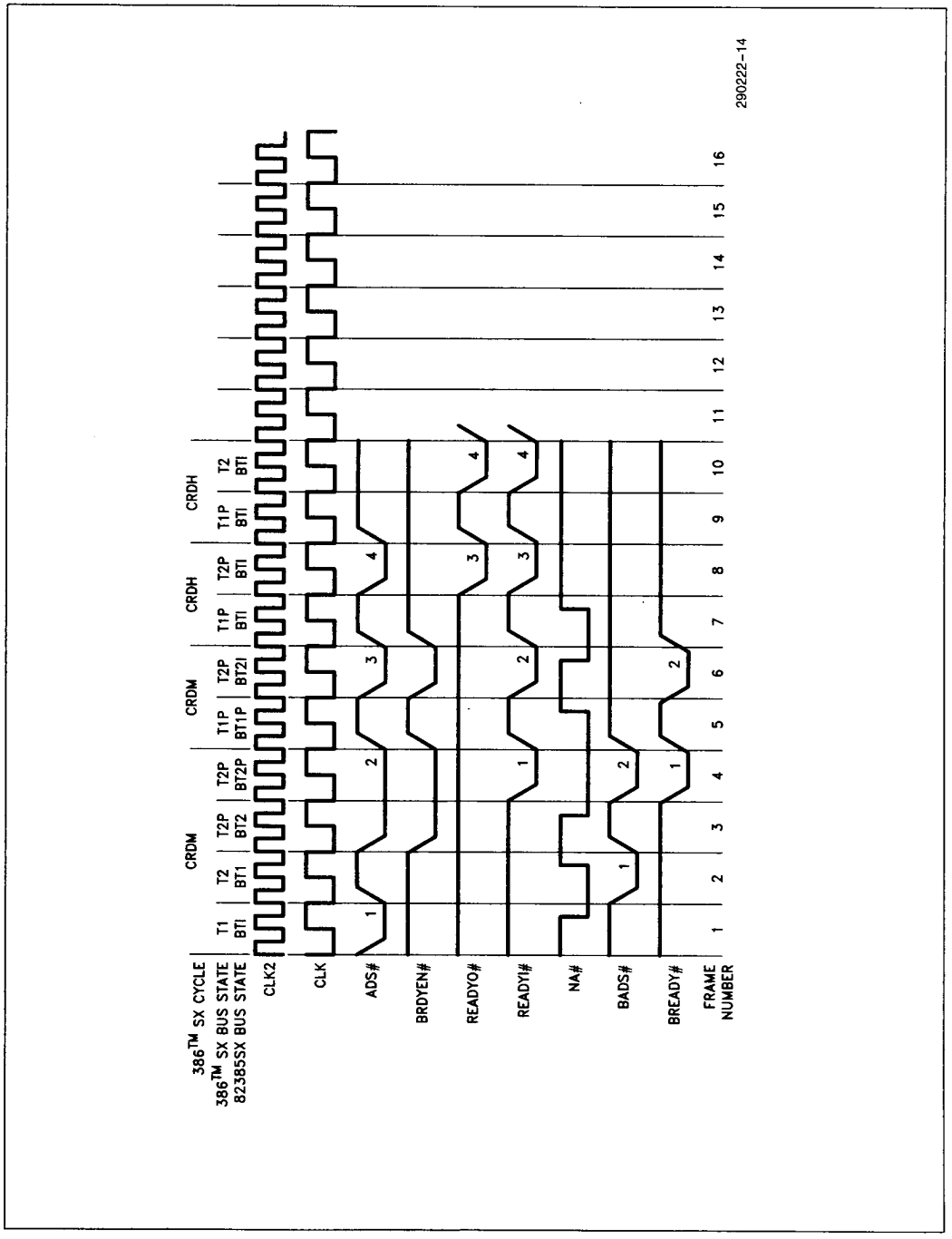


Figure 4-2B. READYO#, BRDYEN#, and NA# (N = 1)

sides on the 386 SX local bus in space decoded via LBA#. If desired, the 82385SX NA# output can be ignored and the 386 SX NA# input tied high. The 386 SX NA# input should never be tied low, which would always keep it active.

4.1.4 LBA# AND NCA# GENERATION

The 82385SX inputs signals LBA# and NCA# are generated by decoding the 386 SX address (A1–A23) and cycle definition (W/R#, D/C#, M/IO#) lines. The 82385SX samples them at the end of the first state in which they become available, which is either T1 or the first T2P cycle. The decode configuration and timings are illustrated respectively in Figures 4-3A and 4-3B.

4.2 Cache Interface

The following is a description of the external data cache and 82385SX cache interface.

4.2.1 CACHE CONFIGURATIONS

The 82385SX controls the cache memory via the control signals shown in Figure 4-1. These signals drive one of four possible cache configurations, as depicted in Figures 4-4A through 4-4D. Figure 4-4A shows a direct mapped cache organized as 8K words. The likely design choice is two 8K x 8 SRAMs. Figure 4-4B depicts the same cache memory but with a data transceiver between the cache and 386 SX data bus. In this configuration, CT/R# controls the transceiver direction, COEA# drives the transceiver output enable (COEB# could also be used), and DEFOE# is strapped high. A data buffer is required if the chosen SRAM does not have a separate output enable. Additionally, buffers may be used to ease SRAM timing requirements or in a system with a heavily loaded data bus. (Guidelines for SRAM selection are included in Chapter 6.)

Figure 4-4C depicts a two-way set associative cache organized as two banks (A and B) of 4K words each. The likely design choice is eight 4K x 4 SRAMs. Finally, Figure 4-4D depicts the two-way organization with data buffers between the cache memory and data bus.

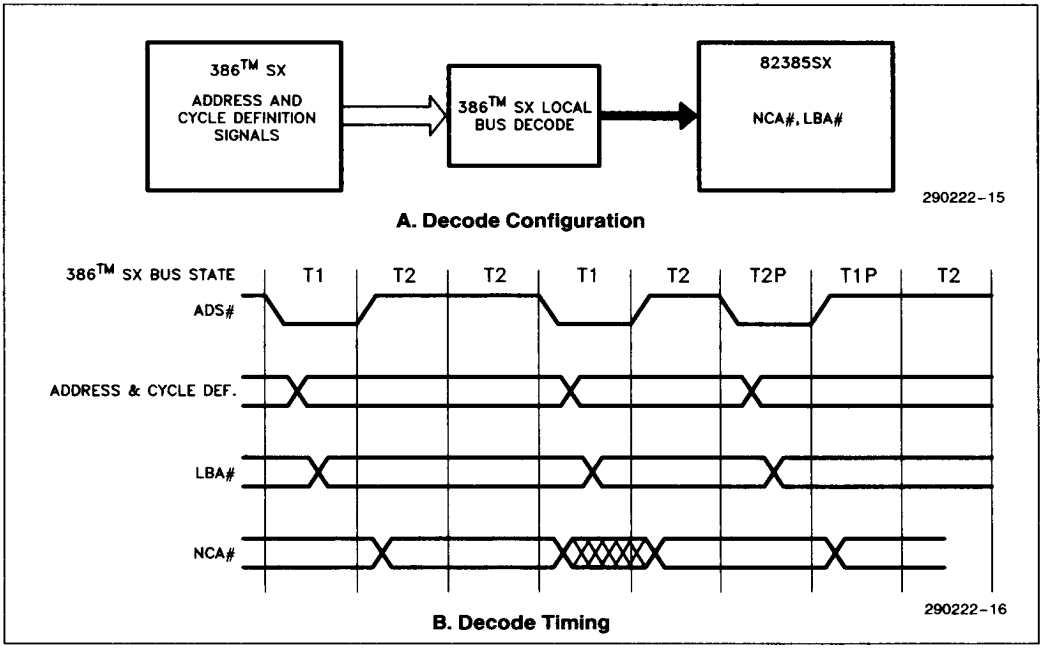


Figure 4-3. NCA#, LBA# Generation

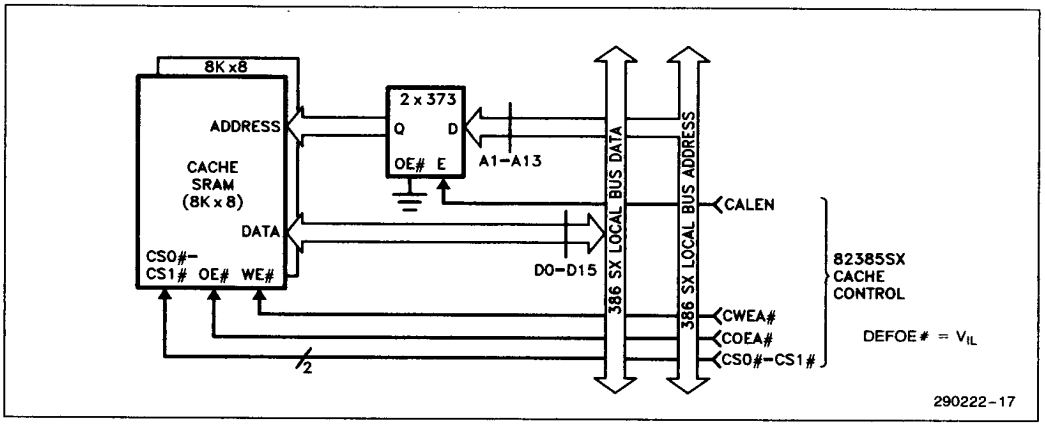


Figure 4-4A. Direct Mapped Cache without Data Buffers

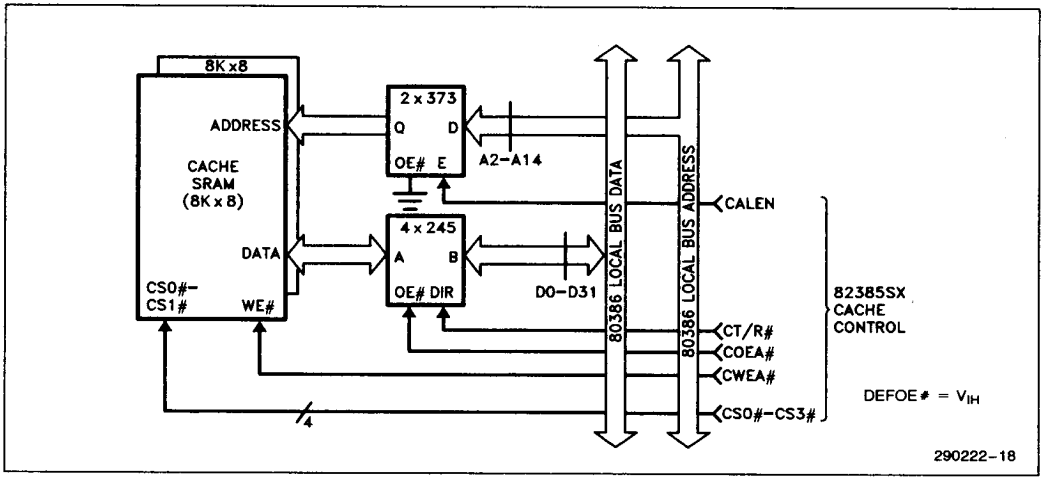


Figure 4-4B. Direct Mapped Cache with Data Buffers

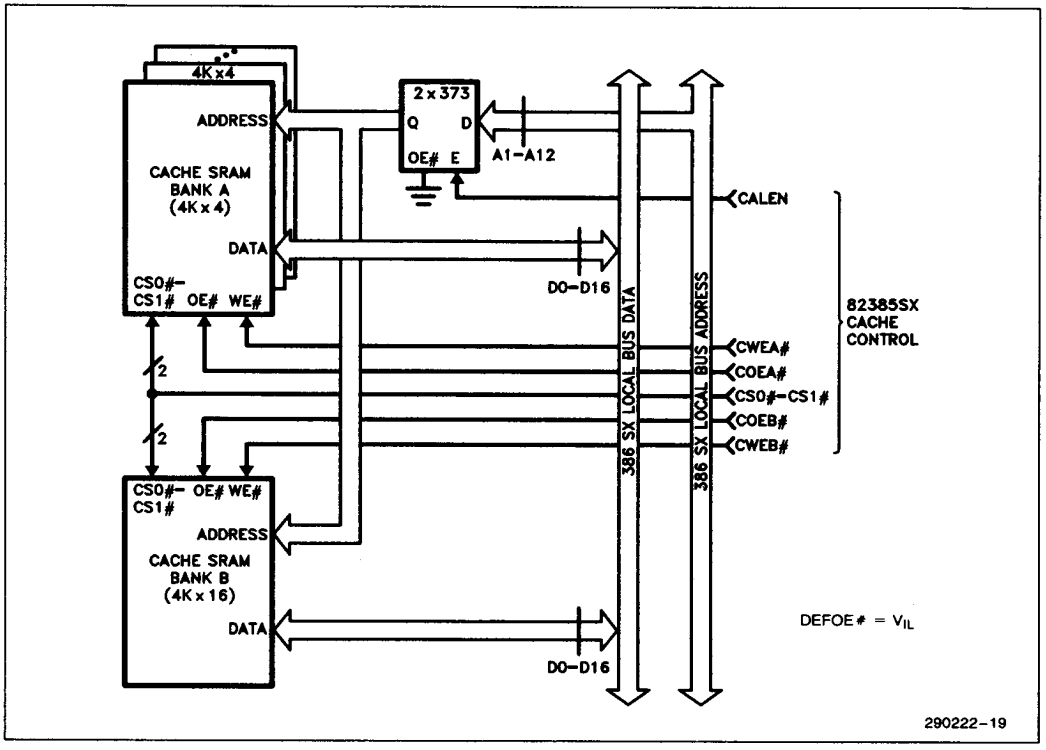


Figure 4-4C. Two-Way Set Associative Cache without Data Buffers

5

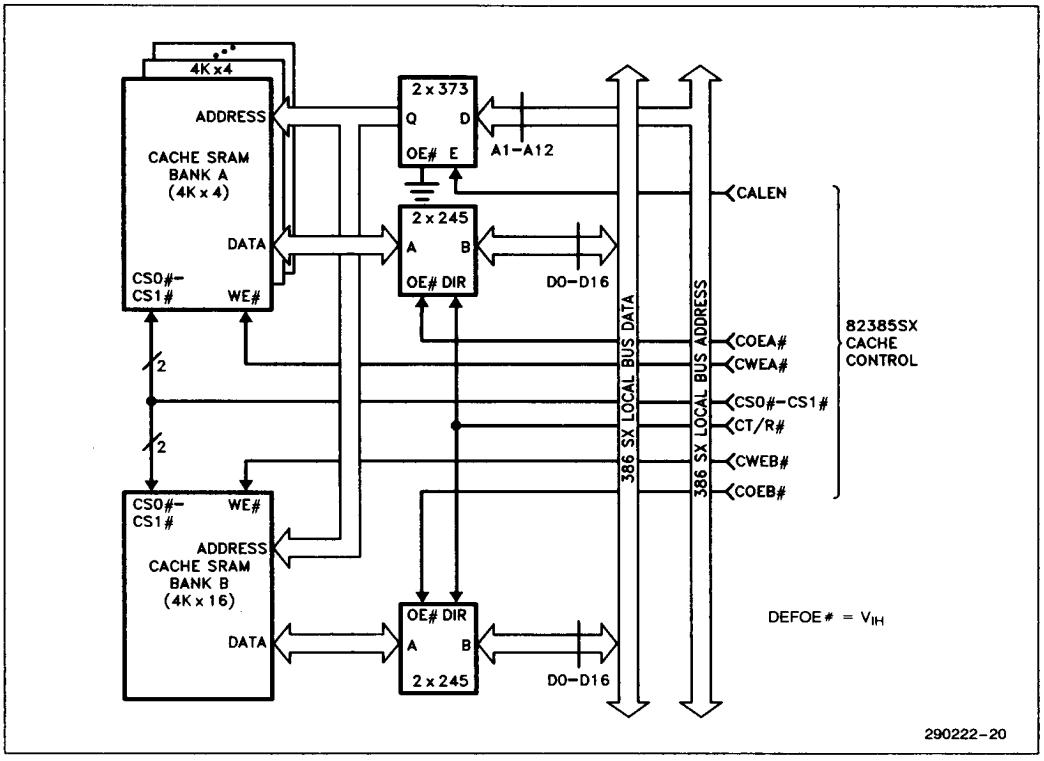
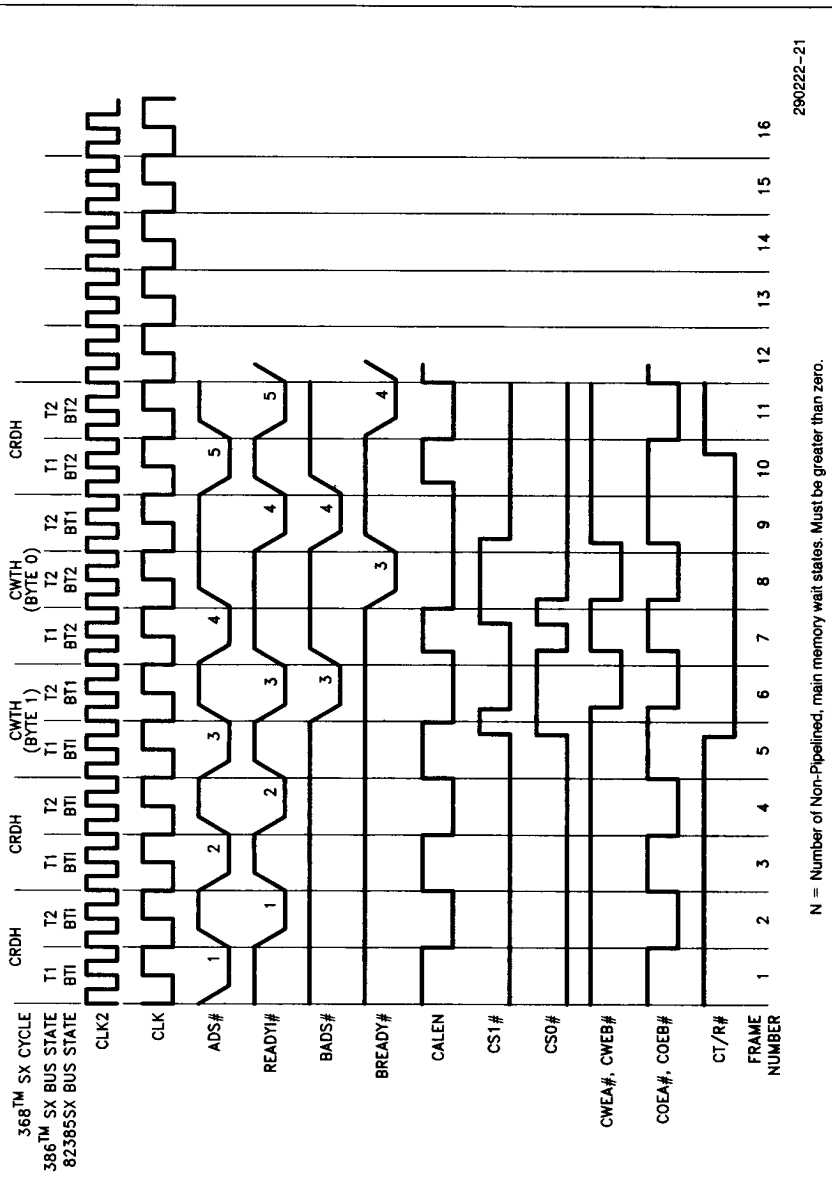


Figure 4-4D. Two-Way Set Associative Cache with Data Buffers

4.2.2 CACHE CONTROL ... DIRECT MAPPED

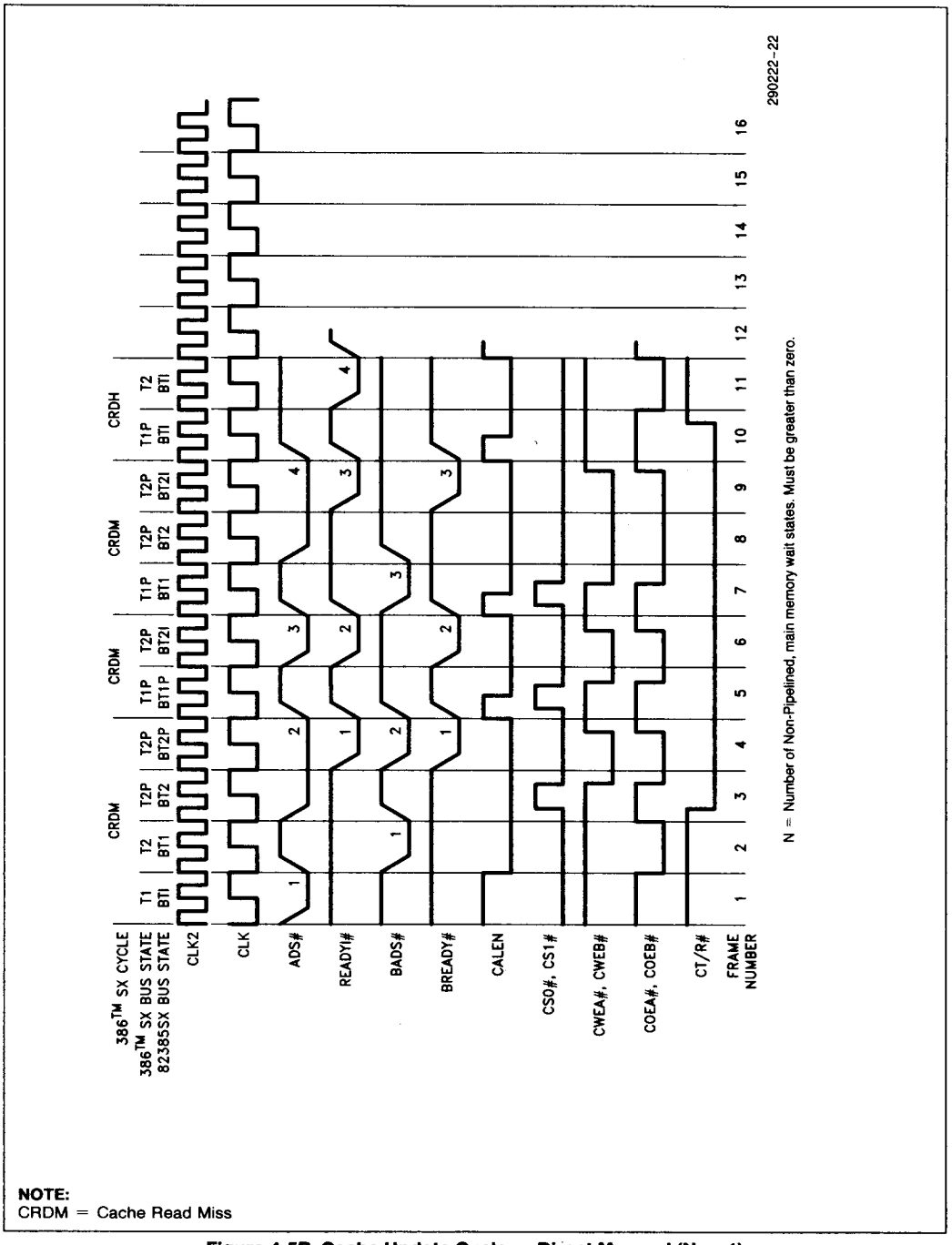
Figure 4-5A illustrates the timing of cache read and write hits, while Figure 4-5B illustrates cache updates. In a read hit, the cache output enables are driven from the beginning of T2 (cycle 1 of Figure 4-5A). If at the end of T1 the cycle is qualified as a cacheable read, the output enables are asserted on the assumption that the cycle will be a hit. (Driving the output enables before the actual hit/miss decision is made eases SRAM timing requirements.)

Cycle 1 of Figure 4-5B illustrates what happens when the assumption of a hit turns out to be wrong. Note that the output enables are asserted at the beginning of of T2, but then disabled at the end of T2. Once the output enables are inactive, the 82385SX turns the transceiver around (via CT/R#) and drives the write enables to begin the cache update cycle. Note in Figure 4-5B that once the 386 SX is in pipelined mode, the output enables need not be driven prior to a hit/miss decision, since the decision is made earlier via the pipelined address information.



NOTES:
CRDH = Cache Read Hit
CWTH = Cache Write Hit

Figure 4-5A. Cache Read and Write Cycles—Direct Mapped (N = 1)



NOTE:
CRDM = Cache Read Miss

Figure 4-5B. Cache Update Cycles—Direct Mapped (N = 1)

One consequence of driving the output enables low in a miss before the hit/miss decision is made is that since the cache starts driving the 386 SX data bus, the 82385SX cannot enable the 74646 transceiver (Figure 4-1) until after the cache outputs are disabled. (The timing of the 74646 control signals is described in the next chapter.) The result is that the 74646 cannot be enabled soon enough to support N = 0 main memory ("N" was defined in Section 4.0 as the number of non-pipelined main memory wait states). This means that memory which can run with zero wait states in a non-pipelined cycle should not be mapped into cacheable memory. This should not present a problem, however, as a main memory system built with N = 0 memory has no need of a cache. (The main memory is as fast as the cache.) Zero wait state memory can be supported if it is decoded as non-cacheable. The 82385SX knows that a cycle is non-cacheable in time not to drive the cache output enables, and can thus enable the 74646 sooner.

In a write hit, the 82385SX only updates the cache bytes that are meant to be updated as directed by the 386 SX byte enables. This prevents corrupting cache data in partial doubleword writes. Note in Figure 4-5A that the appropriate bytes are selected via the cache byte select lines CS0# and CS1#. In a read hit, both select lines are driven as the 386 SX will simply ignore data it does not need. Also, in a cache update (read miss), both selects are active in order to update the cache with a complete line (word).

4.2.3 CACHE CONTROL ... TWO-WAY SET ASSOCIATIVE

Figures 4-6A and 4-6B illustrate the timing of cache read hits, write hits, and updates for a two-way set associative cache. (Note that the cycle sequences are the same as those in Figure 4-5A and 4-5B.) In a cache read hit, only one bank on the other is enabled to drive the 386 SX data bus, so unlike the control of a direct mapped cache, the appropriate cache output enable cannot be driven until the outcome of the hit/miss decision is known. (This implies stricter SRAM timing requirements for a two-way set associative cache.) In write hits and read misses, only one bank or the other is updated.

4.3 387 SX Interface

The 387 SX Math Coprocessor interfaces to the 386 SX just as it would in a system without an 82385SX. The 387 SX READYO# output is logically "AND"ed along with all other 386 SX local bus ready sources (Figure 4-1), and the output is fed to the 387 SX READY#, 82385SX READYI#, and 386 SX READY# inputs.

The 386 SX uniquely addresses the 387 SX by driving M/IO# low and A23 high. The 82385SX decodes this internally and treats 387 SX accesses in the same way it treats 386 SX cycles in which LBA# is asserted, it ignores them.

5.0 82385SX LOCAL BUS AND SYSTEM INTERFACE

The 82385SX system interface is the 82385SX Local Bus, which presents a "386 SX-like" front end to the system. The system ties to it just as it would to a 386 SX. Although this 386 SX-like front end is functionally equivalent to a 386 SX, there are timing differences which can easily be accounted for in a system design.

The following is a description of the 82385SX system interface. After presenting the 82385SX bus state machine, the 82385SX bus signals are described, as are techniques for accommodating any differences between the 82385SX bus and 386 SX bus. Following this is a discussion of the 82385SX's condition upon reset.

5.1 The 82385SX Bus State Machine

5.1.1 MASTER MODE

Figure 5-1A illustrates the 82385SX bus state machine when the 82385SX is programmed in master mode. Note that it is almost identical to the 386 SX bus state machine, only the bus states are 82385SX bus states (BT1P, BTH, etc.) and the state transitions are conditioned by 82385SX bus inputs (BNA# BHOLD, etc.). Whereas a "pending request" to the 386 SX state machine indicates that the 386 SX execution or prefetch unit needs bus access, a pending request to the 82385SX state machine indicates that a 386 SX bus cycle needs to be forwarded to the system (read miss, non-cacheable read, write, etc.). The only difference between the state machines is that the 82385SX does not implement a direct BT1P-BT2P transition. If BNA# is asserted in BT1P, the resulting state sequence is BT1P-BT2I-BT2P. The 82385SX's ability to sustain a pipeline is not affected by the lack of this transition.

5.1.2 SLAVE MODE

The 82385SX's slave mode state machine (Figure 5-1B) is similar to the master mode machine except that now transitions are conditioned by BHLDA rather than BHOLD. (Recall that in slave mode, the roles of BHOLD and BHLDA are reversed from their master mode roles.) Figure 5-2 clarifies slave mode state machine operation. Upon reset, a slave mode

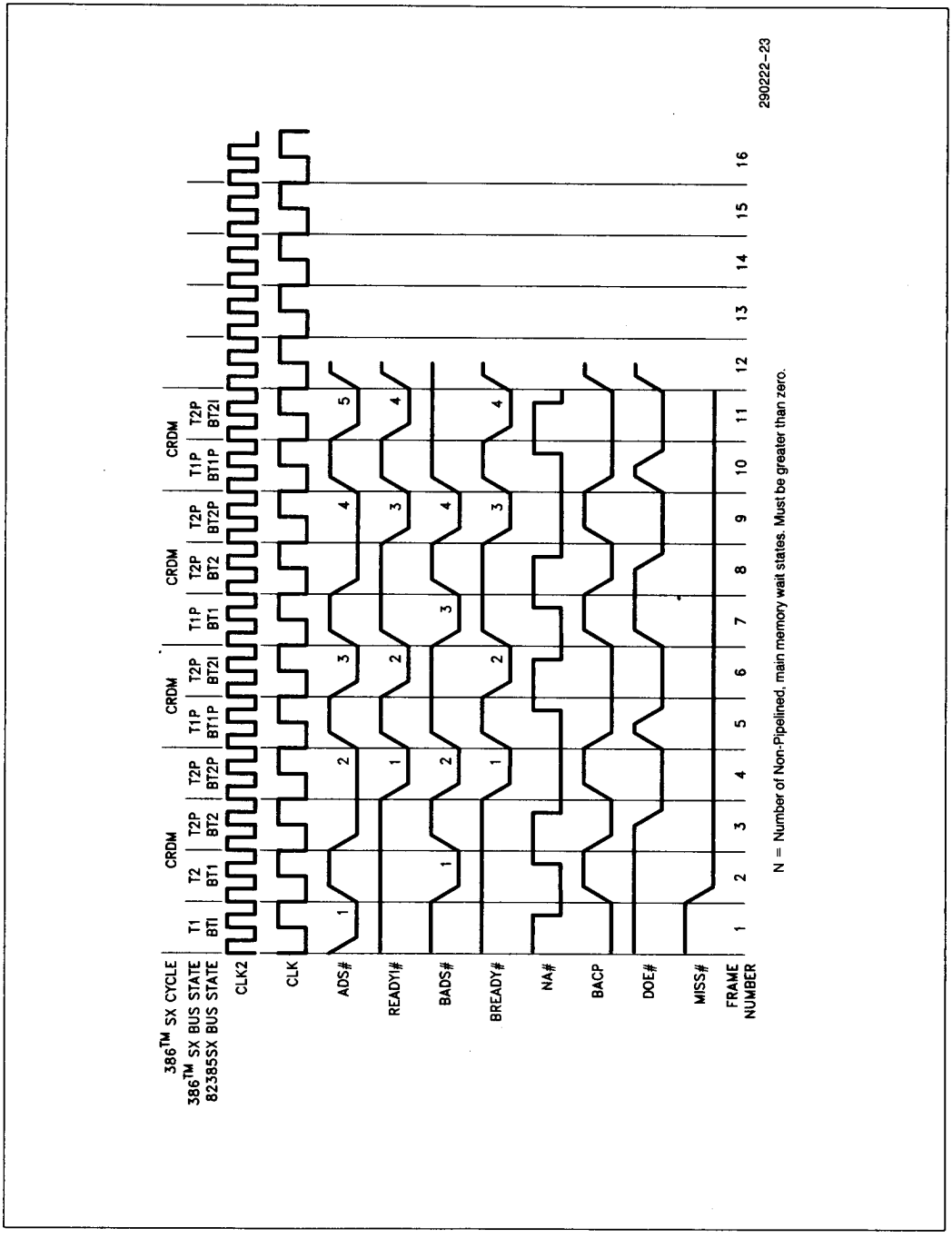


Figure 4-6A. Cache Read and Write Cycles—Two Way Associative (N = 1)

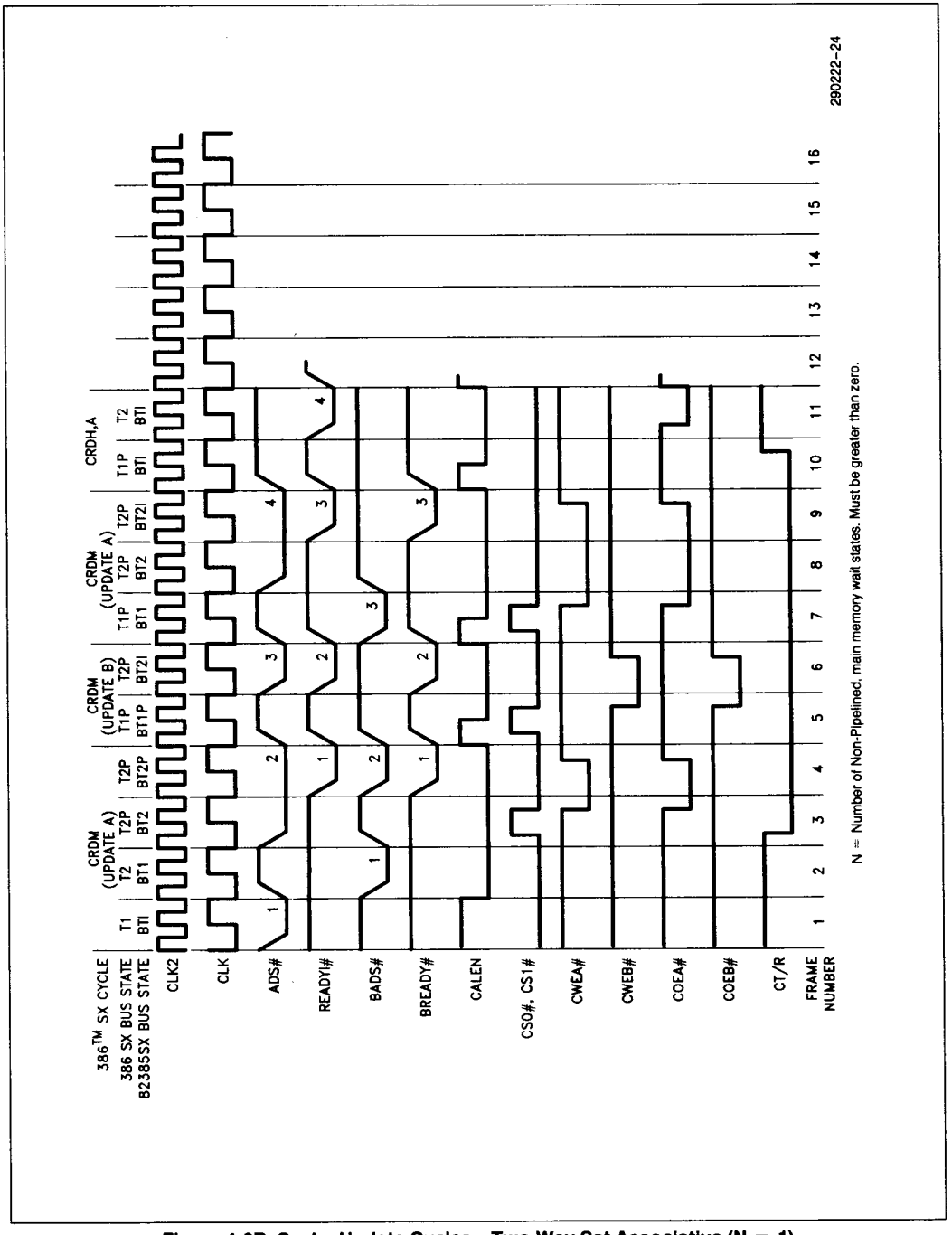


Figure 4-6B. Cache Update Cycles—Two Way Set Associative (N = 1)

82385SX enters the BTH state. When the 386 SX of the slave 82385SX subsystem has a cycle that needs to be forwarded to the system, the 82385SX moves to BTI and issues a hold request via BHOLD. It is important to note that a slave mode 82385SX does not drive the bus in a BTI state. When the master or bus arbiter returns BHLDA, the slave 82385SX enters BT1 and runs the cycle. When the cycle is completed, and if no additional requests are pending, the 82385SX moves back to BTH and disables BHOLD.

If, while a slave 82385SX is running a cycle, the master or arbiter drops BHLDA (Figure 5-2B), the 82385SX will complete the current cycle, move to BTH and remove the BHOLD request. If the 82385SX still had cycles to run when it was kicked off the bus, it will immediately assert a new BHOLD and move to BTI to await bus acknowledgement. Note, however, that it will only move to BTI if BHLDA is negated, insuring that the handshake sequence is completed.

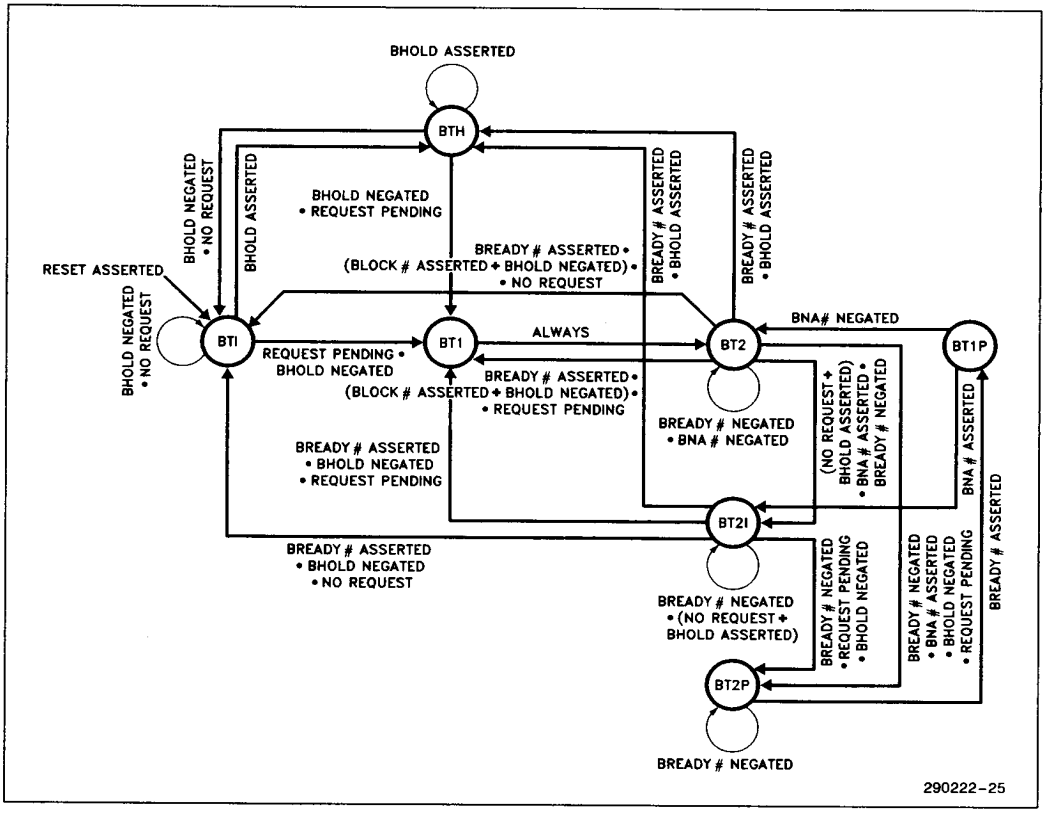


Figure 5-1A. 82385SX Local Bus State Machine—Master Mode

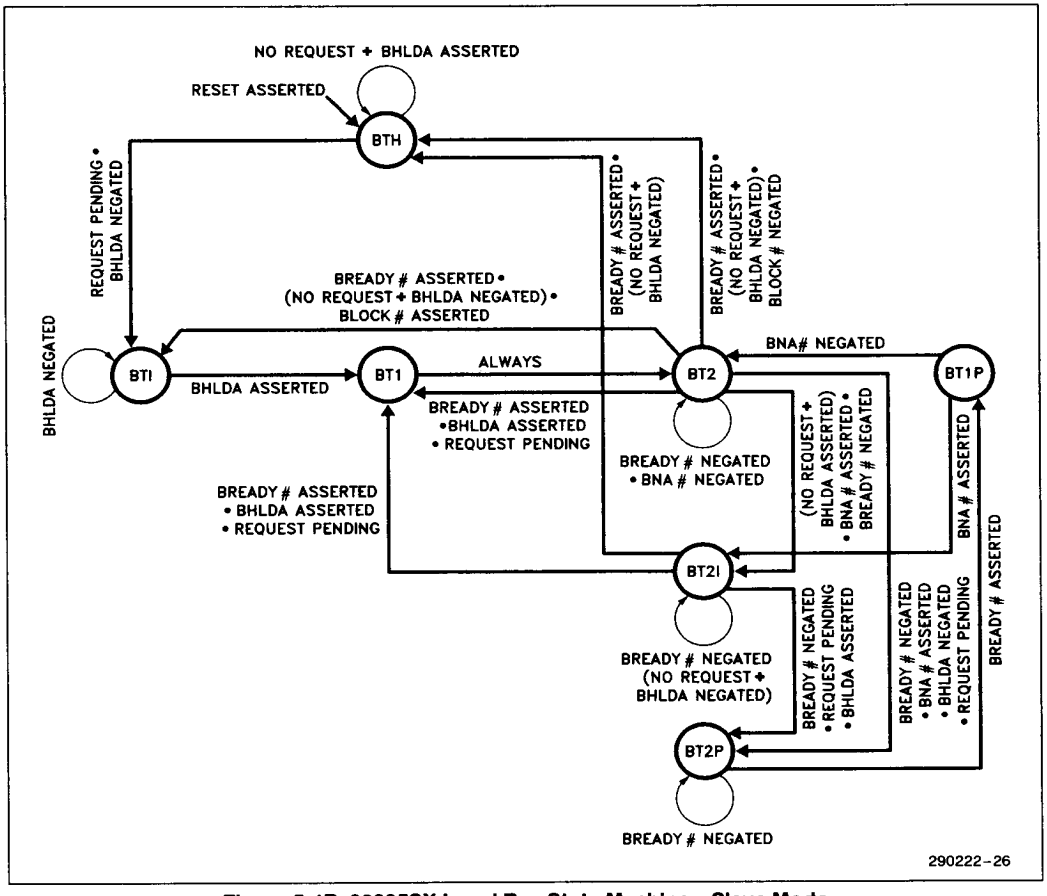


Figure 5-1B. 82385SX Local Bus State Machine—Slave Mode

5

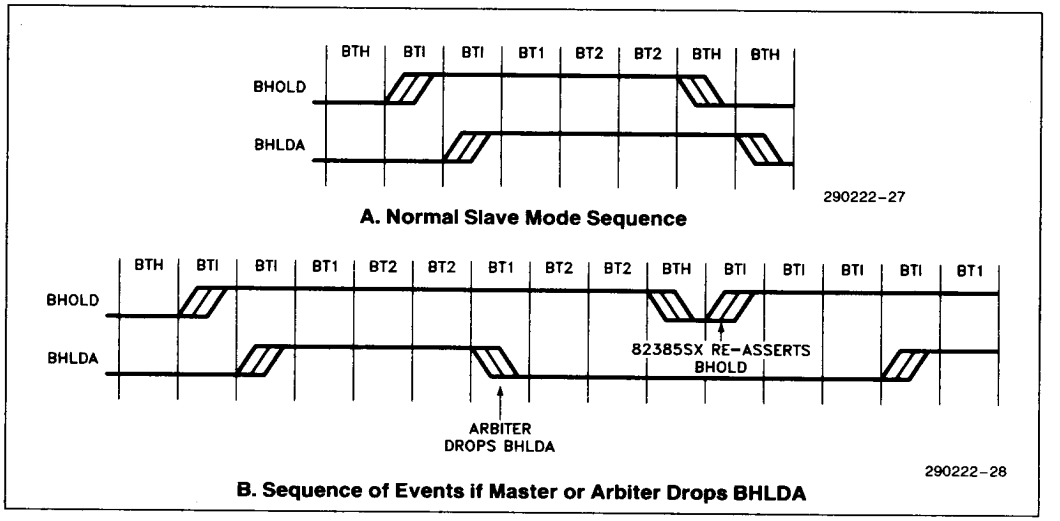


Figure 5-2. BHOLD/BHLDA—Slave Mode

There are several cases in which a slave 82385SX will not immediately release the bus if BHLDA is dropped. For example, if BHLDA is dropped during a BT2P state, the 82385SX has already committed to the next system bus pipelined cycle and will execute it before releasing the bus. Also, the 82385SX will complete a sequence of locked cycles before releasing the bus. This should not present any problems, as a properly designed arbiter will not assume that the 82385SX has released the bus until it sees BHOLD become inactive.

5.2 The 82385SX Local Bus

The 82385SX bus can be broken up into two groups of signals: those which have direct 386 SX counterparts, and additional status and control signals provided by the 82385SX. The operation and interaction of all 82385SX bus signals are depicted in Figures 5-3A through 5-3L for a wide variety of cycle sequences. These diagrams serve as a reference for the 82385SX bus discussion and provide insight into the dual bus operation of the 82385SX.

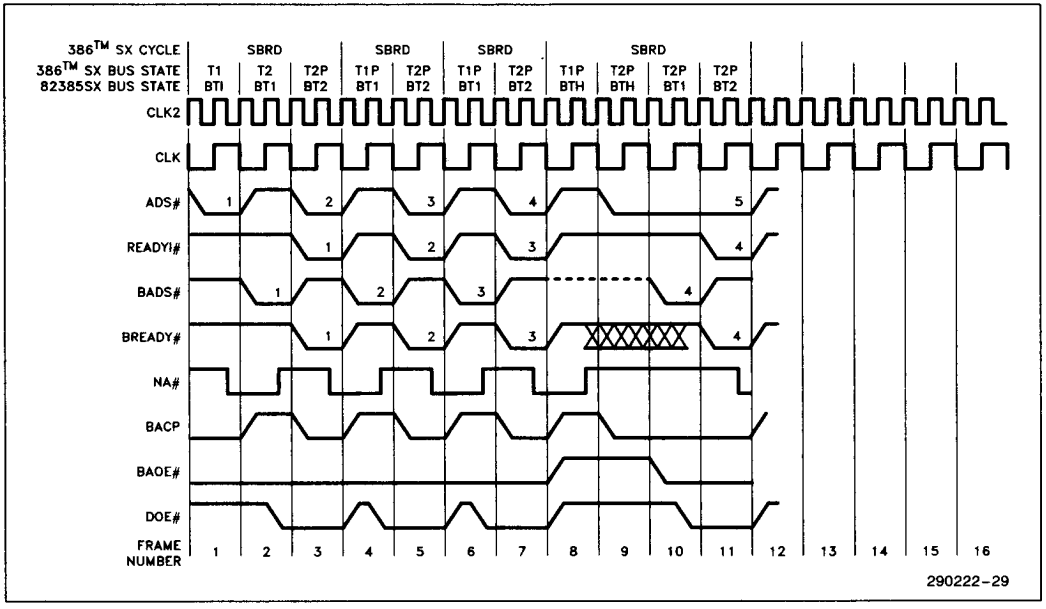


Figure 5-3A. Consecutive SBRD Cycles—(N = 0)

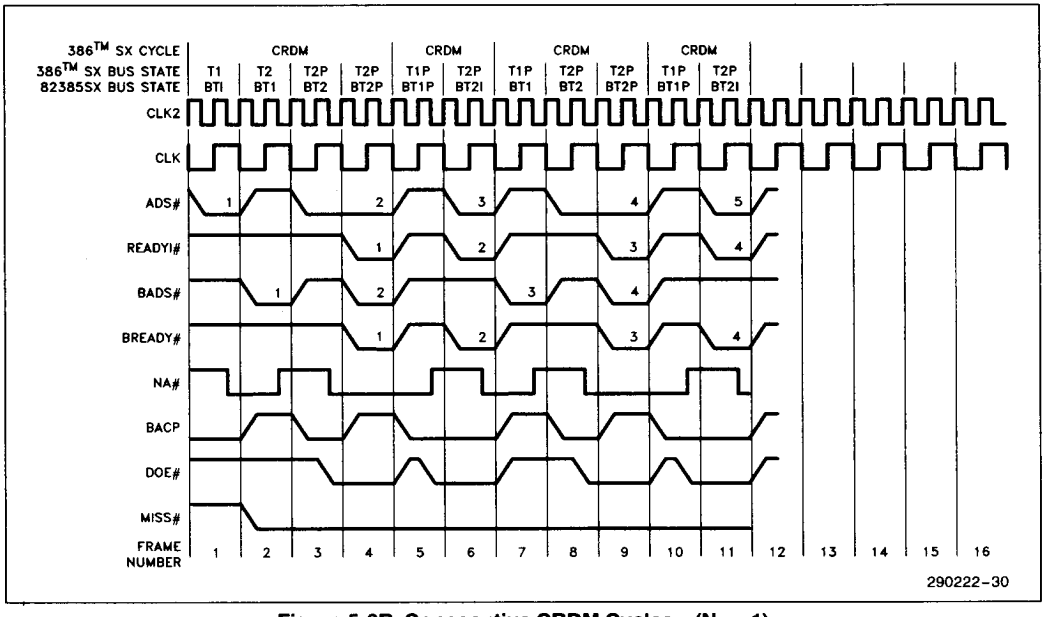


Figure 5-3B. Consecutive CRDM Cycles—(N = 1)

5

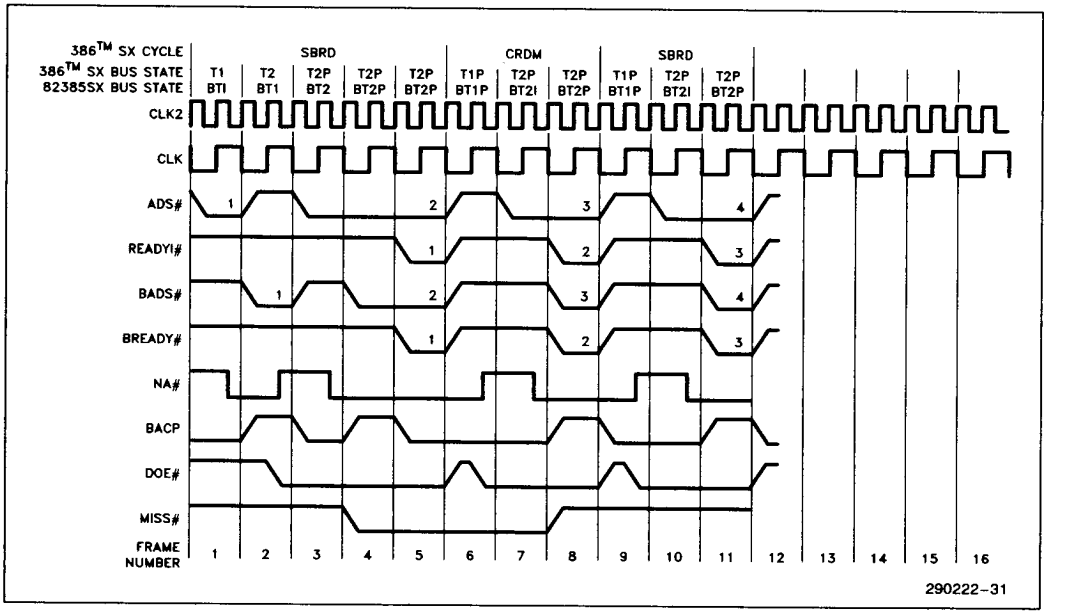


Figure 5-3C. SBRD, CRDM, SBRD—(N = 2)

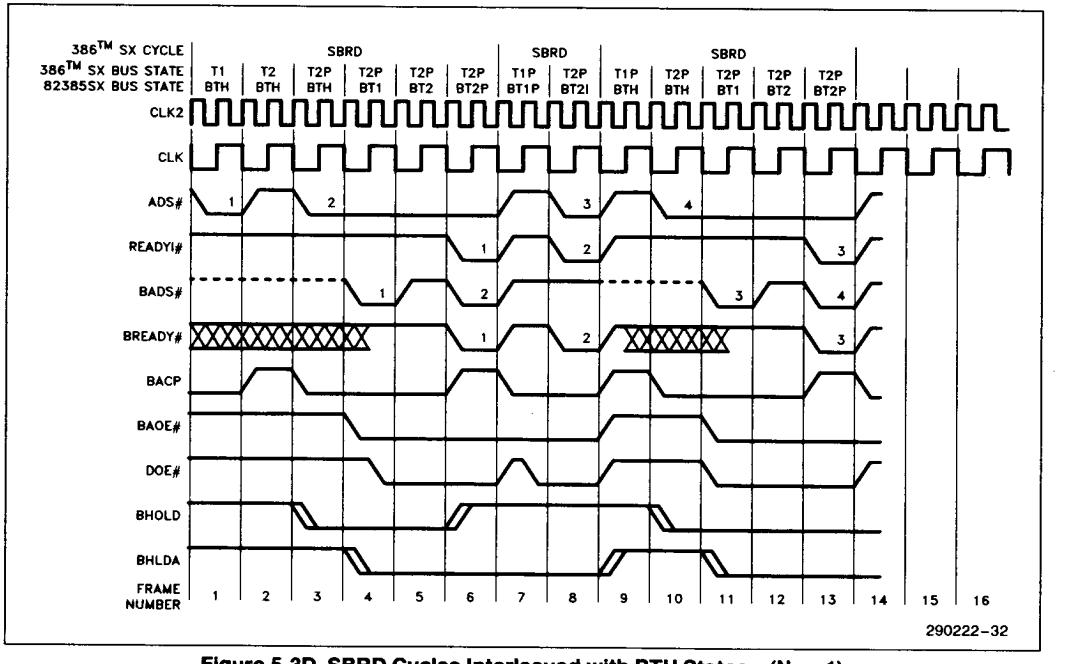


Figure 5-3D. SBRD Cycles Interleaved with BTH States—(N = 1)

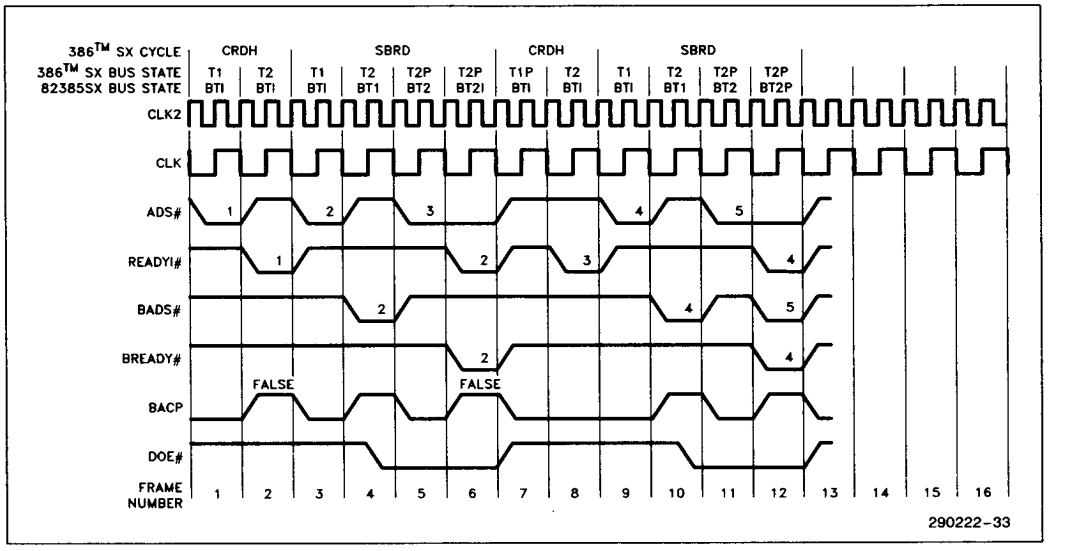


Figure 5-3E. Interleaved SBRD/CDRH Cycles—(N = 1)

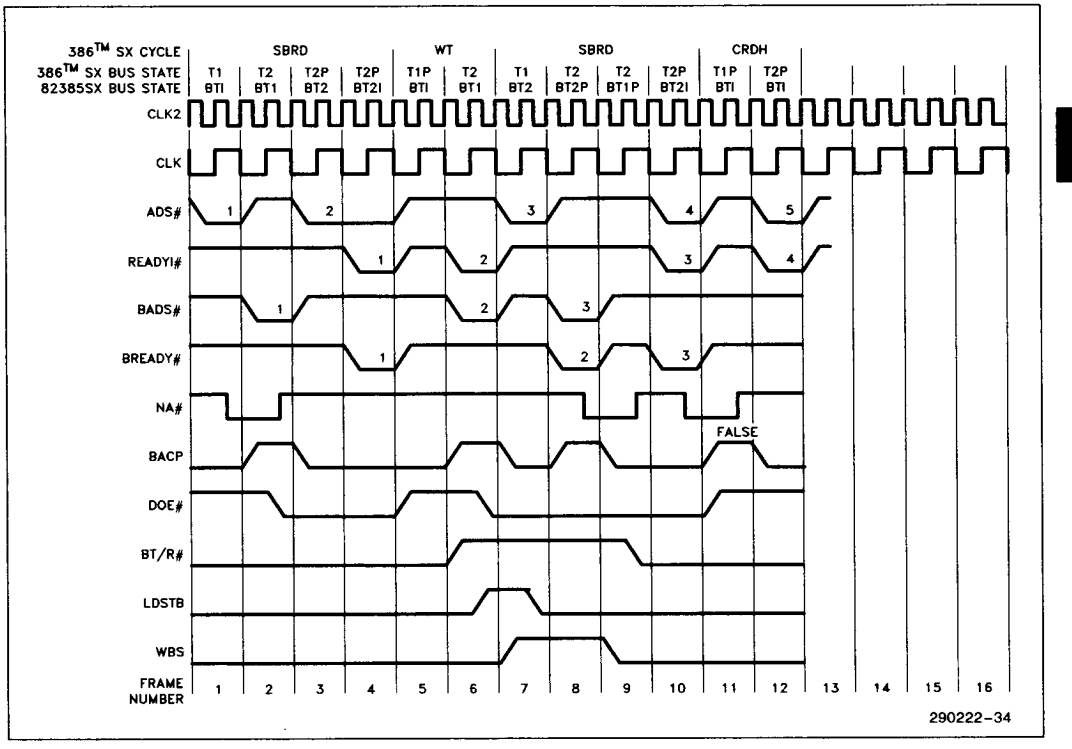


Figure 5-3F. SBRD, WT, SBRD, CRDH—(N = 1)

5

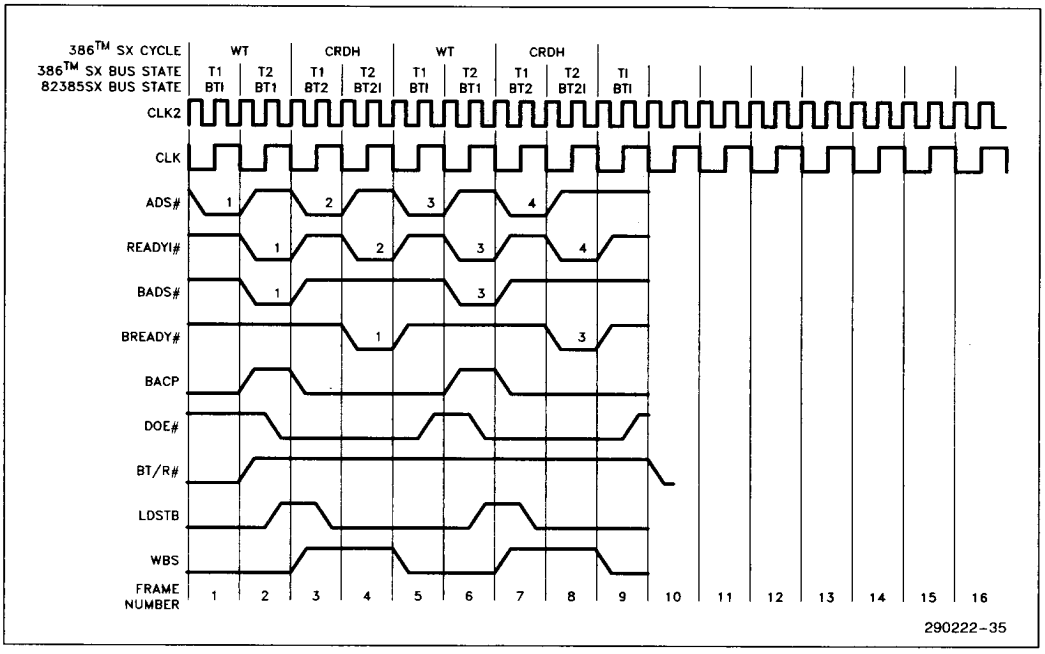


Figure 5-3G. Interleaved WT/CRDH Cycles—(N = 1)

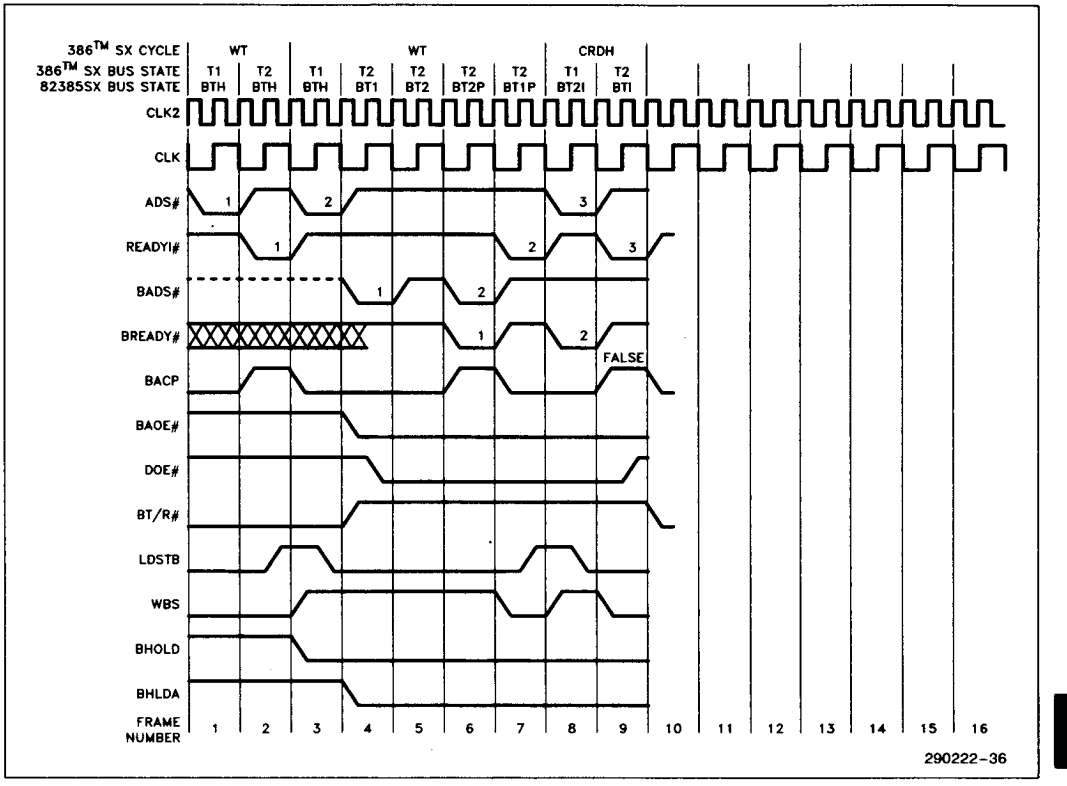


Figure 5-3H. WT, WT, CRDH—(N = 1)

5

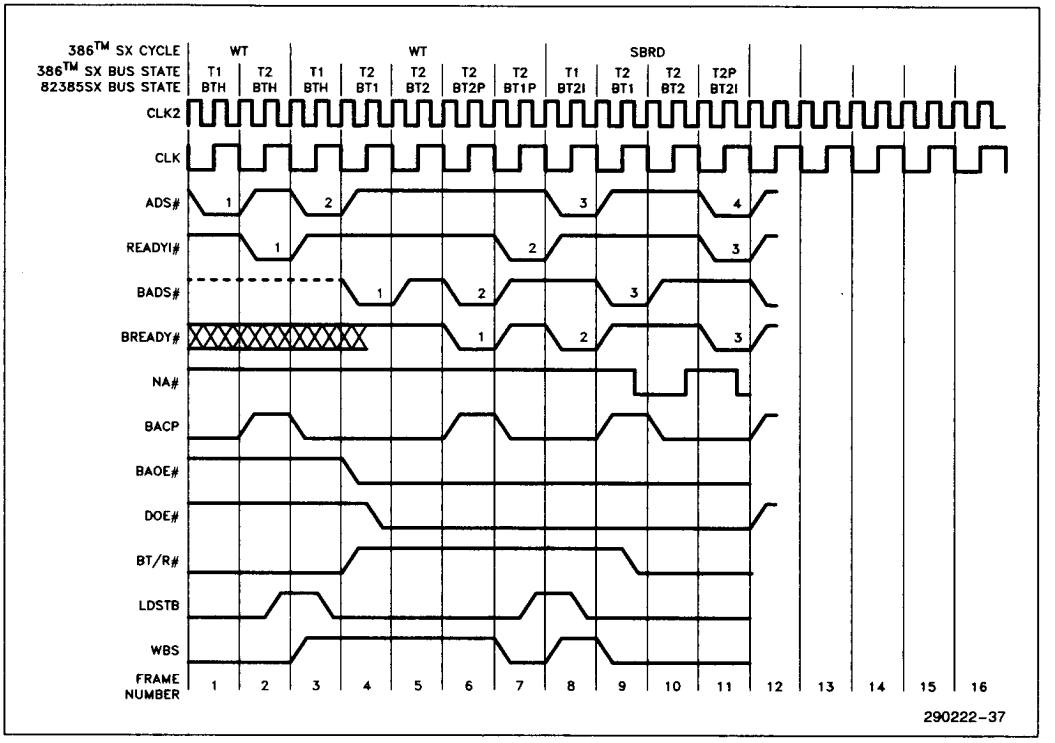


Figure 5-3I. WT, WT, SBRD—(N = 1)

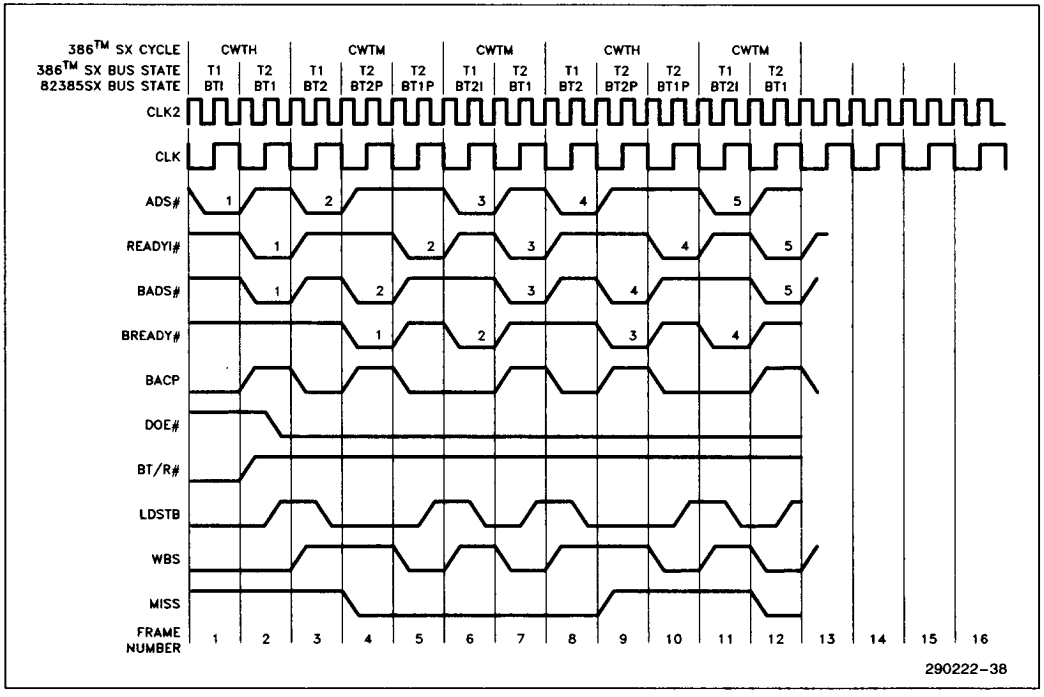


Figure 5-3J. Consecutive Write Cycles—(N = 1)

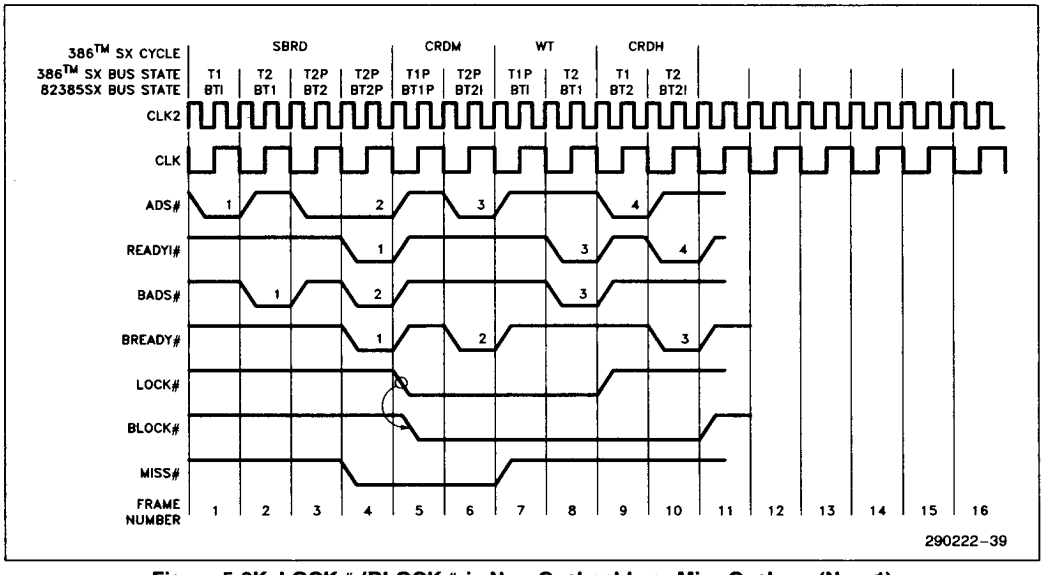


Figure 5-3K. LOCK#/BLOCK# in Non-Cacheable or Miss Cycles—(N = 1)

5

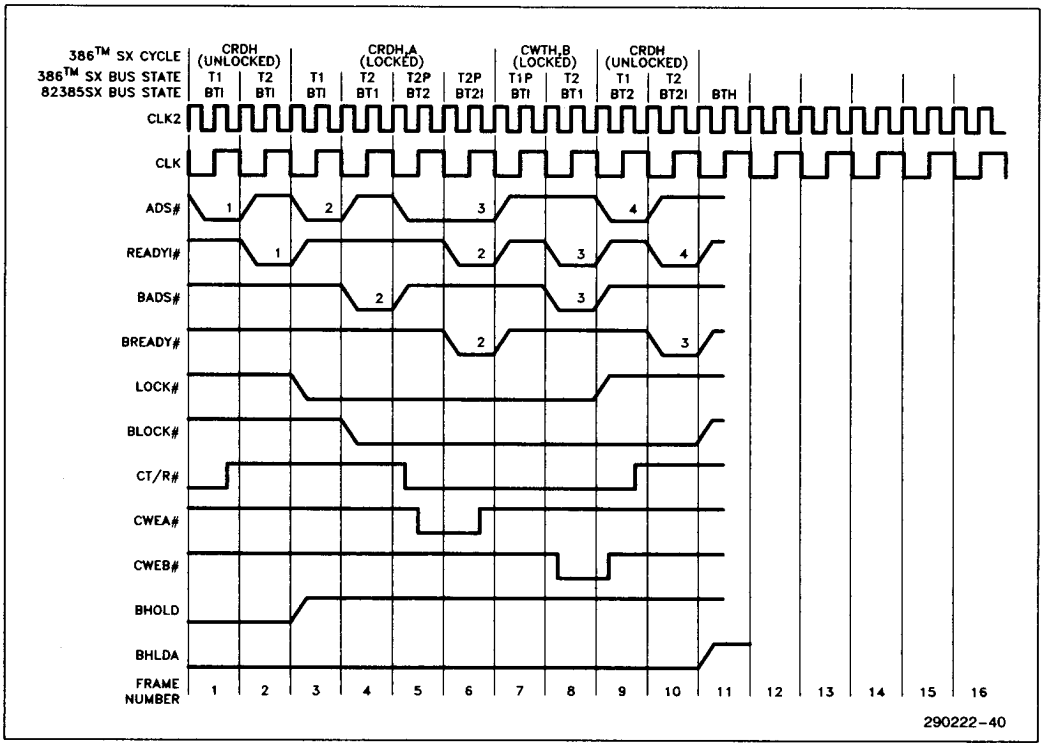


Figure 5-3L. LOCK#/BLOCK# in Cache Read Hit Cycle—(N = 1)

5.2.1 82385SX BUS COUNTERPARTS TO 386™ SX SIGNALS

The following sections discuss the signals presented on the 82385SX local bus which are functional equivalents to the signals present at the 386 SX local bus.

5.2.1.1 Address Bus (BA1–BA23) and Cycle Definition Signals (BM/IO#, BD/C#, BW/R#)

These signals are not driven directly by the 82385SX, but rather are the outputs of the 74374 address/cycle definition latch. (Refer to Figure 4-1 for the hardware interface.) This latch is controlled by the 82385SX BACP and BAOE# outputs. The behavior and timing of these outputs and the latch they control (typically F or AS series TTL) ensure that BA1–BA23, BM/IO#, BW/R#, and BD/C# are compatible in timing and function to their 386 SX counterparts.

The behavior of BACP can be seen in Figure 5-3B, where the rising edge of BACP latches and forwards the 386 SX address and cycle definition signals in a BT1 or first BT2P state. However, the 82385SX need not be the current bus master to latch the 386 SX address, as evidenced by cycle 4 of Figure 5-3A. In this case, the address is latched in frame 8, but not forwarded to the system (via BAOE#) until frame 10. (The latch and output enable functions of the 74374 are independent and invisible to one another.)

Note that in frames 2 and 6 the BACP pulses are marked "False". The reason is that BACP is issued and the address latched before the hit/miss determination is made. This ensures that should the cycle be a miss, the 82385SX bus can move directly into BT1 without delay. In the case of a hit, the latched address is simply never qualified by the assertion of BADS#. The 82385SX bus stays in BTI if there is no access pending (new cycle is a hit) and no bus activity. It will move to and stay in BT2I if the system has requested a pipelined cycle and the 82385SX does not have a pending bus access (new cycle is a hit).

5.2.1.2 Data Bus (BD0–BD15)

The 82385SX data bus is the system side of the 74646 latching transceiver. (See Figure 4-1.) This device is controlled by the 82385SX outputs LDSTB, DOE#, and BT/R#. LDSTB latches data in write cycles, DOE# enables the transceiver outputs, and BT/R# controls the transceiver direction. The interaction of these signals and the transceiver is such that BD0–BD15 behave just like their 386 SX counterparts. The transceiver is configured such that data flow in write cycles (A to B) is latched, and data flow in read cycles (B to A) is flow-through.

Although BD0–BD15 function just like their 386 SX counterparts, there is a timing difference that must be accommodated for in a system design. As mentioned above, the transceiver is transparent during read cycles, so the transceiver propagation delay must be added to the 386 SX data setup. In addition, the cache SRAM setup must be accommodated for in cache read miss cycles.

For non-cacheable reads the data setup is given by:

$$\text{Min BD0–BD15 Read Data Setup} = \text{386 SX Min Data Setup} + \text{74646 B-to-A Max Propagation Delay}$$

The required BD0–BD15 setup in a cache read miss is given by:

$$\text{Min BD0–BD15 Read Data Setup} = \text{74646 B-to-A Max Propagation Delay} + \text{Cache SRAM Min Write Setup} + \text{One CLK2 Period} - \text{82385SX CWEA\# or CWEB\# Min Delay}$$

If a data buffer is located between the 386 SX data bus and the cache SRAMs, then its maximum propagation delay must be added to the above formula as well. A design analysis should be completed for every new design to determine actual margins.

A design can accommodate the increased data setup by choosing appropriately fast main memory DRAMs and data buffers. Alternatively, a designer may deal with the longer setup by inserting an extra wait state into cache read miss cycles. If an additional state is to be inserted, the system bus controller should sample the 82385SX MISS# output to distinquish read misses from cycles that do not require the longer setup. Tips on using the 82385SX MISS# signal are presented later in this chapter.

The behavior of LDSTB, DOE#, and BT/R# can be understood via Figures 5-3A through 5-3L. Note that in cycle 1 of Figure 5-3A (A non-cacheable system read), DOE# is activated midway through BT1, but in cycle 1 of Figure 5-3B (a cache read miss), DOE# is not activated until midway through BT2. The reason is that in a cacheable read cycle, the cache SRAMs are enabled to drive the 386 SX data bus before the outcome of the hit/miss decision (in anticipation of a hit.) In cycle 1 of Figure 5-3B, the assertion of DOE# must be delayed until after the 82385SX has disabled the cache output buffers. The result is that N=0 main memory should not be mapped into the cache.

5.2.1.3 Byte Enables (BBHE#, BBLE#)

These outputs are driven directly by the 82385SX, and are completely compatible in timing and function with their 386 SX counterparts. When a 386 SX cycle is forwarded to the 82385SX bus, the 386 SX byte enables are duplicated on BBHE# and BBLE#. The one exception is a cache read miss, during which BBHE# and BBLE# are both active regardless of the status of the 386 SX byte enables. This ensures that the cache is updated with a valid 16-bit entry.

5.2.1.4 Address Status (BADS#)

BADS# is identical in function and timing to its 386 SX counterpart. It is asserted in BT1 and BT2P states, and indicates that valid address and cycle definition (BA1–BA23, BBHE#, BBLE#, BM/IO#, BW/R#, BD/C#) information is available on the 82385SX bus.

5.2.1.5 Ready (BREADY#)

The 82385SX BREADY# input terminates 82385SX bus cycles just as the 386 SX READY# input terminates 386 SX bus cycles. The behavior of BREADY# is the same as that of READY#, but note in the A.C timing specifications that a cache read miss requires a longer BREADY# setup than do other cycles. This must be accommodated for in ready logic design.

5.2.1.6 Next Address (BNA#)

BNA# is identical in function and timing to its 386 SX counterpart. Note that in Figures 5-3A through 5-3L, BNA# is assumed asserted in every BT1P or first BT2 state. Along with the 82385SX's pipelining of the 386 SX, this ensures that the timing diagrams accurately reflect the full pipelined nature of the dual bus structure.

5.2.1.7 Bus Lock (BLOCK#)

The 386 SX flags a locked sequence of cycles by asserting LOCK#. During a locked sequence, the 386 SX does not acknowledge hold requests, so the

sequence executes without interruption by another master. The 82385SX forces all locked 386 SX cycles to run on the 82385SX bus (unless LBA# is active), regardless of whether or not the referenced location resides in the cache. In addition, a locked sequence of 386 SX cycles is run as a locked sequence on the 82385SX bus; BLOCK# is asserted and the 82385SX does not allow the sequence to be interrupted. Locked writes (hit or miss) and locked read misses affect the cache and cache directory just as their unlocked counterparts do. A locked read hit, however, is handled differently. The read is necessarily forced to run on the 82385SX local bus, and as the data returns from main memory, it is "re-copied" into the cache. (See Figure 5-3L.) The directory is not changed as it already indicates that this location exists in the cache. This activity is invisible to the system and ensures that semaphores are properly handled.

BLOCK# is asserted during locked 82385SX bus cycles just as LOCK# is asserted during locked 386 SX cycles. The BLOCK# maximum valid delay, however, differs from that of LOCK#, and this must be accounted for in any circuitry that makes use of BLOCK#. The difference is due to the fact that LOCK#, unlike the other 386 SX cycle definition signals, is not pipelined. The situation is clarified in Figure 5-3K. In cycle 2 the state of LOCK# is not known before the corresponding system read starts (Frame 4 and 5). In this case, LOCK# is asserted at the beginning of T1P, and the delay for BLOCK# to become active is the delay of LOCK# from the 386 SX plus the propagation delay through the 82385SX. This occurs because T1P and the corresponding BT1P are concurrent (Frame 5). The result is that BLOCK# should not be sampled at the end of BT1P. The first appropriate sampling point is midway through the next state, as shown in Frame 6. In Figure 5-3L, the maximum delay for BLOCK# to become valid in Frame 4 is the same as the maximum delay for LOCK# to become valid from the 386 SX. This is true since the pipelining issue discussed above does not occur.

The 82385 should negate BLOCK# after: BREADY# of the last 82385 Locked Cycle was asserted AND LOCK# turns inactive.

This means that in a sequence of cycles which begins with a 82385 Locked Cycle and goes on with all the possible Locked Cycles (other 82385 cycles, idles, and local cycles), while LOCK# is continuously active, the 82385 will maintain BLOCK# active continuously. Another implication is that in a Locked Posted Write Cycle followed by non-locked sequence, BLOCK# is negated one CLK after BREADY# of the write cycle. In other 82385 Locked Cycles, followed by non-locked sequences, BLOCK# is negated one CLK after LOCK# is negated, which occurs two CLKs after BREADY# is asserted. In the last case BLOCK# active moves by one CLK to the non-locked sequence.

The arbitration rules of Locked Cycles are:

MASTER MODE:

BHOLD input signal is ignored when BLOCK# or internal lock (16-bit non-aligned cycle) are active. BHLDA output signal remains inactive, and BAOE# output signal remains active at that time interval.

SLAVE MODE:

The 82385 does not relinquish the system bus if BLOCK# or internal lock are active. The BHOLD output signal remains active when BLOCK# or internal lock is active plus one CLK. The BHLDA input signal is ignored when BLOCK# or the internal lock is active plus one CLK. This means the 82385 slave does not respond to BHLDA inactivation. The BAOE# output signal remains active during the same time interval.

5.2.2 ADDITIONAL 82385SX BUS SIGNALS

The 82385SX bus provides two status outputs and one control input that are unique to cache operation and thus have no 386 SX counterparts. The outputs are MISS# and WBS, and the input is FLUSH.

5.2.2.1 Cache Read/Write Miss Indication (MISS#)

MISS# can be thought of as an extra 82385SX bus cycle definition signal similar to BM/IO#, BW/R#, and BD/C#, that distinguishes cacheable read and write misses from other cycles. MISS#, like the other definition signals, becomes valid with BADS# (BT1 or first BT2P). The behavior of MISS# is illustrated in Figures 5-3B, 5-3C, and 5-3J. The 82385SX floats MISS# when another master owns the bus, allowing multiple 82385SXs to share the same node in multi-cache systems. MISS# should thus be lightly pulled up (~ 20K) to keep it negated during hold (BTH) states.

MISS# can serve several purposes. As discussed previously, the BD0–BD15 and BREADY# setup times in a cache read miss are longer than in other cycles. A bus controller can distinguish these cycles by gating MISS# with BW/R#. MISS# may also prove useful in gathering 82385SX system performance data.

5.2.2.2 WRITE BUFFER STATUS (WBS)

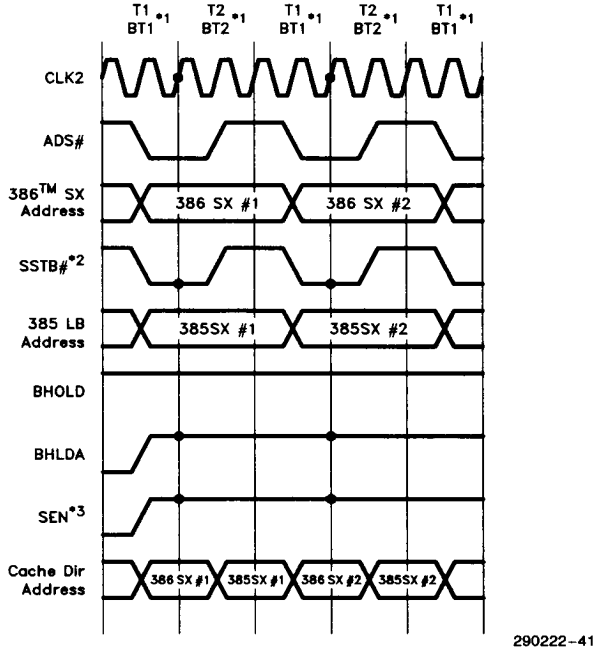
WBS is activated when 386 SX write cycle data is latched into the 74676 latching transceiver (via LDSTB). It is deactivated upon completion of the write cycle on the 82385SX bus when the 82385SX sees the BREADY# signal. WBS behavior is illustrated in Figures 5-3F through 5-3J, and potential applications are discussed in Chapter 3.

5.2.2.3 Cache Flush (FLUSH)

FLUSH is an 82385SX input which is used to reset all tag valid bits within the cache directory. The FLUSH input must be kept active for at least 4 CLK (8 CLK2) periods to complete the directory flush. Flush is generally used in diagnostics but can also be used in applications where snooping cannot guarantee coherency.

5.3 Bus Watching (Snoop) Interface

The 82385SX's bus watching interface consists of the snoop address (SA1–SA23), snoop strobe (SSTB#), and snoop enable (SEN) inputs. If masters reside at the system bus level, then the SA1–SA23 inputs are connected to the system address lines and SEN the system bus memory write command. SSTB# indicates that a valid address is present on the system bus. Note that the snoop bus inputs are synchronous, so care must be taken to ensure that they are stable during their sample windows. If no master resides beyond the 82385 bus level, then the 82385 inputs SA1–SA23, SEN, and SSTB# can respectively tie directly to BA1–BA23, BW/R#, and BADS# of the other system bus master (see Figure 5.5). However, it is recommended that SEN be driven by the logical "AND" of BW/R# and BM/IO# so as to prevent I/O writes from unnecessarily invalidating cache data.



NOTE:
*1. These states are induced by another System Bus master.
*2. SSTB# on the 82385SX is tied directly to BADS# of the System Bus master.
*3. SEN on the 82385SX is tied directly to BW/R# of the System Bus master.

Figure 5.4. Interleaved Snoop and 386™ SX Accesses to the Cache Directory

5

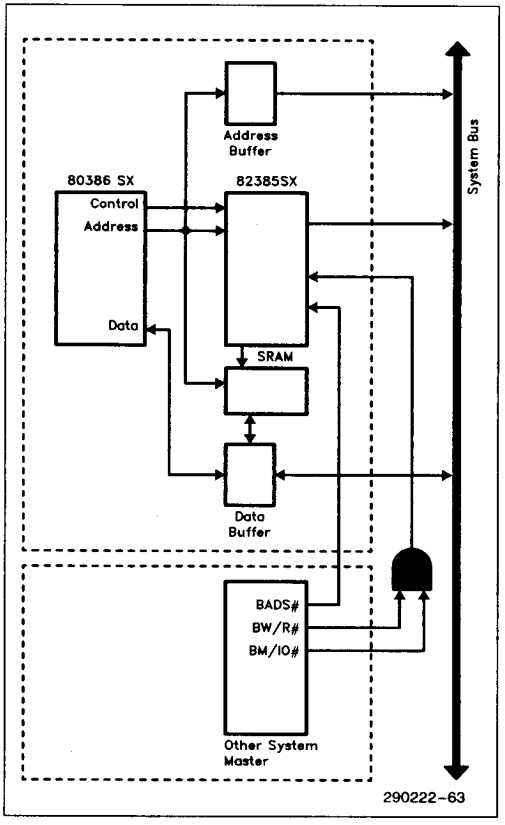


Figure 5.5. Snooping Connections in a Multi Master Environment

When the 82385SX detects a system write by another master and the conditions in Figure 5.4 are met: CLK2 PHI1 rising (CLK falling), BHLDA asserted, SEN asserted, SSTB# asserted, it internally latches SA1–SA23 and runs a cache look-up to see if the altered main memory location is duplicated in the cache. If yes (a snoop hit), the line valid bit associated with that cache entry is cleared. An important feature of the 82385SX is that even the 386 SX is running zero wait state hits out of the cache, all snoops are serviced. This is accomplished by time multiplexing the cache directory between the 386 SX address and the latched system address. If the SSTB# signal occurs during an 82385SX comparison cycle (for the 386 SX), the 386 SX cycle has the highest priority in accessing the cache directory. This takes the first of the two 386 SX states. The other state is then used for the snoop comparison. This worst case example, depicted in Figure 5.4, shows the 386 SX running zero wait state hits on the 386 SX local bus, and another master running zero wait state writes on the 82385SX bus. No snoops are missed, and no performance penalty incurred.

5.4 Reset Definition

Table 5-1 summarizes the states of all 82385SX outputs during reset and initialization. A slave mode 82385SX tri-states its "386 SX-like" front end. A master mode 82385SX emits a pulse stream on its BACP output. As the 386 SX address and cycle definition lines reach their reset values, this stream will latch the reset values through to the 82385SX bus.

Table 5-1. Pin State during RESET and Initialization

Output Name	Signal Level during RESET and Initialization	
	Master Mode	Slave Mode
NA#	High	High
READY0#	High	High
BRDYEN#	High	High
CALEN	High	High
CWEA#–CWEB#	High	High
CS0#, CS1#	Low	Low
CT/R#	High	High
COEA#–COEB#	High	High
BADS#	High	High Z
BBHE#, BBLE#	386 BE#	High Z
BLOCK#	High	High Z
MISS#	High	High Z
BACP	Pulse(1)	Pulse
BAOE#	Low	High
BT/R#	Low	Low
DOE#	High	High
LDSTB	Low	Low
BHOLD	—	Low
BHLDA	Low	—
WBS	Low	Low

NOTE:
1. In Master Mode, BAOE# is low and BACP emits a pulse stream during reset. As the 386 SX address and cycle definition signals reach their reset values, the pulse stream on BACP will latch these values through to the 82385SX local bus.

6.0 82385SX SYSTEM DESIGN CONSIDERATIONS

6.1 Introduction

This chapter discusses techniques which should be implemented in an 82385SX system. Because of the high frequencies and high performance nature of the 386 SX CPU/82385SX system, good design and layout techniques are necessary. It is always recommended to perform a complete design analysis of new system designs.

6.2 Power and Grounding

6.2.1 POWER CONNECTIONS

The 82385SX utilizes 8 power (V_{CC}) and 10 ground (V_{SS}) pins. All V_{CC} and V_{SS} pins must be connected to their appropriate plane. On a printed circuit board, all V_{CC} pins must be connected to the power plane and all V_{SS} pins must be connected to the ground plane.

6.2.2 POWER DECOUPLING

Although the 82385SX itself is generally a "passive" device in that it has a few output signals, the cache subsystem as a whole is quite active. Therefore, many decoupling capacitors should be placed around the 82385SX cache subsystem.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the decoupling capacitors and their respective devices as much as possible. Capacitors specifically for PGA packages are also commercially available, for the lowest possible inductance.

6.2.3 RESISTOR RECOMMENDATIONS

Because of the dual structure of the 82385SX subsystem (386 SX Local Bus and 82385SX Local Bus), any signals which are recommended to be pulled up will be respective to one of the busses. The following sections will discuss signals for both busses.

6.2.3.1 386 SX LOCAL BUS

For typical designs, the pullup resistors shown in Table 6-1 are recommended. This table correlates to Chapter 7 of the 386 SX Data Sheet. However, particular designs may have a need to differ from the listed values. Design analysis is recommended to determine specific requirements.

6.2.3.2 82835SX Local Bus

Pullup resistor recommendations for the 82385SX Local Bus signals are shown in Table 6-2. Design analysis is necessary to determine if deviations to the typical values given are needed.

Table 6-1. Recommended Resistor Pullups to V_{CC} (386™ SX Local Bus)

Pin and Signal	Pullup Value	Purpose
ADS# PGA E13 PQFP 123	20 KΩ ±10%	Lightly Pull ADS# Negated for 386 SX Hold States
LOCK# PGA F13 PQFP 118	20 KΩ ±10%	Lightly Pull LOCK# Negated for 386 SX Hold States

Table 6-2. Recommended Resistor Pullups to V_{CC} (82385SX Local Bus)

Signal and Pin	Pullup Value	Purpose
BADS# PGA N9 PQFP 89	20 KΩ ±10%	Lightly Pull BADS# Negated for 82385SX Hold States
BLOCK# PGA P9 PQFP 86	20 KΩ ±10%	Lightly Pull BLOCK# Negated for 82385SX Hold States
MISS# PGA N8 PQFP 85	20 KΩ ±10%	Lightly Pull MISS# Negated for 82385SX Hold States

6.3 82385SX Signal Connections

6.3.1 CONFIGURATION INPUTS

The 82835 configuration signals (M/S#, 2W/D#, DEFOE#) must be connected (pulled up) to the appropriate logic level for the system design. There is also a reserved 82385SX input which must be tied to the appropriate level. Refer to Table 6-3 for the signals and their required logic level.

Table 6-3. 82385SX Configuration Inputs Logic Levels

Pin and Signal	Logic Level	Purpose
M/S# PGA B13 PQFP 124	High	Master Mode Operation
	Low	Slave Mode Operation
2W/D# PGA D12 PQFP 127	High	2-Way Set Associative
	Low	Direct Mapped
Reserved PGA L14 PQFP 102	High	Must be tied to V_{CC} via a pull-up for proper functionality
DEFOE# PGA A14 PQFP 128	N/A	Define Cache Output Enable. Allows use of any SRAM.

NOTE:
The listed 82385SX pins which need to be tied high should use a pull-up resistor in the range of 5 KΩ to 20 KΩ.

6.3.2 CLK2 and RESET

The 82385SX has two inupts to which the 386 SX CLK2 signal must be connected. One is labeled CLK2 (82385SX pin C13) and the other is labeled BCLK2 (82385SX pin L13). These two inputs must be tied together on the printed circuit board.

The 82385SX also has two reset inputs. RESET (82385SX pin D13) and BRESET (82385SX pin K12) must be connected on the printed circuit board.

6.4 Unused Pin Requirements

For reliable operation, ALWAYS connect unused inputs to a valid logic level. As is the case with most other CMOS processes, a floating input will increase the current consumption of the component and give an indeterminate state to the component.

6.5 Cache SRAM Requirements

The 82385SX offers the option of using SRAMs with or without an output enable pin. This is possible by inserting a transceiver between the SRAMs and the 386 SX local data bus and strapping DEFOE# to the appropriate logic level for a given system configuration. This transceiver may also be desirable in a system which has a very heavily loaded 386 SX local data bus. The following sections discuss the SRAM requirements for all cache configurations.

6.5.1 CACHE MEMORY WITHOUT TRANSCEIVERS

As discussed in Section 3.2, the 82385SX presents all of the control signals necessary to access the cache memory. The SRAM chip selects, write enables, and output enables are driven directly by the 82385SX. Table 6-4 lists the required SRAM specifications. These specifications allow for zero margins. They should be used as guides for the actual system design.

Table 6-4. SRAM Specs for Non-Buffered Cache Memory

SRAM Spec Requirements				
	Direct Mapped		2-Way Set Associative	
	16 MHz	20 MHz	16 MHz	20 MHz
Read Cycle Requirements				
Address Access (MAX)	64 ns	44 ns	62 ns	42 ns
Chip Select Access (MAX)	76	56	76	56
OE# to Data Valid (MAX)	25	19	19	14
OE# to Data Float (MAX)	20	20	20	20
Write Cycle Requirements				
Chip Select to End of Write (MIN)	40	30	40	30
Address Valid to End of Write (MIN)	58	42	56	40
Write Pulse Width (MIN)	40	30	40	30
Data Setup (MAX)	—	—	—	—
Data Hold (MIN)	4	4	4	4

6.5.2 CACHE MEMORY WITH TRANSCEIVERS

To implement an 82385SX subsystem using cache memory transceivers, COEA# or COEB# must be used as output enable signals for the transceivers and DEFOE# must be appropriately strapped for proper COEx# functionality (since the cache SRAM transceivers must be enabled for writes as well as reads). DEFOE# must be tied high when using cache SRAM transceivers. In a 2-way set associative organization, COEA# enables the transceiver for bank A and COEB# enables the bank B transceiver. A direct mapped cache may use either COEA# or COEB# to enable the transceiver. Table 6-5 lists the required SRAM specifications. These specifications allow for zero margin. They should be used as guides for the actual system design.

7.0 SYSTEM TEST CONSIDERATIONS

7.1 Introduction

Power On Self Testing (POST) is performed by most systems after a reset. This chapter discusses the requirements for properly testing an 82385SX based system after power up.

7.2 Main Memory (DRAM) Testing

Most systems perform a memory test by writing a data pattern and then reading and comparing the data. This test may also be used to determine the total available memory within the system. Without properly taking into account the 82385SX cache memory, the memory test can give erroneous results. This will occur if the cache responds with read hits during the memory test routine.

7.2.1 MEMORY TESTING ROUTINE

In order to properly test main memory, the test routine must not read from the same block consecutively. For instance, if the test routine writes a data pattern to the first 16 Kbytes of memory (0000–3FFFH), reads from the same block, writes a new pattern to the same locations (0000–3FFFH), and read the new pattern, the second pattern tested would have had data returned from the 82385SX cache memory. Therefore, it is recommended that the test routine work with a memory block of at least 32 Kbytes. This will guarantee that no 16 Kbyte block will be read twice consecutively.

7.3 82385SX Cache Memory Testing

With the addition of SRAMs for the cache memory, it may be desirable for the system to be able to test the cache SRAMs during system diagnostics. This requires the test routine to access only the cache memory. The requirements for this routine are based on where it resides within the memory map. This can

5

Table 6-5. SRAM Specs for Buffered Cache Memory

SRAM Spec Requirements				
	Direct Mapped		2-Way Set Associative	
	16 MHz	20 MHz	16 MHz	20 MHz
Read Cycle Requirements				
Address Access (MAX)	57 ns	37 ns	55 ns	35 ns
Chip Select Access (MAX)	68	48	68	48
OE# to Data Valid (MAX)	N/A	N/A	N/A	N/A
OE# to Data Float (MAX)	N/A	N/A	N/A	N/A
Write Cycle Requirements				
Chip Select to End of Write (MIN)	40	30	40	30
Address Valid to End of Write (MIN)	58	42	56	40
Write Pulse Width (MIN)	40	30	40	30
Data Setup (MAX)	25	15	25	15
Data Hold (MIN)	3	3	3	3

be broken into two areas: the routine residing in cacheable memory space or the routine residing in either non-cacheable memory or on the 386 SX local bus (using the LBA# input).

7.3.1 TEST ROUTINE IN THE NCA# OR LBA# MEMORY MAP

In this configuration, the test routine will never be cached. The recommended method is code which will access a single 16 Kbyte block during the test. Initially, a 16 Kbyte read (assume 0000–3FFFH) must be executed. This will fill the cache directory with the address information which will be used in the diagnostic procedure. Then, a 16 Kbyte write to the same address locations (0000–3FFFH) will load the cache with the desired test pattern (due to write hits). The comparison can be made by completing another 16 Kbyte read (same locations, 0000–3FFFH), which will be cache read hits. Subsequent writes and reads to the same addresses will enable various patterns to be tested.

7.3.2 TEST ROUTINE IN CACHEABLE MEMORY

In this case, it must be understood that the diagnostic routine must reside in the cache memory before the actual data testing can begin. Otherwise, when the 386 SX performs a code fetch, a location within the cache memory which is to be tested will be altered due to the read miss (code fetch) update.

The first task is to load the diagnostic routine into the top of the cache memory. It must be known how much memory is required for the code as the rest of the cache memory will be tested as in the earlier method. Once the diagnostics have been cached (via read updates), the code will perform the same type of read/write/read/compare as in the routine explained in the above section. The difference is that now the amount of cache memory to be tested is 16 Kbytes minus the length of the test routine.

7.4 82385SX Cache Directory Testing

Since the 82385SX does not directly access the data bus, it is not possible to easily complete a comparison of the cache directory. (The 82385SX can serially transmit its directory contents. See Section 7.5.) However, the cache memory tests described in Section 7.3 will indicate if the directory is working properly. Otherwise, the data comparison within the diagnostics will show locations which fail.

There is a slight possibility that the cache memory comparison could pass even if locations within the directory gave false hit/miss results. This could cause the comparison to always be performed to main memory instead of the cache and give a proper comparison to the 386 SX. The solution here is to use the MISS# output of the 82385SX as an indicator to a diagnostic port which can be read by the 386 SX. It could also be used to flag an interrupt if a failure occurs.

The implementation of these techniques in the diagnostics will assure proper functionality of the 82385SX subsystem.

7.5 Special Function Pins

As mentioned in Chapter 3, there are three 82385SX pins which have reserved functions in addition to their normal operational functions. These pins are MISS#, WBS, and FLUSH.

As discussed previously, the 82385SX performs a directory flush when the FLUSH input is held active for at least 4 CLK (8 CLK2) cycles. However, the FLUSH pin also serves as a diagnostic input to the 82385SX. The 82385SX will enter a reserved mode if the FLUSH pin is high at the falling edge of RESET.

If, during normal operation, the FLUSH input is active for only one CLK (2 CLK2) cycle/s, the 82385SX will enter another reserved mode. Therefore it must be guaranteed that FLUSH is active for at least the 4 CLK (8 CLK2) cycle specification.

WBS and MISS# serve as outputs in the 82385SX reserved modes.

8.0 MECHANICAL DATA

8.1 Introduction

This chapter discusses the physical package and its connections in detail.

8.2 Pin Assignment

The 82385SX PGA pinout as viewed from the top side of the component is shown by Figure 8-1. Its pinout as viewed from the Pin side of the component is shown in Figure 8-2.

The 82385SX Plastic Quad Flat Pack (PQFP) pinout from the top side of the component is shown by Figure 8-3.

V_{CC} and V_{SS} connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Each V_{CC} and V_{SS} must be connected to the appropriate voltage level. The circuit board should include V_{CC} and GND planes for power distribution and all V_{CC} and V_{SS} pins must be connected to the appropriate plane.

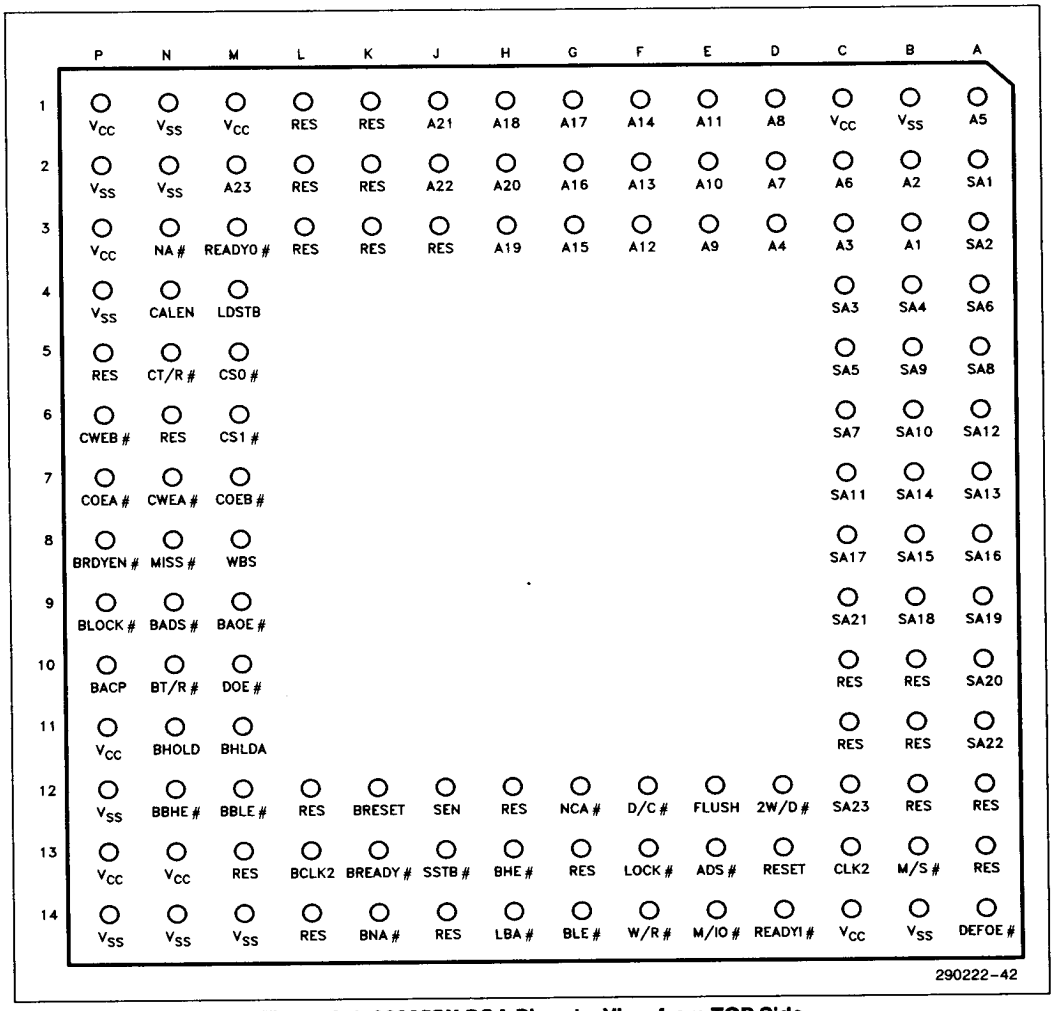


Figure 8-1. 82385SX PGA Pinout—View from TOP Side

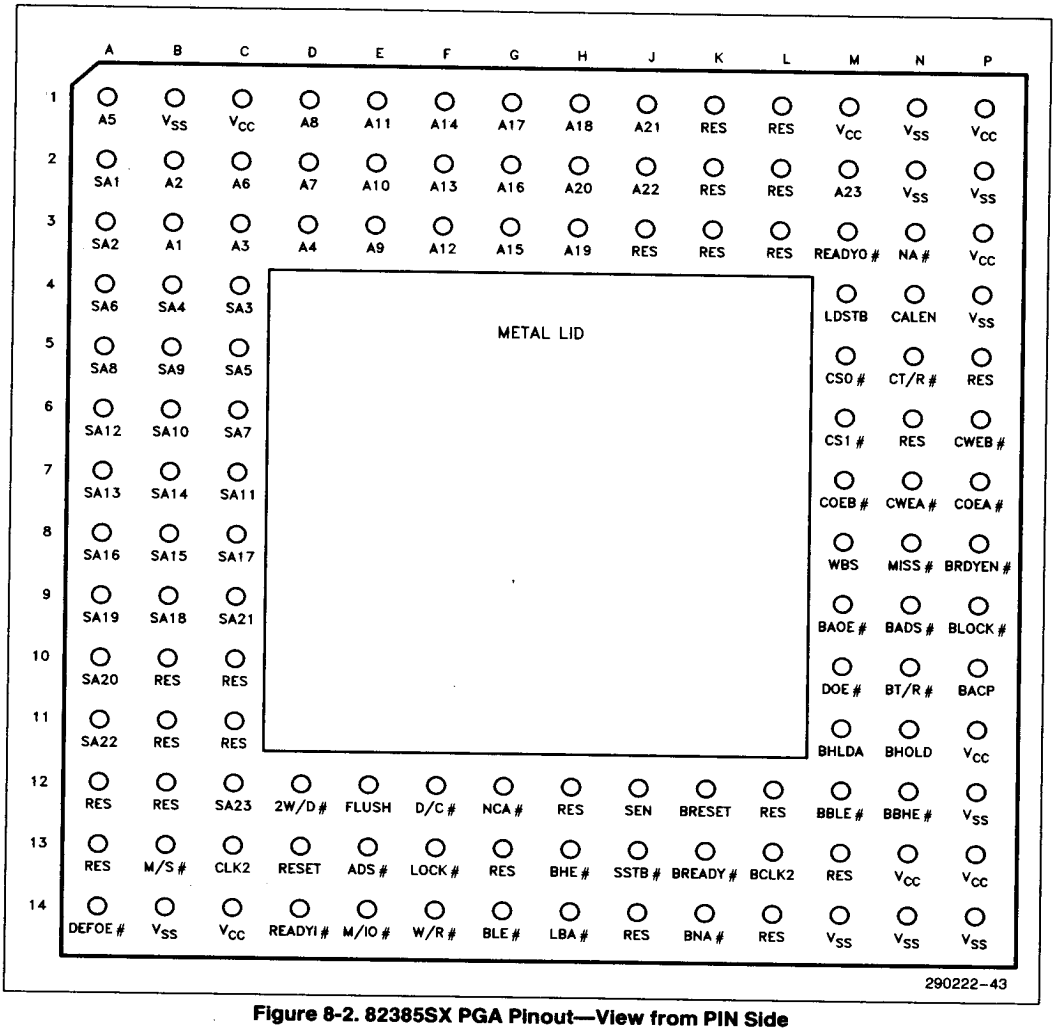


Figure 8-2. 82385SX PGA Pinout—View from PIN Side

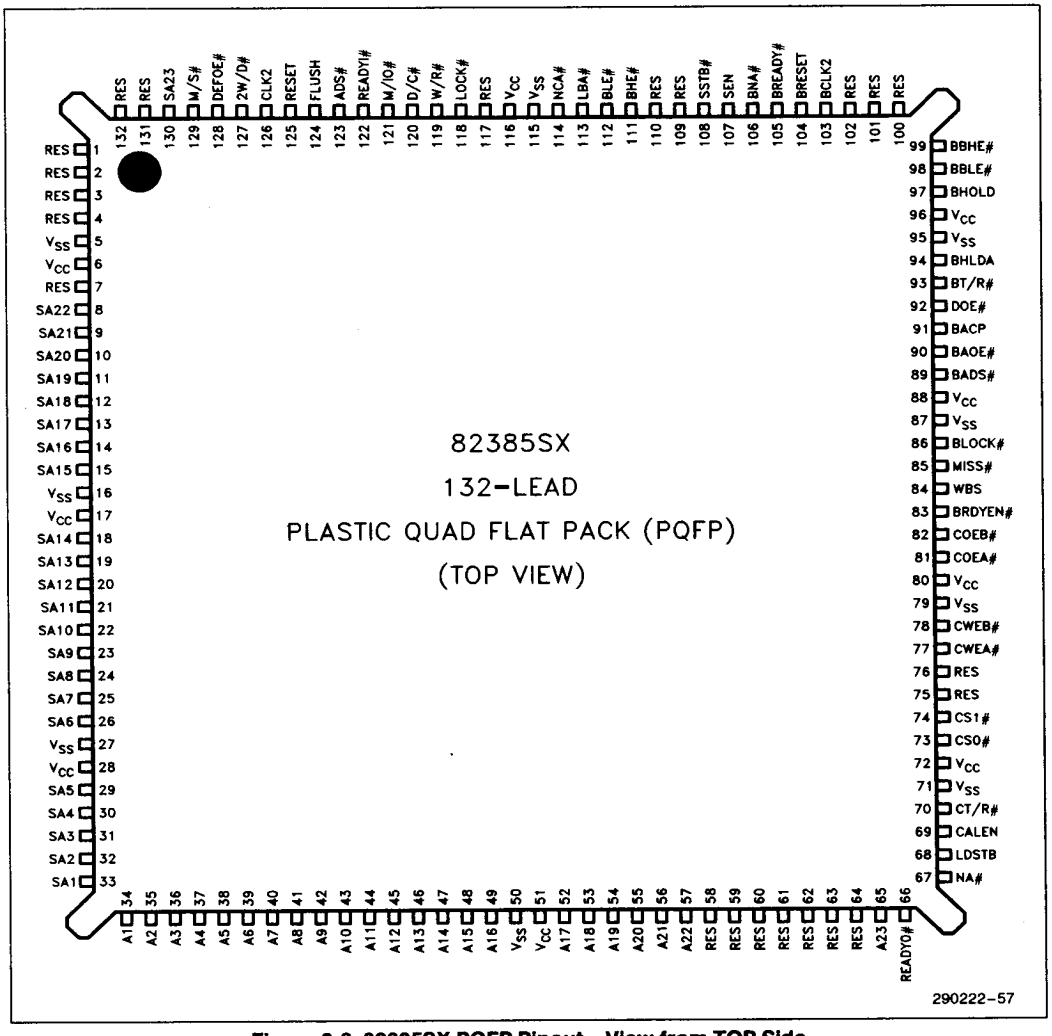


Figure 8-3. 82385SX PQFP Pinout—View from TOP Side

Table 8-1. 82385SX Pinout—Functional Grouping

PGA	PQFP	Signal
M2	65	A23
J2	57	A22
J1	56	A21
H2	55	A20
H3	54	A19
H1	53	A18
G1	52	A17
G2	49	A16
G3	48	A15
F1	47	A14
F2	46	A13
F3	45	A12
E1	44	A11
E2	43	A10
E3	42	A9
D1	41	A8
D2	40	A7
C2	39	A6
A1	38	A5
D3	37	A4
C3	36	A3
B2	35	A2
B3	34	A1
G14	112	BLE#
H13	111	BHE#
C13	126	CLK2
D13	125	RESET
K12	104	BRESET
L13	103	BCLK2
F14	119	W/R#
F12	120	D/C#
E14	121	M/IO#
F13	118	LOCK#
E13	123	ADS#

PGA	PQFP	Signal
G12	114	NCA#
H14	113	LBA#
D14	122	READYI#
M3	66	READYO#
C12	130	SA23
A11	8	SA22
C9	9	SA21
A10	10	SA20
A9	11	SA19
B9	12	SA18
C8	13	SA17
A8	14	SA16
B8	15	SA15
B7	18	SA14
A7	19	SA13
A6	20	SA12
C7	21	SA11
B6	22	SA10
B5	23	SA9
A5	24	SA8
C6	25	SA7
A4	26	SA6
C5	29	SA5
B4	30	SA4
C4	31	SA3
A3	32	SA2
A2	33	SA1
J12	107	SEN#
J13	108	SSTB#
C1	6	V_{CC}
C14	17	V_{CC}
M1	28	V_{CC}
N13	51	V_{CC}
P1	72	V_{CC}
P3	80	V_{CC}
P11	88	V_{CC}
P13	96	V_{CC}
—	116	V_{CC}

PGA	PQFP	Signal
N3	67	NA#
E12	124	FLUSH
M8	84	WBS
N8	85	MISS#
A14	128	DEFOE#
B13	129	M/S#
D12	127	2W/D#
M10	92	DOE#
M4	68	LDSTB
N11	97	BHOLD
M11	94	BHLDA
B1	5	V_{SS}
B14	16	V_{SS}
M14	27	V_{SS}
N1	50	V_{SS}
N2	71	V_{SS}
N14	79	V_{SS}
P2	87	V_{SS}
P4	95	V_{SS}
P12	115	V_{SS}
P14	—	V_{SS}
N9	89	BADS#
M12	98	BBLE#
N12	99	BBHE#
P9	86	BLOCK#
K14	106	BNA#
N4	69	CALEN
P7	81	COEA#
M7	82	COEB#
N7	77	CWEA#
P6	78	CWEB#
M5	73	CS0#
M6	74	CS1#

PGA	PQFP	Signal
N5	70	CT/R#
P8	83	BRDYEN#
K13	105	BREADY#
P10	91	BACP
M9	90	BAOE#
N10	93	BT/R#
A12	1	V_{CC} (*)
A13	131	V_{CC} (*)
B10	7	V_{CC} (*)
B11	3	V_{CC} (*)
B12	132	V_{CC} (*)
C10	4	V_{CC} (*)
C11	2	V_{CC} (*)
G13	117	V_{CC} (*)
H12	110	V_{CC} (*)
J3	60	V_{CC} (*)
J14	109	V_{CC} (*)
K1	58	V_{CC} (*)
K2	59	V_{CC} (*)
K3	62	V_{CC} (*)
L1	61	V_{CC} (*)
L2	63	V_{CC} (*)
L3	64	V_{CC} (*)
L12	100	N.C. (*)
L14	102	V_{CC} (*)
M13	101	N.C. (*)
N6	75	N.C. (*)
P5	76	N.C. (*)

*Reserved pins, N.C. indicates a no connect.

8.3 Package Dimensions and Mounting

The 82385SX PGA package is a 132-pin ceramic Pin Grid Array. The pins are arranged 0.100 inch (2.54 mm) center-to-center, in a 14 × 14 matrix, three rows around.

A wide variety of available PGA sockets allow low insertion force or zero insertion force mounting. These come in a choice of terminals such as solder-tail, surface mount, or wire wrap.

The 82385SX PQFP is a 132-lead Plastic Quad Flat Pack. The pins are "fine pitch", 0.025 inches (0.635 mm) center to center.

The PQFP device is intended to be surface mounted directly to the printed board although sockets are available for this device.

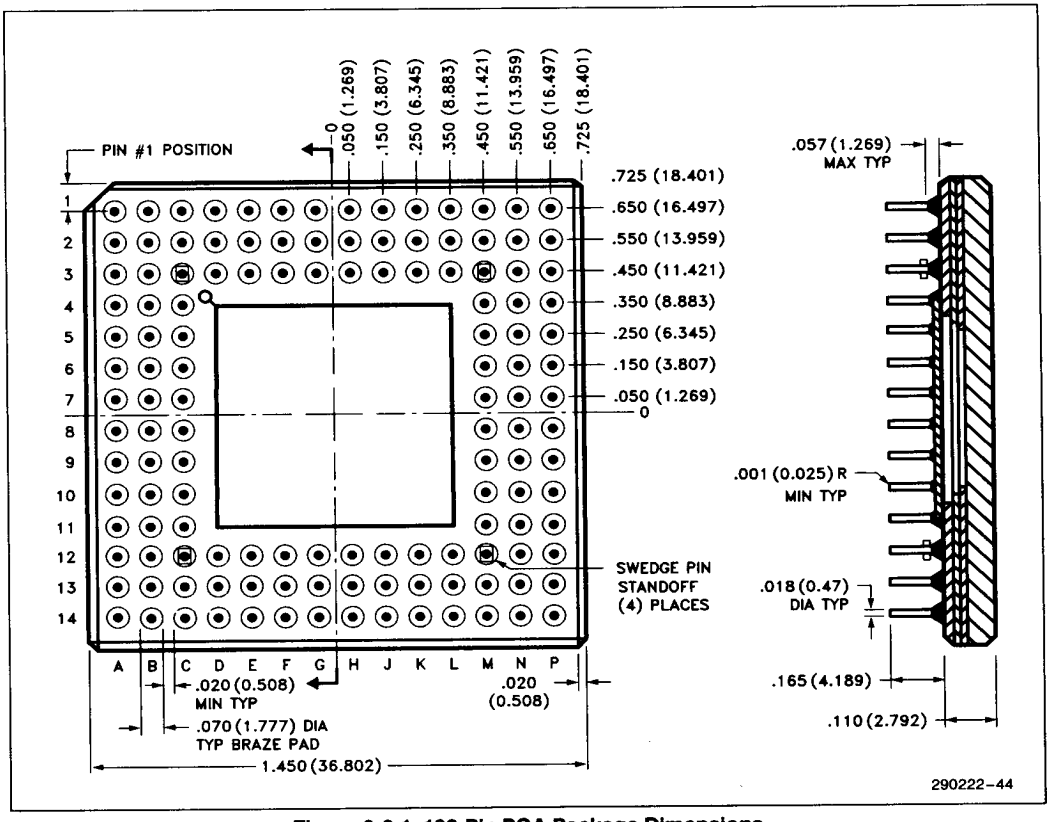


Figure 8-3.1. 132-Pin PGA Package Dimensions

5

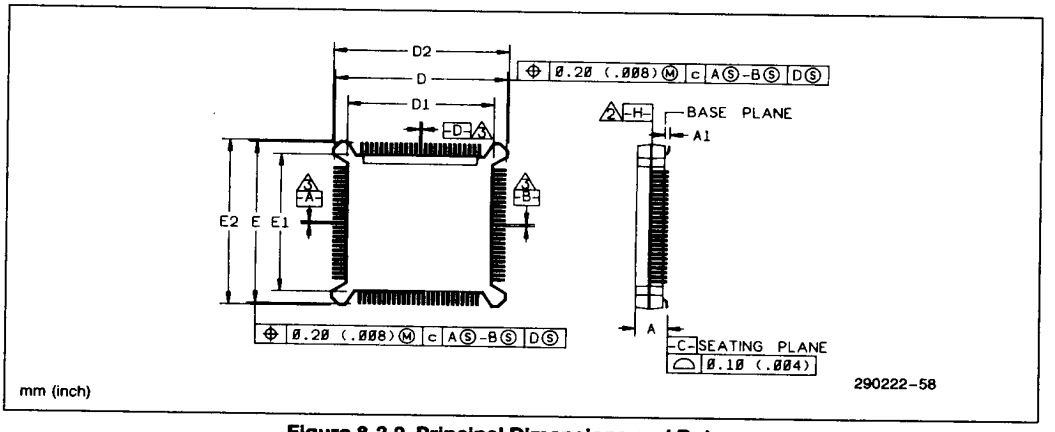


Figure 8-3.2. Principal Dimensions and Datums

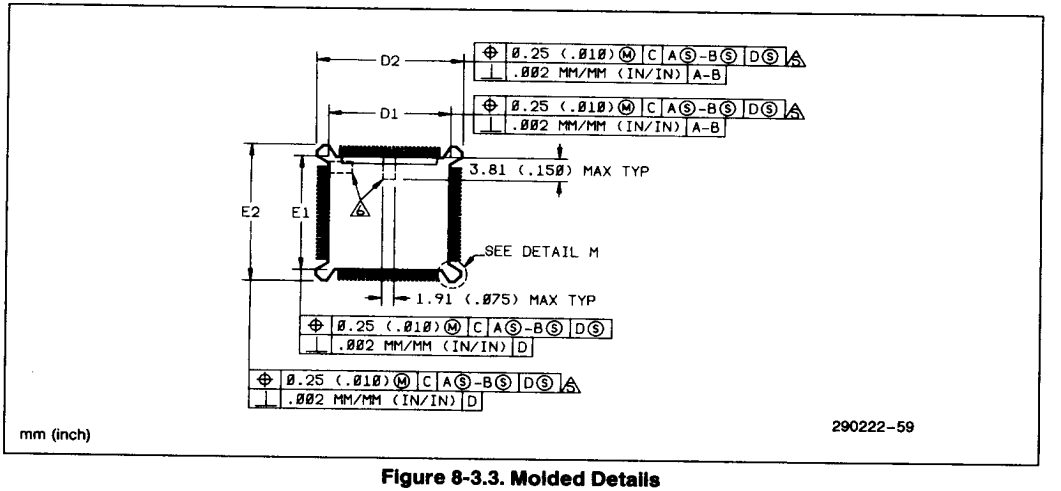


Figure 8-3.3. Molded Details

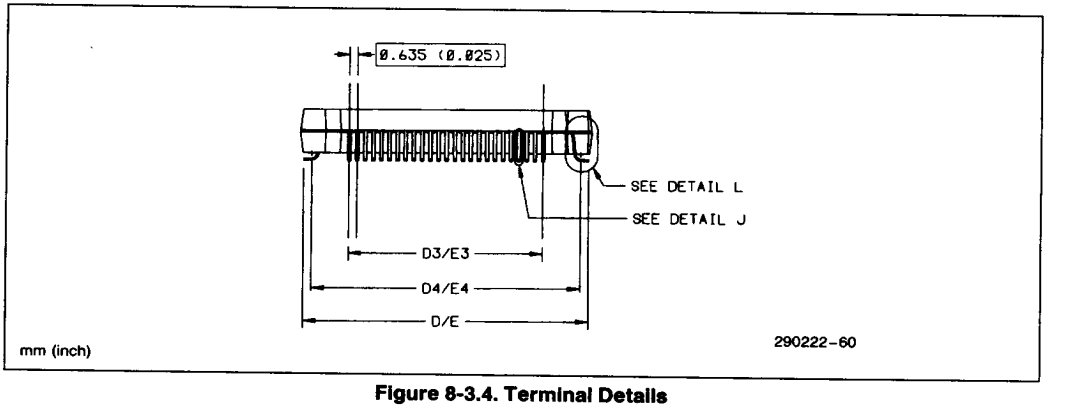


Figure 8-3.4. Terminal Details

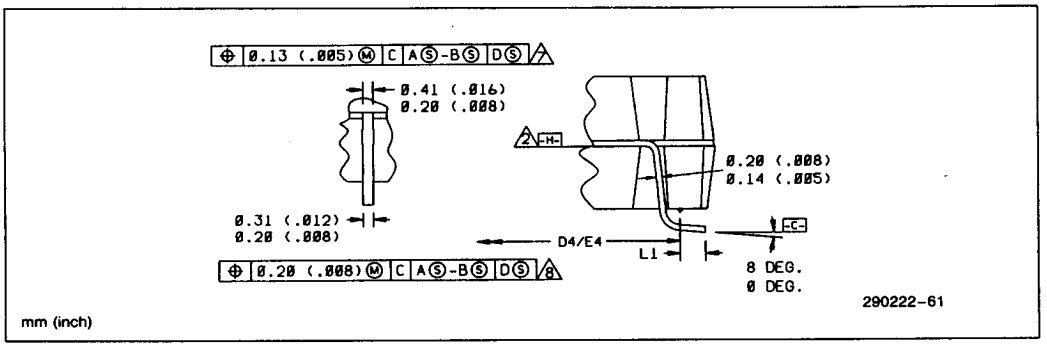


Figure 8-3.5. Typical Lead

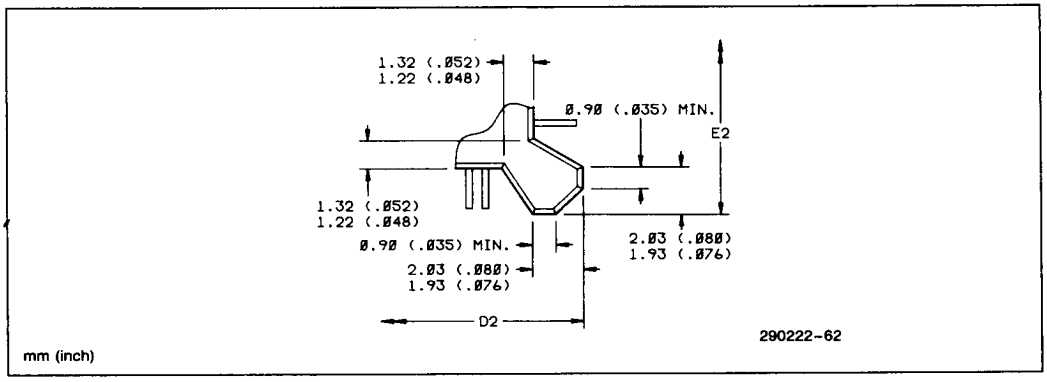


Figure 8-3.6. Detail M

5

PLASTIC QUAD FLAT PACK

Table 8-3.1. Symbol List for Plastic Quad Flat Pack

Letter or Symbol	Description of Dimensions
A	Package height: distance from seating plane to highest point of body
A1	Standoff: Distance from seating plane to base plane
D/E	Overall package dimension: lead tip to lead tip
D1/E1	Plastic body dimension
D2/E2	Bumper Distance
D3/E3	Footprint
L1	Foot length
N	Total number of leads

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane -H- located at the mold parting line and coincident with the bottom of the lead where lead exits plastic body.
3. Datums A-B and -D- to be determined where center leads exit plastic body at datum plane -H-.
4. Controlling Dimension, Inch.
5. Dimensions D1, D2, E1 and E2 are measured at the mold parting line and do not include mold protrusion. Allowable mold protrusion of 0.18 mm (0.007 in) per side.
6. Pin 1 identifier is located within one of the two zones indicated.
7. Measured at datum plane -H-.
8. Measured at seating plane datum -C-.

Table 8-3.2. PQFP Dimensions and Tolerances

Intel Case Outline Drawings Plastic Quad Flat Pack 0.025 Inch Pitch			
Symbol	**Description**	**Min**	**Max**
N	Leadcount	132	
A	Package Height	0.160	0.170
A1	Standoff	0.020	0.030
D, E	Terminal Dimension	1.075	1.085
D1, E1	Package Body	0.947	0.953
D2, E2	Bumper Distance	1.097	1.103
D3, E3	Lead Dimension	0.800 REF	
L1	Foot Length	0.020	0.030
Issue	IWS Preliminary 1/15/87		

Intel Case Outline Drawings Plastic Quad Flat Pack 0.64 mm Pitch			
Symbol	**Description**	**Min**	**Max**
N	Leadcount	132	
A	Package Height	4.06	4.32
A1	Standoff	0.51	0.76
D, E	Terminal Dimension	27.31	27.56
D1, E1	Package Body	24.05	24.21
D2, E2	Bumper Distance	27.86	28.02
D3, E3	Lead Dimension	20.32 REF	
L1	Foot Length	0.51	0.76
Issue	IWS Preliminary 1/15/87		

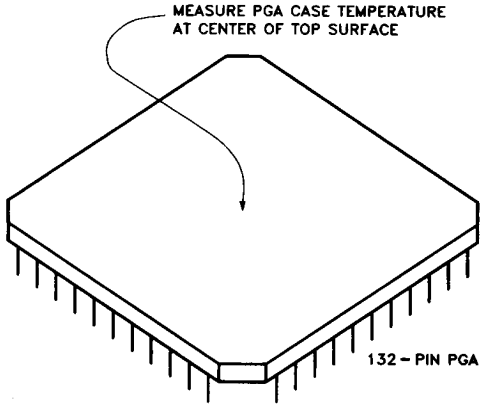
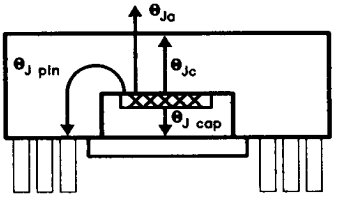


Figure 8-3.7. Measuring 82385SX PGA Case Temperature

Table 8-3.3. 82385SX PGA Package Typical Thermal Characteristics

Parameter	Thermal Resistance—°C/Watt						
	Airflow—f^3/min (m^3/sec)						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ Junction-to-Case (Case Measured as Figure 8-3.7)	2	2	2	2	2	2	2
θ Case-to-Ambient (No Heatsink)	19	18	17	15	12	10	9
θ Case-to-Ambient (with Omnidirectional Heatsink)	16	15	14	12	9	7	6
θ Case-to-Ambient (with Unidirectional Heatsink)	15	14	13	11	8	6	5

NOTES:
1. Table 8-3.3 applies to 82385SX PGA plugged into socket or soldered directly onto board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$.
3. $\theta_{J\text{-}CAP}$ = 4°C/W (approx.)
   $\theta_{J\text{-}PIN}$ = 4°C/W (inner pins) (approx.)
   $\theta_{J\text{-}PIN}$ = 8°C/W (outer pins) (approx.)



290222-46

Table 8-3.4. 82385 PQFP Package Typical Thermal Characteristics

Parameter	Thermal Resistance—°C/Watt						
	Airflow—/LFM						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ Junction-to-Case (Case Measured as Figure 8-3.7)	5	5	5	5	5	5	5
θ Case-to-Ambient (No Heatsink)	23.5	22.0	20.5	17.5	14.0	11.5	9.5
θ Case-to-Ambient (with Omnidirectional Heatsink)	TO BE DEFINED						
θ Case-to-Ambient (with Unidirectional Heatsink)							

NOTES:
1. Table 8-3.4 applies to 82385SX PQFP plugged into socket or soldered directly onto board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$.
3. $\theta_{J\text{-}CAP}$ = 4°C/W (approx.)
   $\theta_{J\text{-}PIN}$ = 4°C/W (inner pins) (approx.)
   $\theta_{J\text{-}PIN}$ = 8°C/W (outer pins) (approx.)

8.4 Package Thermal Specification

The case temperature should be measured at the center of the top surface as in Figure 8-3.7 for PGA or Table 8-3.3 for PQFP. The case temperature may be measured in any environment to determine whether or not the 82385SX is within the specified operating range.

9.0 ELECTRICAL DATA

9.1 Introduction

This chapter presents the A.C. and D.C specifications for the 82385SX.

9.2 Maximum Ratings

Storage Temperature ..... −65°C to +150°C
Case Temperature under Bias ... −65°C to +110°C
Supply Voltage
with Respect to V_{SS} ..... −0.5V to +6.5V
Voltage on Any Other Pin .... −0.5V to V_{CC} + 0.5V

NOTE:
Stress above those listed may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those listed in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Although the 82385SX contains protective circuitry to resist damage from static electric discharges, always take precautions against high static voltages or electric fields.

9.3 D.C. Specifications T_{CASE} = 0°C to +85°C; V_{CC} = 5V ±5%; V_{SS} = 0V

Table 9-1. D.C. Specifications (16 MHz and 20 MHz)

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IL}	Input Low Voltage	−0.3	0.8	V	(Noe 1)
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{CL}	CLK2, BCLK2 Input Low	−0.3	0.8	V	(Note 1)
V_{CH}	CLK2, BCLK2 Input High	V_{CC} − 0.8	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −1 mA
I_{CC}	Power Supply Current		275	mA	(Note 2)
I_{LI}	Input Leakage Current		±15	μA	0V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±15	μA	0.45V < V_{OUT} < V_{CC}
C_{IN}	Input Capacitance		10	pF	(Note 3)
C_{CLK}	CLK2 Input Capacitance		20	pF	(Note 3)

NOTES:
1. Minimum value is not 100% tested.
2. I_{CC} is specified with inputs driven to CMOS levels. I_{CC} may be higher if driven to TTL levels.
3. Sampled only.

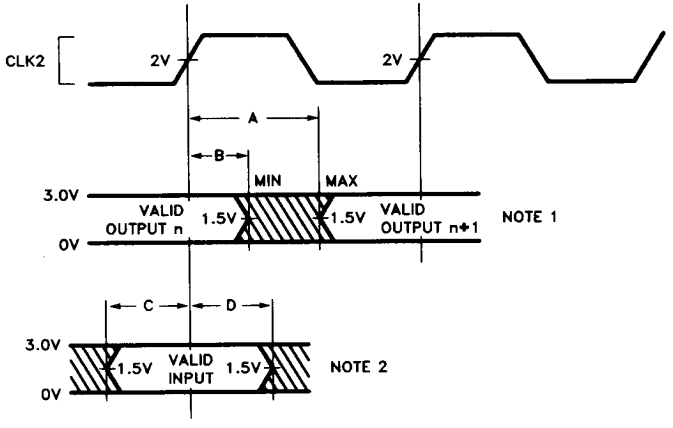
9.4 A.C. Specifications

The A.C. specifications given in the following tables consist of output delays and input setup requirements. The A.C. diagram's purpose is to illustrate the clock edges from which the timing parameters are measured. The reader should not infer any other timing relationships from them. For specific information on timing relationships between signals, refer to the appropriate functional section.

A.C. spec measurement is defined in Figure 9-1. Inputs must be driven to the levels shown when A.C. specifications are measured. 82385SX output delays are specified with minimum and maximum limits, which are measured as shown. 82385SX input setup and hold times are specified as minimums and define the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct 82385SX operation.

9.4.1 FREQUENCY DEPENDENT SIGNALS

The 82385SX has signals whose output valid delays are dependent on the clock frequency. These signals are marked in the A.C. Specification Tables with a Note 1.



LEGEND:
A—Maximum output delay specification
B—Minimum output delay specification
C—Minimum input setup specification
D—Minimum input hold specification

NOTES:
1. Under rated loading 82385SX output (t_r and t_f) is typically ≤ 4.0 ns from 0.8V to 2.0V.
2. Input waveforms have t_r ≤ 2.0 ns from 0.8V to 2.0V.

Figure 9-1. Drive Levels and Measurement Points for A.C. Specification

5

A.C. SPECIFICATION TABLES

Functional operating range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C

A.C. Specifications at 16 MHz

Symbol	Parameter	Min	Max	Units	Notes
t1	Operating Frequency	15.4	16	MHz	
t2	CLK2, BCLK2 Period	31.25	32.5	ns	
t3a	CLK2, BCLK2 High Time @ 2V	10		ns	
t3b	CLK2, BCLK2 High Time @ 3.7V	7		ns	3
t4a	CLK2, BCLK2 Low Time @ 2V	10		ns	
t4b	CLK2, BCLK2 Low Time @ 0.8V	7		ns	3
t5	CLK2, BCLK2 Fall Time		8	ns	3, 9
t6	CLK2, BCLK2 Rise Time		8	ns	3, 9
t7a	A4–A12 Setup Time	30		ns	1
t7b	LOCK# Setup Time	19		ns	1
t7c	BLE#, BHE# Setup Time	21		ns	1
t7d	A1–A3, A13–A23 Setup Time	23		ns	1
t8	A1–A23, BLE#, BHE#, LOCK# Hold	3		ns	
t9a	M/IO#, D/C# Setup Time	30		ns	1
t9b	W/R# Setup Time	30		ns	1
t9c	ADS# Setup Time	30		ns	1
t10	M/IO#, D/C#, W/R#, ADS# Hold Time	5		ns	
t11	READYI# Setup Time	19		ns	1
t12	READYI# Hold Time	4		ns	
t13a1	NCA# Setup Time (See t55b2)	27		ns	6
t13a2	NCA# Setup Time (See t55b3)	20		ns	6
t13b	LBA# Setup Time	16		ns	
t14a	NCA# Hold Time	4		ns	
t14b	LBA# Hold Time	4		ns	
t15	RESET, BRESET Setup Time	13		ns	
t16	RESET, BRESET Hold Time	4		ns	
t17	NA# Valid Delay	12	42	ns	1 (25 pF Load)
t18	READYO# Valid Delay	3	31	ns	1 (25 pF Load)
t19	BRDYEN# Valid Delay	3	31	ns	
t21a1	CALEN Rising, PHI1	3	30	ns	
t21a2	CALEN Falling, PHI1	3	30	ns	
t21a3	CALEN Falling in T1P, PHI2	3	30	ns	
t21b	CALEN Rising Following CWTH	3	39	ns	1
t21c	CALEN Pulse Width	10		ns	
t21d	CALEN Rising to CS# Falling	13		ns	

A.C. SPECIFICATION TABLES (Continued)

Functional operating range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C

A.C. Specifications at 16 MHz (Continued)

Symbol	Parameter	Min	Max	Units	Notes
t22a1	CWEx# Falling, PHI1 (CWTH)	4	31	ns	1
t22a2	CWEx# Falling, PHI2 (CRDM)	4	31	ns	1
t22b	CWEx# Pulse Width	40		ns	1, 2
t22c1	CWEx# Rising, PHI1 (CWTH)	4	31	ns	1
t22c2	CWEx# Rising, PHI2 (CRDM)	4	31	ns	1
t23a1	CS1#, CS2# Rising, PHI1 (CRDM)	6	41	ns	1
t23a2	CS1#, CS2# Rising, PHI2 (CWTH)	6	41	ns	1
t23a3	CS1#, CS2# Falling, PHI1 (CWTH)	6	41	ns	1
t23a4	CS1#, CS2# Falling, PHI2 (CRDM)	6	41	ns	1
t24a1	CT/R# Rising, PHI2 (CRDH)	6	43	ns	1
t24a2	CT/R# Falling, PHI1 (CRDH)	6	43	ns	1
t24a3	CT/R# Falling, PHI2 (CRDH)	6	43	ns	1
t25a	COEA#, COEB# Falling (Direct)	4	33	ns	(25 pF Load)
t25b	COEA#, COEB# Falling (2-Way)	4	34	ns	1 (25 pF Load)
t25c1	COEx# Rising Delay @ T_{CASE} = 0C	4	20	ns	(25 pF Load)
t25c2	COEx# Rising Delay @ T_{CASE} = T_{MAX}	4	20	ns	(25 pF Load)
t23b	COEx# Falling to CSx# Rising	0		ns	
t25d	CWEx# Falling to COEx# Falling or CWEx# Rising to COEx# Rising	0	10	ns	(25 pF Load)
t26	CS0#, CS1# Falling to CWEx# Rising	40		ns	1, 2
t27	CWEx# Falling to CS0#, CS1# Falling	0		ns	
t28a	CWEx# Rising to CALEN Rising	0		ns	
t28b	CWEx# Rising to CS0#, CS1# Falling	0		ns	
t31	SA(1-23) Setup Time	25		ns	
t32	SA(1-23) Hold Time	3		ns	
t33	BADS# Valid Delay	4	33	ns	1
t34	BADS# Float Delay	4	33	ns	3
t35	BNA# Setup Time	11		ns	
t36	BNA# Hold Time	15		ns	
t37	BREADY# Setup Time	31		ns	1
t38	BREADY# Hold Time	4		ns	
t40a	BACP Rising Delay	0	26	ns	
t40b	BACP Falling Delay	0	28	ns	
t41	BAOE# Valid Delay	3	23	ns	

A.C. SPECIFICATION TABLES (Continued)

Functional operating range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C

A.C. Specifications at 16 MHz (Continued)

Symbol	Parameter	Min	Max	Units	Notes
t43a	BT/R# Valid Delay	2	27	ns	
t43b1	DOE# Falling Delay	2	30	ns	
t43b2	DOE# Rising Delay @ T_{CASE} = 0C	3	23	ns	
t43b3	DOE# Rising Delay @ T_{CASE} = T_{MAX}	3	26	ns	
t43c	LDSTB Valid Delay	2	33	ns	
t44a	SEN Setup Time	15		ns	
t44b	SSTB# Setup Time	15		ns	
t45	SEN, SSTB# Hold Time	5		ns	
t46	BHOLD Setup Time	26		ns	
t47	BHOLD Hold Time	5		ns	
t48	BHLDA Valid Delay	3	33	ns	
t55a	BLOCK# Valid Delay	3	36	ns	1, 5
t55b1	BBxE# Valid Delay	3	36	ns	1, 7
t55b2	BBxE# Valid Delay	3	36	ns	1, 7
t55b3	BBxE# Valid Delay	3	43	ns	1, 7
t55c	LOCK# Falling to BLOCK# Falling	0	36	ns	1, 5
t56	MISS# Valid Delay	3	43	ns	1
t57	MISS#, BBxE#, BLOCK# Float Delay	4	40	ns	3
t58	WBS Valid Delay	3	39	ns	1
t59	FLUSH Setup Time	21		ns	
t60	FLUSH Hold Time	5		ns	
t61	FLUSH Setup to RESET Low	31		ns	
t62	FLUSH Hold from RESET Low	31		ns	

A.C. SPECIFICATION TABLES

Functional operating range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C

A.C. Specifications at 20 MHz

Symbol	Parameter	Min	Max	Units	Notes
t1	Operating Frequency	15.4	20	MHz	
t2	CLK2, BCLK2 Period	25	32.5	ns	
t3a	CLK2, BCLK2 High Time @ 2V	10		ns	
t3b	CLK2, BCLK2 High Time @ 3.7V	7		ns	3
t4a	CLK2, BCLK2 Low Time @ 2V	10		ns	
t4b	CLK2, BCLK2 Low Time @ 0.8V	7		ns	3
t5	CLK2, BCLK2 Fall Time		8	ns	3, 9
t6	CLK2, BCLK2 Rise Time		8	ns	3, 9
t7a1	A4–A12 Setup Time	20		ns	1
t7a2	A1–A3, A13–A19, A21–A23 Setup Time	18		ns	1
t7a3	A20 Setup Time	16		ns	1
t7b	LOCK# Setup Time	16		ns	1
t7c	BLE#, BHE# Setup Time	18		ns	1
t8	A1–A23, BLE#, BHE#, LOCK# Hold	3		ns	
t9a	M/IO#, D/C# Setup Time	20		ns	1
t9b	W/R# Setup Time	20		ns	1
t9c	ADS# Setup Time	22		ns	1
t10	M/IO#, D/C#, W/R#, ADS# Hold Time	5		ns	
t11	READYI# Setup Time	12		ns	1
t12	READYI# Hold Time	4		ns	
t13a1	NCA# Setup Time (See t55b2)	21		ns	6
t13a2	NCA# Setup Time (See t55b3)	16		ns	6
t13b	LBA# Setup Time	10		ns	
t14a	NCA# Hold Time	4		ns	
t14b	LBA# Hold Time	4		ns	
t15	RESET, BRESET Setup Time	12		ns	
t16	RESET, BRESET Hold Time	4		ns	
t17	NA# Valid Delay	12	34	ns	1 (25 pF Load)
t18	READYO# Valid Delay	3	26	ns	1 (25 pF Load)
t19	BRDYEN# Valid Delay	3	26	ns	
t21a1	CALEN Rising, PHI1	3	24	ns	
t21a2	CALEN Falling, PHI1	3	24	ns	
t21a3	CALEN Falling in T1P, PHI2	3	24	ns	
t21b	CALEN Rising Following CWTH	3	34	ns	1
t21c	CALEN Pulse Width	10		ns	

A.C. SPECIFICATION TABLES (Continued)

Functional operating range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C

A.C. Specifications at 20 MHz (Continued)

Symbol	Parameter	Min	Max	Units	Notes
t21d	CALEN Rising to CS# Falling	13		ns	
t22a1	CWEx# Falling, PHI1 (CWTH)	4	27	ns	1
t22a2	CWEx# Falling, PHI2 (CRDM)	4	27	ns	1
t22b	CWEx# Pulse Width	30		ns	1, 2
t22c1	CWEx# Rising, PHI1 (CWTH)	4	27	ns	1
t22c2	CWEx# Rising, PHI2 (CRDM)	4	27	ns	1
t23a1	CS1#, CS2# Rising, PHI1 (CRDM)	6	37	ns	1
t23a2	CS1#, CS2# Rising, PHI2 (CWTH)	6	37	ns	1
t23a3	CS1#, CS2# Falling, PHI1 (CWTH)	6	37	ns	1
t23a4	CS1#, CS2# Falling, PHI2 (CRDM)	6	37	ns	1
t24a1	CT/R# Rising, PHI2 (CRDH)	6	38	ns	1
t24a2	CT/R# Falling, PHI1 (CRDH)	6	38	ns	1
t24a3	CT/R# Falling, PHI2 (CRDH)	6	38	ns	1
t25a	COEA#, COEB# Falling (Direct)	4	22	ns	(25 pF Load)
t25b	COEA#, COEB# Falling (2-Way)	4	24.5	ns	1 (25 pF Load)
t25c	COEx# Rising Delay	5	17	ns	(25 pF Load)
CACHE SRAM WRITE CYCLES					
t23b	COEx# Falling to CSx# Rising	0		ns	8
t25d	CWEx# Falling to COEx# Falling or CWEx# Rising to COEx# Rising	0	10	ns	8 (25 pF Load)
t26	CS0#, CS1# Falling to CWEx# Rising	30		ns	1, 2
t27	CWEx# Falling to CS0#, CS1# Falling	0		ns	
t28a	CWEx# Rising to CALEN Rising	0		ns	
t28b	CWEx# Rising to CS0#, CS1# Falling	0		ns	
t31	SA(1–23) Setup Time	19		ns	
t32	SA(1–23) Hold Time	3		ns	
t33	BADS# Valid Delay	4	28	ns	1
t34	BADS# Float Delay	4	30	ns	3
t35	BNA# Setup Time	9		ns	
t36	BNA# Hold time	15		ns	
t37	BREADY# Setup Time	26		ns	1
t38	BREADY# Hold Time	4		ns	
t40a	BACP Rising Delay	0	20	ns	
t40b	BACP Falling Delay	0	22	ns	

A.C. SPECIFICATION TABLES (Continued)

Functional operating range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C

A.C. Specifications at 20 MHz (Continued)

Symbol	Parameter	Min	Max	Units	Notes
t41	BAOE# Valid Delay	3	18	ns	
t43a	BT/R# Valid Delay	2	19	ns	
t43b1	DOE# Falling Delay	2	23	ns	
t43b2	DOE# Rising Delay @ T_{CASE} = 0C	4	17	ns	
t43b3	DOE# Rising Delay @ T_{CASE} = T_{MAX}	4	19	ns	
t43c	LDSTB Valid Delay	2	26	ns	
t44a	SEN Setup Time	11		ns	
t44b	SSTB# Setup Time	11		ns	
t45	SEN, SSTB# Hold Time	5		ns	
t46	BHOLD Setup Time	17		ns	
t47	BHOLD Hold Time	5		ns	
t48	BHLDA Valid Delay	3	28	ns	
t55a	BLOCK# Valid Delay	3	30	ns	1, 5
t55b1	BBxE# Valid Delay	3	30	ns	1, 7
t55b2	BBxE# Valid Delay	3	30	ns	1, 7
t55b3	BBxE# Valid Delay	3	36	ns	1, 7
t55c	LOCK# Falling to BLOCK# Falling	0	30	ns	1, 5
t56	MISS# Valid Delay	3	35	ns	1
t57	MISS#, BBxE#, BLOCK# Float Delay	4	32	ns	3
t58	WBS Valid Delay	3	37	ns	1
t59	FLUSH Setup Time	16		ns	
t60	FLUSH Hold Time	5		ns	
t61	FLUSH Setup to RESET Low	26		ns	
t62	FLUSH Hold from RESET Low	26		ns	

82385SX A.C. Specification Notes:

1. Frequency dependent specifications.
2. Used for cache data memory (SRAM) specifications.
3. This parameter is sampled, not 100% tested. Guaranteed by design.
5. BLOCK# delay is either from BPHI1 or from 386 LOCK#. Refer to Figures 5-3K and 5-3L in the 82385SX data sheet.
6. NCA# setup time is now specified to the rising edge of BPHI2 in the state after 386 SX addresses become valid (either the state after the first T2 or after the first T2P).
7. BBxE# Valid Delay is a function of NCA# setup.
   BBxE# valid delay:
   - t55b1 For cacheable system bus accesses
   - t55b2 For NCA# setup < t13a1
   - t55b3 For t13a2 < NCA# setup < t13a1

8. t23b and t25d are only valid specifications when DEFOE# = V_{CC}. Otherwise, if DEFOE# = V_{SS}, COEx# is never asserted during cache SRAM write cycles. If DEFOE# = V_{SS}, t23b and t25d are Not Applicable.
9. t5 is measured from 0.8V to 3.7V. t6 is measured from 3.7V to 0.8V.

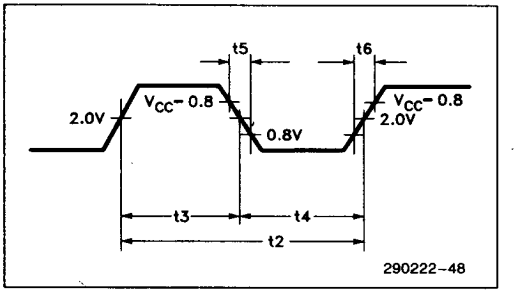


Figure 9-2. CLK2, BCLK2 Timing

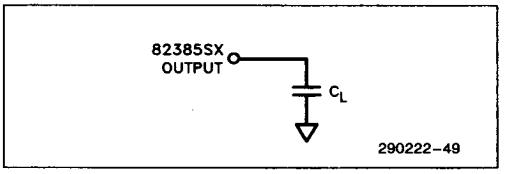
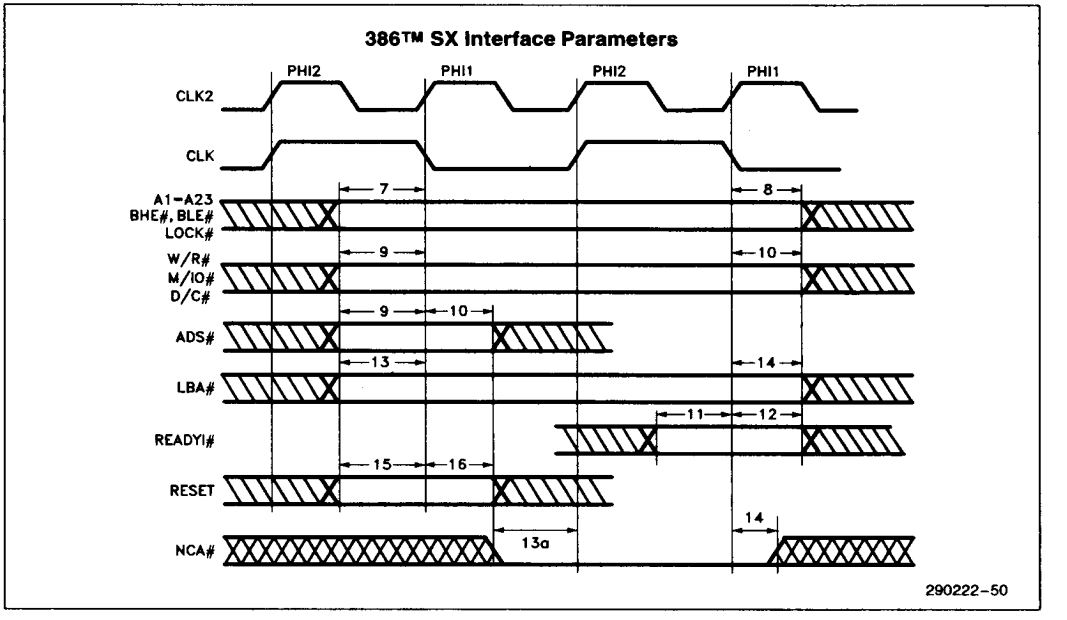
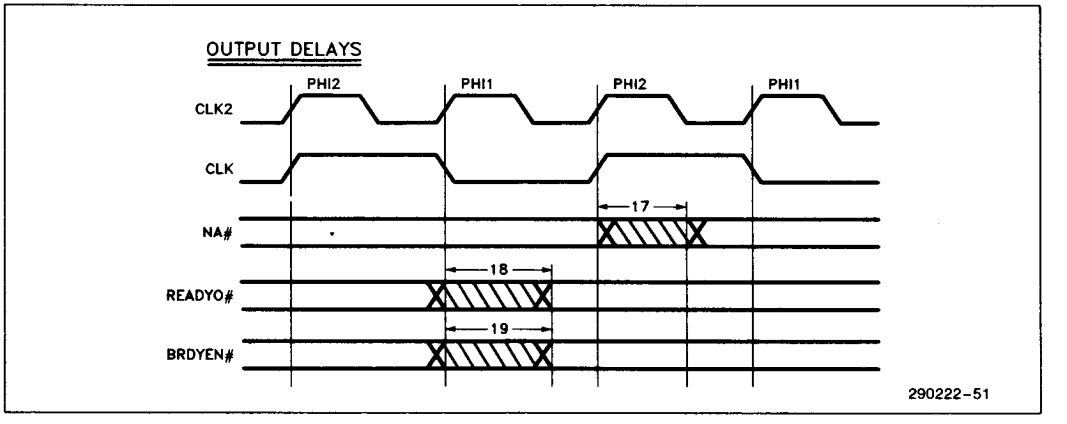
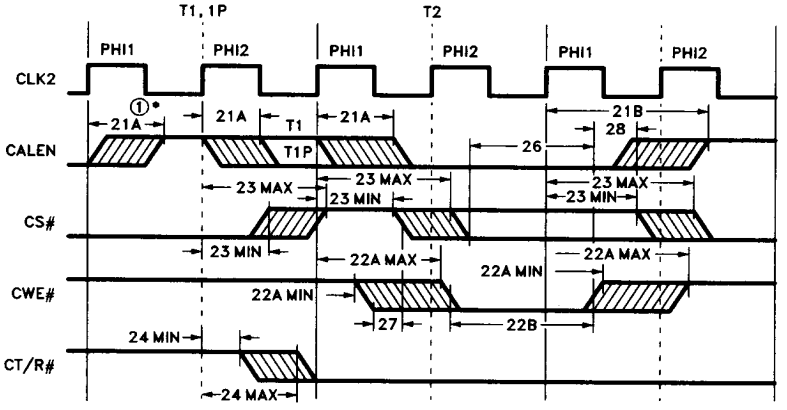


Figure 9-3. A.C. Test Load





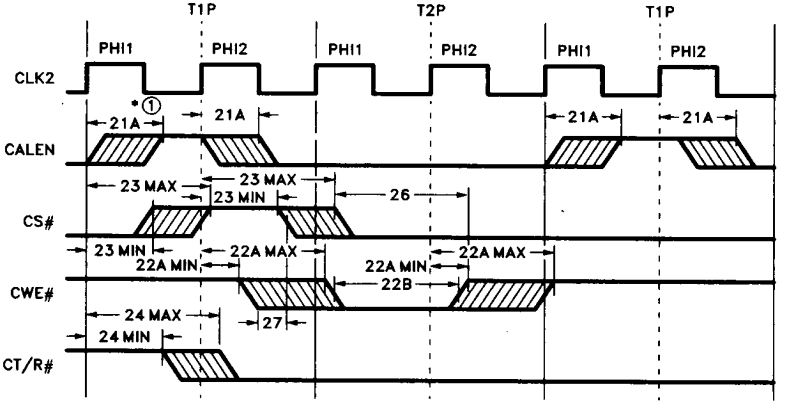
Cache Write Hit Cycle



290222-52

① *. This would be 21B if previous bus cycle was Cache Write Hit cycle.

Cache Read Miss (Cache Update Cycle)

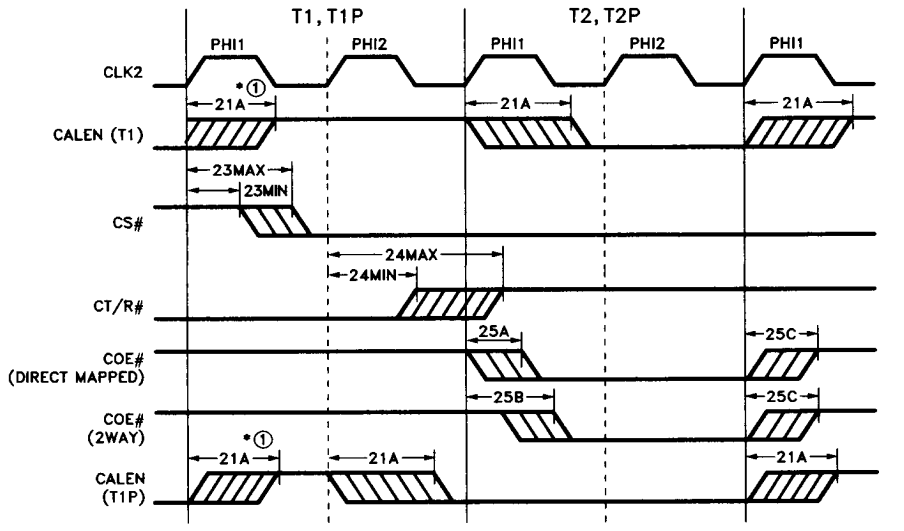


290222-53

① *. This would be 21B if previous bus cycle was Cache Write Hit cycle.

5

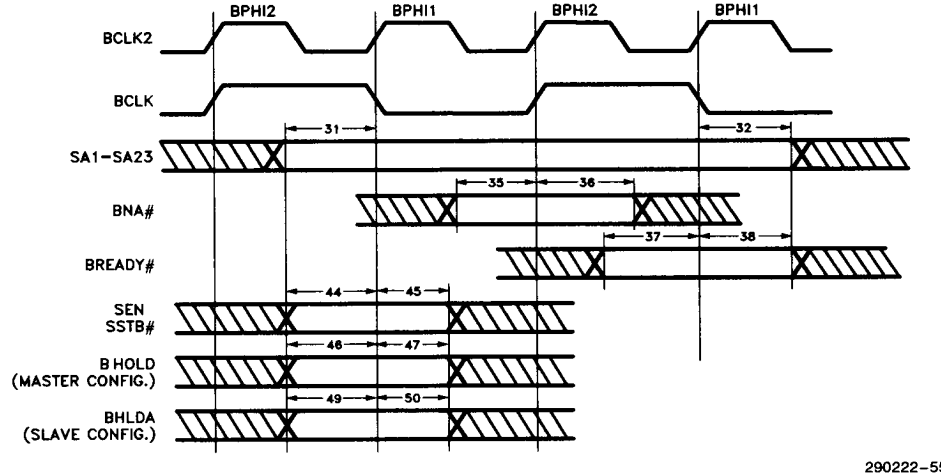
Cache Read Cycle



290222-54

① *. This would be 21B if previous bus cycle was Cache Write Hit cycle.

System Bus Interface Parameters

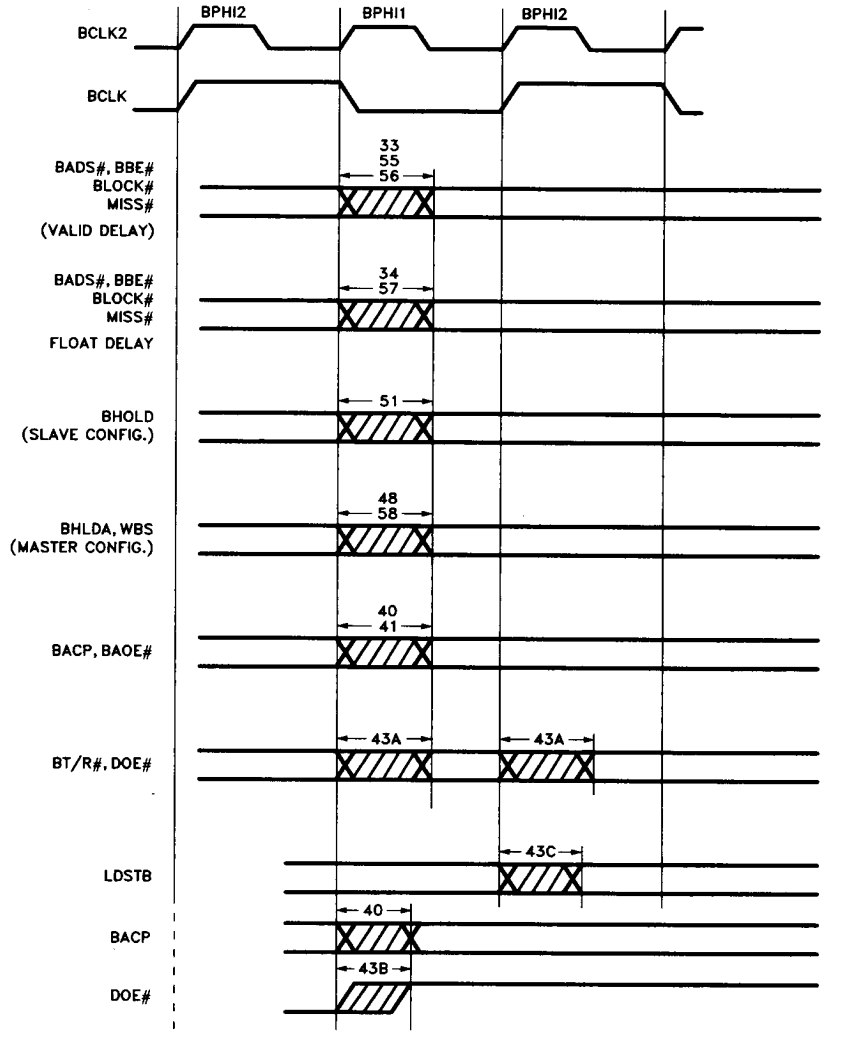


290222-55

① *. This would be 21B if previous bus cycle was Cache Write Hit cycle.

System Bus Interface Parameters (Continued)

OUTPUT DELAYS



290222-56

APPENDIX A

82385SX Signal Summary

Signal Group/Name	Signal Function	Active State	Input/ Output	Tri-State Output?
386 SX INTERFACE				
RESET	386 SX Reset	High	I	—
A1–A23	386 SX Address Bus	High	I	—
BHE#, BLE#	386 SX Byte Enables	Low	I	—
CLK2	386 SX Clock	—	I	—
READYO#	Ready Output	Low	O	No
BRDYEN#	Bus Ready Enable	Low	O	No
READYI#	386 SX Ready Input	Low	I	—
ADS#	386 SX Address Status	Low	I	—
M/IO#	386 SX Memory / I/O Indication	—	I	—
W/R#	386 SX Write/Read Indication	—	I	—
D/C#	386 SX Data/Control Indication	—	I	—
LOCK#	386 SX Lock Indication	Low	I	—
NA#	386 SX Next Address Request	Low	O	No
CACHE CONTROL				
CALEN	Cache Address Latch Enable	High	O	No
CT/R#	Cache Transmit/Receive	—	O	No
CS0#, CS1#	Cache Chip Selects	Low	O	No
COEA#, COEB#	Cache Output Enables	Low	O	No
CWEA#, CWEB#	Cache Write Enables	Low	O	No
LOCAL DECODE				
LBA#	386 SX Local Bus Access	Low	I	—
NCA#	Non-Cacheable Access	Low	I	—
STATUS AND CONTROL				
MISS#	Cache Miss Indication	Low	O	Yes
WBS	Write Buffer Status	High	O	No
FLUSH	Cache Flush	High	I	—

82385SX Signal Summary (Continued)

Signal Group/Name	Signal Function	Active State	Input/ Output	Tri-State Output?
82385SX INTERFACE				
BREADY#	82385SX Ready Input	Low	I	—
BNA#	82385SX Next Address Request	Low	I	—
BLOCK#	82385SX Lock Indication	Low	O	Yes
BADS#	82385SX Address Status	Low	O	Yes
BBHE#, BBLE#	82385SX Byte Enables	Low	O	yes
DATA/ADDR CONTROL				
LDSTB	Local Data Strobe	Pos. Edge	O	No
DOE#	Data Output Enable	Low	O	No
BT/R#	Bus Transmit/Receive	—	O	No
BACP	Bus Address Clock Pulse	Pos. Edge	O	No
BAOE#	Bus Address Output Enable	Low	O	No
CONFIGURATION				
2W/D#	2-Way/Direct Map Select	—	I	—
M/S#	Master/Slave Select	—	I	—
DEFOE#	Define Cache Output Enable	—	I	—
COHERENCY				
SA1–SA23	Snoop Address Bus	High	I	—
SSTB#	Snoop Strobe	Low	I	—
SEN	Snoop Enable	High	I	—
ARBITRATION				
BHOLD	Hold	High	I/O	No
BHLDA	Hold Acknowledge	High	I/O	No

5