82961KA
PAGE PRINTER CONTROLLER

- **High Integration i960® Page Printer Controller(1)**
  - **— Direct Interface to 32-bit 80960KA or KB(2) Embedded Processors**
- **Direct Non-Impact Printer Video Interface**
  - **— Automatic DMA Burst DRAM Access to Transmit Video Image**
  - **— Internal Phase Lock Loop**
  - **— Top and Left Margin, Page Height and Width**
- **Direct Generic Printer Engine Interface to TEC, Canon, Ricoh and Okidata Printer Engines**
- **Programmable ROM/EPROM Interface**
  - **— Direct Interface to Two Banks**
  - **— Expandable to Eight Banks**
  - **— Programmable ROM Size and Wait States**
- **Programmable System Timer**
- **Programmable DRAM Interface**
  - **— Direct Interface to Four Banks**
  - **— Programmable DRAM Size and Wait States**
  - **— Page Mode Cache to Reduce Wait States on First Access**
  - **— Transparent Refresh of DRAM Banks**
  - **— Interfaces to 16- and 32-bit DRAM Systems**
- **Programmable I/O Control**
  - **— Chip-Select, Access Time, Recovery Time**
  - **— Wait State Control for Eight External Devices**
- **Burst Interface Support for i960 KA/KB Bus**
- **Automatic Data Conversion from 16-bit Font Cartridge to 32-bit i960 Embedded Processor Format**
- **Low-Cost 132-Lead Plastic Quad Flat Pack (PQFP)**

Intel's 82961KA page printer controller is the first member of a new family of page printer companion peripherals that address the need for high integration and cost reduction. It is designed to interface Intel's 80960K-series of embedded processors to a variety of non-impact or laser printer mechanisms. The 82961KA controller contains complete DRAM, ROM and I/O controllers, the associated logic required to control virtually all non-impact printer mechanisms, a programmable wait state generator and programmable chip select generation logic. The 82961KA controller—coupled with an 80960Kx plus DRAM, ROM and the appropriate I/O—forms the nucleus for a cost-effective non-impact printer controller.

Designs that employ the 82961KA controller provide substantial system performance improvements. The 82961KA device decouples DRAM and video output subsystems from the synchronous 80960KA/KB bus to achieve increased performance. The 82961KA device's unique programmable video output controller manages virtually every aspect of memory address generation, timing and control once the device begins to produce the video output signal.

1. The 82961KA i960 Page Printer Controller is based on the single-chip controller architecture created by Peerless Systems Corp.
2. Throughout this data sheet, 80960Kx refers to the 80960KA and KB processors.

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82961KA
Page Printer Controller

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TABLES

1.0 PURPOSE

This data sheet describes the 82961KA page printer controller. It provides the information required to begin designing with the 82961KA printer controller. It contains functional and physical descriptions, electrical characteristics and specifications, absolute maximum ratings and package and pin definitions.

2.0 82961KA FUNCTIONAL OVERVIEW

The 82961KA integrates onto a single chip all the "glue" or support logic required in a 80960Kx processor design with a high performance interface to non-impact printers. 82961KA functional blocks are:

- 80960K-Series L-Bus Interface
- ROM Interface
- DRAM Interface
- I/O Interface
- Printer Video Interface
- Printer Communication Interface
- System Timer

The 82961KA is the first member of a new family of page printer companion peripherals. It is intended to operate in the non-impact printer environment. However, many of its features make it extremely well-suited for other applications. The 82961KA provides a direct interface between the Intel 80960Kx microprocessor and system memory, communication channels and printer engine.

The 82961KA is designed for flexibility, ease of use and optimum performance while employing a minimal number of external components. A page printer's host communication environment can range from a simple serial or parallel port to a complete Ethernet implementation. To support this vast range, the 82961KA is not limited to any specific communication mechanism. Instead, the 82961KA generates chip-selects and control signals that allow the user to easily connect standard communication devices to the 80960Kx. Additionally, the 82961KA can be used in other operating environments to enhance Intel 80960Kx microprocessors by providing memory interfaces and peripheral timing controls.

In the most simplistic implementations, the system consists of clock and reset generation, an 80960Kx microprocessor, peripheral communications with interface devices, the 82961KA, ROM devices, DRAM devices with series damping resistors, minimal printer interface logic, along with the usual oscillators, connectors and PC board.

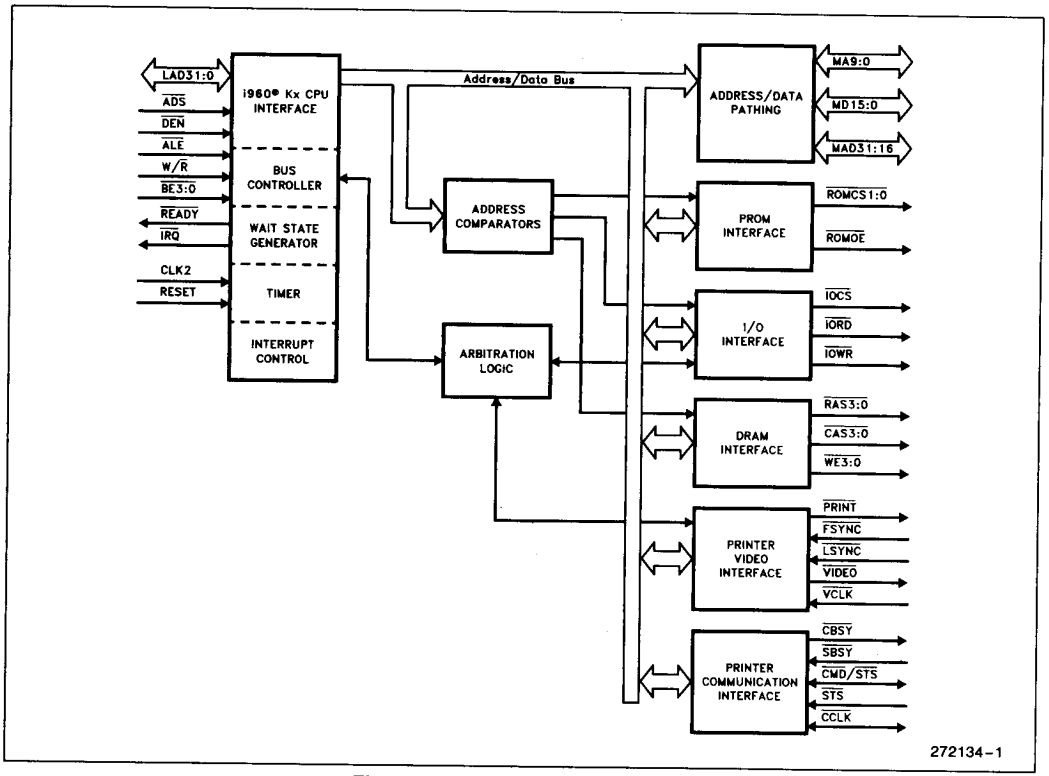

Figure 1. 82961KA Block Diagram

3.0 PACKAGE INFORMATION

3.1 Package Introduction

This section describes the 82961KA pins, pinouts, and thermal characteristics in the 132-pin Plastic Quad Flat Pack (PQFP). For complete package specifications and information, refer to the Intel Packaging Specification (Order No. 231369).

3.2 Pin Descriptions

82961KA pins are described in this section. Table 1 presents the legend for interpreting pin descriptions contained in the following tables. Table 2 defines pins associated with the L-Bus. Tables 3, 4 and 5 define pins associated with memory and I/O interface signals. Table 6 defines pins associated with the printer video interface. Table 7 defines printer communications interface signals. Table 8 defines pins associated with basic processor configuration and control.

Table 1. Pin Description Nomenclature

Symbol(1)	Description
I	Pin is input only
O	Pin is output only
I/O	Pin can be either an input or output
L	Signal is active LOW
L(P)	Signal is active LOW and the signal's sense is programmable
H	Signal is active HIGH
TS	Signal is tristate
OD	Signal is open-drain output
ST	Signal is Schmitt trigger input

NOTE:
1. **Bold** indicates a pin; non-bold indicates a signal.

Table 2. L-Bus Interface Signals

Name	Type	Description
LAD31:0	**I/O** H TS	**LOCAL ADDRESS/DATA BUS** carries 32-bit physical address and data to and from memory, I/O devices or internal registers. During an address cycle, bits 31:2 contain a physical word address and bits 1:0 contain a burst size. During a data cycle, bits 31:0 contain read or write data. Burst size is an encoded number where 00 represents one word and 11 represents four words.
$\overline{\text{ALE}}$	**I** L	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. $\overline{\text{ALE}}$ is asserted during an address cycle and deasserted before a data cycle begins.
$\overline{\text{ADS}}$	**I** L	**ADDRESS/DATA STATUS** indicates an address state. It is asserted during an address cycle and deasserted during a following data cycle. For a burst transaction, $\overline{\text{ADS}}$ is asserted again every data cycle where $\overline{\text{READY}}$ was asserted in the previous cycle.
W/$\overline{\text{R}}$	**I**	**WRITE/$\overline{\text{READ}}$** specifies, during an address cycle, whether the operation is a write or a read. Valid during entire memory, register or I/O operation.
$\overline{\text{DEN}}$	**I** L	**DATA ENABLE** indicates a transfer on the LAD lines. Asserted during all data cycles.
$\overline{\text{READY}}$	**O** OD	**$\overline{\text{READY}}$** indicates data on the LAD signals can be sampled or removed. If $\overline{\text{READY}}$ is not asserted during a data transfer, the data cycle is extended to next cycle by inserting a wait state and $\overline{\text{ADS}}$ is not asserted in the next cycle.
$\overline{\text{BE3:0}}$	**I** L	**BYTE ENABLE:** $\overline{\text{BE}}$ signals specify data bytes on the bus which take part in the current data cycle. $\overline{\text{BE0}}$ corresponds to LAD7:0. $\overline{\text{BE3}}$ corresponds to LAD31:24. $\overline{\text{BE}}$ signals are pipelined. $\overline{\text{BE}}$ signals corresponding to the first data transfer of a burst are asserted during address cycle. $\overline{\text{BE}}$ signals corresponding to subsequent data transfers of a burst are asserted in the data cycle of the current data transfer.
$\overline{\text{IRQ}}$	**O** L OD	**INTERRUPT REQUEST** indicates an interrupt to the 80960Kx processor. When the 82961KA interrupt is cleared, the signal goes inactive for two bus cycles before it can be reasserted.

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Table 3. Memory Interface Signals

Name	Type	Description
MD15:0	I/O H TS	**MEMORY DATA** signals contain the two least significant data bytes for I/O and DRAM memory operations. MD7:0 contain the least significant byte; MD15:8 contain the second most significant byte. If DRAM is configured as 16 bits wide, or the I/O channel being accessed is packed, MD7:0 also contain the third most significant byte and MD15:8 also contain the most significant byte. During a DRAM write operation, only those bytes with a corresponding write enable signal asserted are driven by the 82961KA.
MAD31:29	I/O H TS	**MEMORY ADDRESS/DATA** signals are multi-purpose depending on the device that is selected: ROM MAD31 is not used. MAD30:39 signals output an encoded address range select and are driven high or low. I/O Signals output an encoded address range selected. DRAM Signals contain data bits 29–31 when DRAM is in 32-bit configuration. When DRAM is in 16-bit configuration, these signals are unused and are floated. During a DRAM write operation, only those bytes with a corresponding write enable signal asserted are driven by the 82961KA.
MAD28:16	I/O H TS	**MEMORY ADDRESS/DATA** signals are multi-purpose depending on the device selected: ROM MAD16 is not used. MAD25:17 output address bits 02–08, 17, 19. MAD28:26 are not used and are driven high or low. I/O Signals output address bits 01–08, 17, 19, 21–23. DRAM Signals contain data bits 16–28 with DRAM in 32-bit configuration. When DRAM is in 16-bit configuration, signals are unused and are floated. During a DRAM write operation, only those bytes with a corresponding write enable signal asserted are driven by the 82961KA.
MA9:0	O H	**MEMORY ADDRESS** signals are multi-purpose depending on the device selected: ROM Signals output address bits 09–16, 18, 20. I/O Signals output address bits 09–16, 18, 20. DRAM Signals output multiplexed address bits 00-09. The number of address bits actually multiplexed on these signals depends on the DRAM bank accessed and the programmed size for that bank. Use MA7:0 for 64 Kbit x 16/32 DRAM; use MA8:0 for 256 Kbit x 16/32 DRAM; use MA9:0 for 1 Mbit x 16/32 DRAM.
$\overline{\text{RAS3:0}}$	O L	**ROW ADDRESS STROBE** signals, used for DRAM accesses, are asserted when MA9:0 signals contain a valid row address. $\overline{\text{RAS0}}$ corresponds to the first DRAM bank; $\overline{\text{RAS3}}$ corresponds to the fourth DRAM bank. In page mode the $\overline{\text{RAS}}$ signal of the accessed bank remains asserted after completion of the memory operation, and is deasserted for a bank when a page miss occurs.
$\overline{\text{CAS3:0}}$	O L	**COLUMN ADDRESS STROBE** signals, used for DRAM accesses, are asserted when MA9:0 signals contain a valid column address. $\overline{\text{CAS0}}$ corresponds to the first DRAM bank; $\overline{\text{CAS3}}$ corresponds to the fourth DRAM bank. Only one of the four $\overline{\text{CAS}}$ signals is asserted during a memory operation.
$\overline{\text{WE3:0}}$	O L	**WRITE ENABLE** signals, used for DRAM accesses, are asserted during write operations. For 32-bit wide DRAM, $\overline{\text{WE0}}$ corresponds to the least significant byte MD7:0 and $\overline{\text{WE3}}$ corresponds to the most significant byte MD31:24. $\overline{\text{WE0}}$ also corresponds to the 80960Kx $\overline{\text{BE0}}$ signals and $\overline{\text{WE3}}$ corresponds to the $\overline{\text{BE3}}$ signal. Only those $\overline{\text{WE}}$ signals with a corresponding asserted $\overline{\text{BE}}$ signal are asserted. For 16-bit wide DRAM, $\overline{\text{WE0}}$ corresponds to both the least significant byte, and the third most significant byte, which uses MD7:0. $\overline{\text{WE1}}$ corresponds to both the second most significant byte and the most significant byte, which uses MD15:8. $\overline{\text{WE0}}$ also corresponds to $\overline{\text{BE0}}$ and $\overline{\text{BE2}}$; $\overline{\text{WE1}}$ corresponds to $\overline{\text{BE1}}$ and $\overline{\text{BE3}}$. For 16-bit wide DRAM, DRAM accesses are performed in two 16-bit accesses; $\overline{\text{WE2}}$ and $\overline{\text{WE3}}$ are unused and are deasserted.

Table 4. ROM Signals

Name	Type	Description
$\overline{\text{ROMCS1:0}}$	I/O L TS	**ROM CHIP SELECT** signals indicate an access to one of the eight ROM banks. $\overline{\text{ROMCS0}}$ is used for ROM banks 0–3; $\overline{\text{ROMCS1}}$ for ROM banks 4–7. While $\overline{\text{ROMCS0}}$ or $\overline{\text{ROMCS1}}$ is asserted, the encoded address range select signals MAD30:29 determine the particular ROM bank to be accessed. MAD30:29 signals are guaranteed to be valid during the entire time that $\overline{\text{ROMCS1:0}}$ is asserted. $\overline{\text{ROMCS0}}$ and $\overline{\text{ROMCS1}}$ are never asserted at the same time. These signals are valid during the entire memory operation. During reset, $\overline{\text{ROMCS0}}$ is used as an input to indicate DRAM bus width. If this pin is low during reset, DRAM is configured as a 16-bit bus. If this pin is high, DRAM is configured as a 32-bit bus. This pin is either pulled up (for a 32-bit bus) or pulled down (for a 16-bit bus) through a 10 KΩ resistor. During reset, $\overline{\text{ROMCS1}}$ is used as an input to clear ROM bank 0 size field to zero, disabling it. This allows external ROM and control circuit at address zero. If pin is low during reset, ROM bank 0 is disabled. If pin is high, ROM bank 0 is enabled as normal. This pin is either pulled up (enabled) or pulled down (disabled) through a 10 KΩ resistor.
$\overline{\text{ROMOE}}$	O L	**ROM OUTPUT ENABLE** corresponds to the $\overline{\text{DEN}}$ signal and is asserted during all data cycles to any of the eight ROM banks.

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Table 5. I/O Interface Signals

Name	Type	Description
$\overline{\text{IOCS}}$	O L	**I/O CHIP SELECT** indicates an access to one of the eight I/O device address ranges in an auto-poll cycle. It is asserted at the beginning of an I/O operation and remains asserted for a programmed duration of I/O device select. While $\overline{\text{IOCS}}$ is asserted, encoded address range select signals MAD31:29 determine the particular I/O channel to be accessed. MAD31:29 signals are guaranteed to be valid during the entire time that $\overline{\text{IOCS}}$ is asserted.
$\overline{\text{IOWR}}$	O L	**I/O WRITE** indicates a write operation to one of the eight I/O device address ranges. It is asserted a programmed duration after $\overline{\text{IOCS}}$ is asserted and remains asserted for a programmed duration. It is asserted for I/O write operations only.
$\overline{\text{IORD}}$	O L	**I/O READ** indicates a read operation to one of the eight I/O device address ranges in an auto-poll cycle. It is asserted a programmed duration after $\overline{\text{IOCS}}$ is asserted and remains asserted for a programmed duration. It is asserted for I/O read operations only.

Table 6. Printer Video Interface Signals

Name	Type	Description
$\overline{\text{PRINT}}$	O L(P)	**PRINT REQUEST** indicates printer engine should begin print operation. $\overline{\text{PRINT}}$ signal is a copy of an internal register bit and follows the programming of this bit. For non-printer applications, signal can be used as a general purpose output.
$\overline{\text{FSYNC}}$	I L(P) ST	**FRAME SYNC** indicates printer engine began to print and medium is positioned at top of page. When signal is asserted, the 82961KA controller begins sampling $\overline{\text{LSYNC}}$ signal.
$\overline{\text{LSYNC}}$	I L(P) ST	**LINE SYNC** indicates printer engine began to move the medium and imaging circuitry is positioned at left page position. Each time this signal is asserted, the 82961KA controller counts down the top margin size or initiates a scanline transfer of video data.

Table 6. Printer Video Interface Signals (Continued)

Name	Type	Description
$\overline{\text{VIDEO}}$	O L(P)	$\overline{\text{VIDEO}}$ is the digital serial video data stream. It is driven after each assertion of $\overline{\text{LSYNC}}$ signal after any top margin size is counted. By default, a high on this signal indicates "white space" and low indicates "black space".
$\overline{\text{VCLK}}$	I L(P)	**VIDEO CLOCK** is the video shift rate clock. If the printer engine supplies a video shift rate clock, it is presented on this pin. If the printer engine does not supply a video shift rate clock, an 8x video shift rate clock must be presented on this pin and the 82961KA must be programmed for phase locked loop operation. In phase locked loop operation, the internal video shift rate clock is locked to $\overline{\text{LSYNC}}$ signal active edge. By default, when programmed for 1x operation the video shift rate clock falling edge shifts a bit of video data.

Table 7. Printer Communications Interface Signals

Name	Type	Description
$\overline{\text{CBSY}}$	O L OD	**COMMAND BUSY** indicates 82961KA has command to transmit to the printer engine. $\overline{\text{CBSY}}$ is asserted when 82961KA's printer command register is written; it remains asserted until all command data is sent.
$\overline{\text{SBSY}}$	I L ST	**STATUS BUSY** indicates the printer engine has status to transmit to the 82961KA. When signal is asserted, 82961KA assembles a printer engine status byte in the 82961KA's printer status register using eight transitions of $\overline{\text{CCLK}}$. Note that $\overline{\text{CCLK}}$ may come from the 82961KA or the printer engine, depending on programmed $\overline{\text{CCLK}}$ mode.
$\overline{\text{CMD}}/\overline{\text{STS}}$	I/O L TS	**COMMAND/STATUS DATA** is programmable to be either command data output to printer engine or bidirectional command/status data to/from the printer. Command data is an 8-bit serial command stream to a printer engine. After $\overline{\text{CBSY}}$ is asserted by writing the 82961KA's printer command register, each command bit is presented on this signal, accompanied by a transition of the $\overline{\text{CCLK}}$ signal.
$\overline{\text{STS}}$	I L ST	**STATUS DATA** is an 8-bit serial status from the printer engine. After $\overline{\text{SBSY}}$ is asserted, the printer engine presents each status bit on this signal with each $\overline{\text{CCLK}}$ transition from the 82961KA controller. $\overline{\text{SBSY}}$ must be deasserted and reasserted to begin a second 8-bit status message.
$\overline{\text{CCLK}}$	I/O L TS	**COMMAND CLOCK** is programmable to be either an input clock from the printer engine or an output clock to the printer engine. It causes the printer engine to assemble an 8-bit command or transmit an 8-bit status one bit at a time with each transition of this signal. Each command bit is shifted on a falling edge of $\overline{\text{CCLK}}$ and each status bit is sampled on a rising edge of $\overline{\text{CCLK}}$.

Table 8. Processor Control Signals

Name	Type	Description
CLK2	I	**SYSTEM CLOCK** provides the fundamental timing for the 82961KA. It is twice the frequency of an 80960Kx address or data cycle.
RESET	I ST	**RESET** clears 82961KA internal logic and initializes all internal registers.
V_{CC}	I	**SYSTEM POWER** connections consist of eight pins; it is strongly recommended that these are connected externally to a V_{CC} board plane.
V_{SS}	I	**SYSTEM GROUND** consists of 10 pins; it is strongly recommended that these are connected externally to a V_{SS} board plane.

3.3 82961KA PQFP Pinout

Tables 9 and 10 list 82961KA pin names and package location. See Section 4, Electrical Specifications for specifications and recommended connections.

Table 9. PQFP Pin Name with Package Location (Signal Order)

L-Bus	
Name	**Location**
LAD31	128
LAD30	129
LAD29	130
LAD28	131
LAD27	132
LAD26	1
LAD25	2
LAD24	4
LAD23	5
LAD22	6
LAD21	7
LAD20	8
LAD19	9
LAD18	11
LAD17	12
LAD16	13
LAD15	15
LAD14	16
LAD13	17
LAD12	18
LAD11	19
LAD10	20
LAD9	21
LAD8	23
LAD7	24
LAD6	25
LAD5	27
LAD4	28
LAD3	29
LAD2	30
LAD1	31
LAD0	32
$\overline{ALE}$	119
$\overline{ADS}$	118
W/$\overline{R}$	120

L-Bus (Continued)	
Name	**Location**
$\overline{DEN}$	117
$\overline{READY}$	126
$\overline{BE3}$	121
$\overline{BE2}$	122
$\overline{BE1}$	123
$\overline{BE0}$	124
$\overline{IRQ}$	125

I/O	
Name	**Location**
$\overline{IOCS}$	96
$\overline{IOWR}$	97
$\overline{IORD}$	98

Printer Video	
Name	**Location**
$\overline{VIDEO}$	109
$\overline{PRINT}$	110
$\overline{VCLK}$	111
$\overline{LSYNC}$	112
$\overline{FSYNC}$	113

Printer Comm	
Name	**Location**
$\overline{STS}$	102
$\overline{SBSY}$	104
$\overline{CCLK}$	105
$\overline{CMD/STS}$	107
$\overline{CBSY}$	108

Memory	
Name	**Location**
$\overline{CAS0}$	46
MD0	47
MD1	48
MD2	50

Memory (Continued)	
Name	**Location**
MD3	51
MD4	52
MD5	53
MD6	54
MD7	56
MD8	57
MD9	59
MD10	60
MD11	61
MD12	62
MD13	63
MD14	64
MD15	65
MA0	66
MA1	67
MA2	68
MA3	69
MA4	70
MA5	71
MA6	73
MA7	74
MA8	75
MA9	76
MAD16	77
MAD17	78
MAD18	80
MAD19	81
MAD20	82
MAD21	84
MAD22	85
MAD23	86
MAD24	88
MAD25	89
MAD26	90
MAD27	91

Memory (Continued)	
Name	**Location**
MAD28	92
MAD29	93
MAD30	94
MAD31	95

DRAM	
Name	**Location**
$\overline{WE3}$	33
$\overline{WE2}$	34
$\overline{WE1}$	35
$\overline{WE0}$	36
$\overline{RAS3}$	37
$\overline{CAS3}$	38
$\overline{RAS2}$	40
$\overline{CAS2}$	41
$\overline{RAS1}$	43
$\overline{CAS1}$	44
$\overline{RAS0}$	45

ROM	
Name	**Location**
$\overline{ROMOE}$	99
$\overline{ROMCS1}$	100
$\overline{ROMCS0}$	101

Control	
Name	**Location**
CLK2	114
RESET	116

V_{CC}
14, 26, 49, 58, 72, 103, 115, 127

V_{SS}
3, 10, 22, 39, 42, 55, 79, 83, 87, 106

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Table 10. PQFP Pin Name with Package Location (Pin Order)

Pin	Signal
1	LAD26
2	LAD25
3	V_{SS}
4	LAD24
5	LAD23
6	LAD22
7	LAD21
8	LAD20
9	LAD19
10	V_{SS}
11	LAD18
12	LAD17
13	LAD16
14	V_{CC}
15	LAD15
16	LAD14
17	LAD13
18	LAD12
19	LAD11
20	LAD10
21	LAD9
22	V_{SS}
23	LAD8
24	LAD7
25	LAD6
26	V_{CC}
27	LAD5
28	LAD4
29	LAD3
30	LAD2
31	LAD1
32	LAD0
33	$\overline{WE3}$

Pin	Signal
34	$\overline{WE2}$
35	$\overline{WE1}$
36	$\overline{WE0}$
37	$\overline{RAS3}$
38	$\overline{CAS3}$
39	V_{SS}
40	$\overline{RAS2}$
41	$\overline{CAS2}$
42	V_{SS}
43	$\overline{RAS1}$
44	$\overline{CAS1}$
45	$\overline{RAS0}$
46	$\overline{CAS0}$
47	MD0
48	MD1
49	V_{CC}
50	MD2
51	MD3
52	MD4
53	MD5
54	MD6
55	V_{SS}
56	MD7
57	MD8
58	V_{CC}
59	MD9
60	MD10
61	MD11
62	MD12
63	MD13
64	MD14
65	MD15
66	MA0

Pin	Signal
67	MA1
68	MA2
69	MA3
70	MA4
71	MA5
72	V_{CC}
73	MA6
74	MA7
75	MA8
76	MA9
77	MAD16
78	MAD17
79	V_{SS}
80	MAD18
81	MAD19
82	MAD20
83	V_{SS}
84	MAD21
85	MAD22
86	MAD23
87	V_{SS}
88	MAD24
89	MAD25
90	MAD26
91	MAD27
92	MAD28
93	MAD29
94	MAD30
95	MAD31
96	$\overline{IOCS}$
97	$\overline{IOWR}$
98	$\overline{IORD}$
99	$\overline{ROMOE}$

Pin	Signal
100	$\overline{ROMCS1}$
101	$\overline{ROMCS0}$
102	$\overline{STS}$
103	V_{CC}
104	$\overline{SBSY}$
105	$\overline{CCLK}$
106	V_{SS}
107	$\overline{CMD/STS}$
108	$\overline{CBSY}$
109	$\overline{VIDEO}$
110	$\overline{PRINT}$
111	$\overline{VCLK}$
112	$\overline{LSYNC}$
113	$\overline{FSYNC}$
114	CLK2
115	V_{CC}
116	RESET
117	$\overline{DEN}$
118	$\overline{ADS}$
119	$\overline{ALE}$
120	W/$\overline{R}$
121	$\overline{BE3}$
122	$\overline{BE2}$
123	$\overline{BE1}$
124	$\overline{BE0}$
125	$\overline{IRQ}$
126	$\overline{READY}$
127	V_{CC}
128	LAD31
129	LAD30
130	LAD29
131	LAD28
132	LAD27

3.4 Mechanical Data

Package Dimensions and Mounting

The 82961KA is available in a 132-lead plastic quad flat pack (PQFP). The plastic package uses fine-pitch gull wing leads arranged in a single row along the perimeter of the package with 0.025 inch (0.64 mm) spacing.

The PQFP is normally surface mounted to take best advantage of the plastic package's small footprint and low cost. In some applications, however, designers may prefer to use a socket, either to improve heat dissipation or reduce repair costs.

Pin Assignment

Figures 2 and 3 show the top view of the PQFP; notice that the pins are numbered in order from 1 to 132 around the package's perimeter. Tables 9 and 10 list the function of each pin in the PQFP.

It is strongly recommended that V_{CC} and GND connections be made to multiple V_{CC} and GND pins. Each V_{CC} and GND pin should be connected to the appropriate voltage or ground and externally strapped close to the package. We recommend that you include separate power and ground planes in your circuit board for power distribution.

3.5 Package Thermal Specification

The 82961KA is specified for operation when case temperature is within the range 0°C to +85°C (PQFP). The case temperature should be measured at the top center of the package as shown in Table 11.

The ambient temperature can be calculated from θ_{jc} and θ_{ja} by using the following equations:

$$T_J = T_C + P^*\theta_{jc}$$
$$T_A = T_J - P^*\theta_{ja}$$
$$T_C = T_A + P^*[\theta_{ja} - \theta_{jc}]$$

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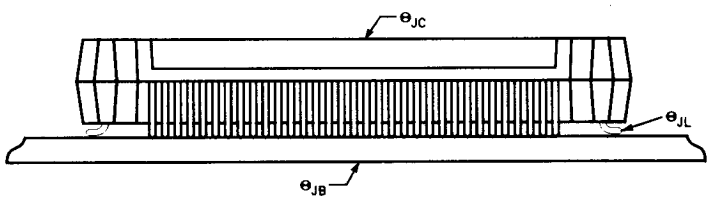
Table 11. 82961KA PQFP Package Thermal Characteristics

PQFP Thermal Resistance—°C/Watt							
Parameter	Airflow—ft./min (m/sec)						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ Junction-to-Case	9	9	9	9	9	9	9
θ Case-to-Ambient (No Heatsink)	22	19	18	16	11	9	8

NOTES:
1. This table applies to 82961KA PQFP soldered directly into board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$.
3. θ_{JL} = 18°C/Watt
   θ_{JB} = 18°C/Watt



272134-36

Values for θ_{ja} and θ_{jc} are given in Table 11 for the PQFP for various airflows. Note that the θ_{ja} for the PGA package can be reduced by adding a heatsink, while a heatsink is not generally used with the plastic package since it is intended to be surface mounted. The maximum allowable ambient temperature (T_A) permitted without exceeding T_C is shown by the charts in Figure 6.

The curves assume the maximum permitted supply current (I_{CC}) at each speed, V_{CC} of 5.0V, and a T_{CASE} of +85°C (PQFP).

3.6 Package Dimensions and Mounting

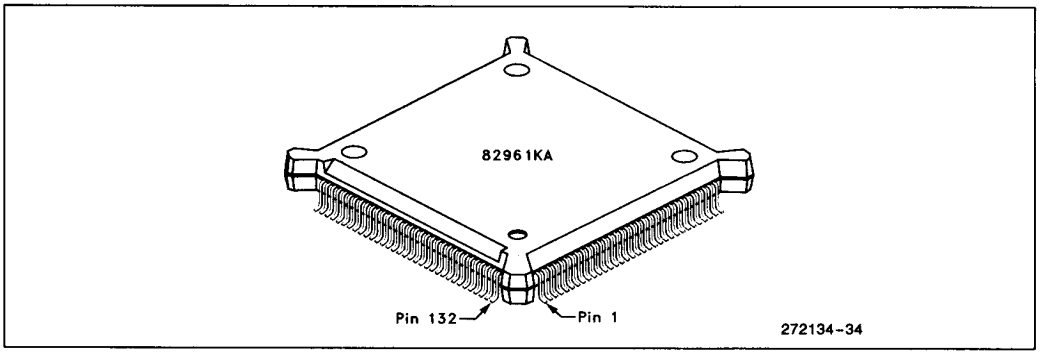


Figure 2. 82961KA 132-Lead Plastic Quad Flat Pack (PQFP) Package

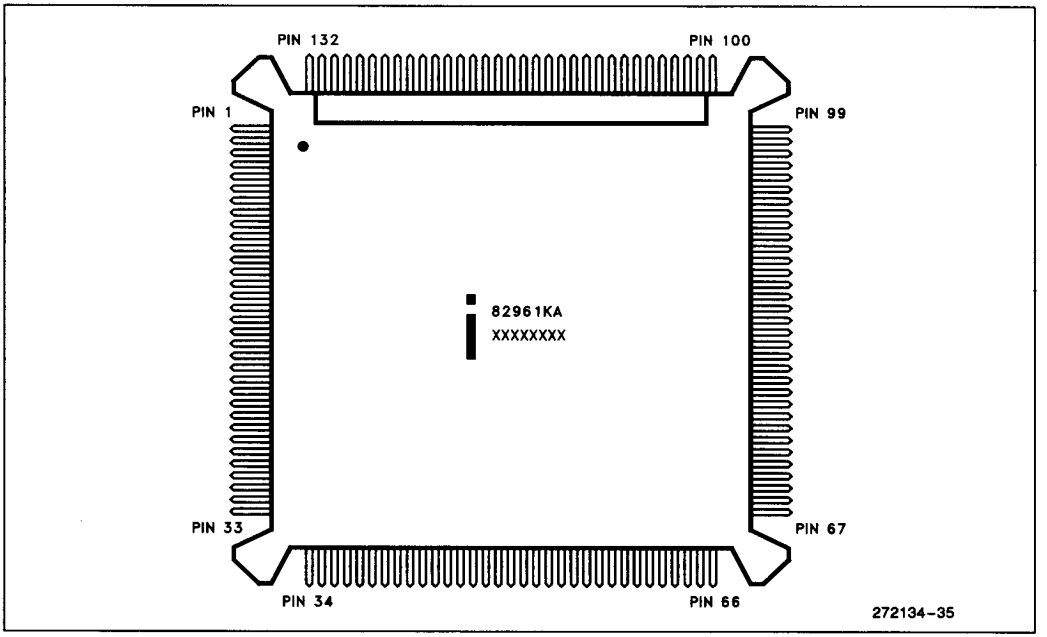


Figure 3. 82961KA PQFP Package (Top View)

4.0 ELECTRICAL SPECIFICATIONS

4.1 Power and Grounding

Power and ground capacitors must be made to all 82961KA power and ground pins. On the circuit board, all V_{CC} pins must be strapped closely together. Similarly, all V_{SS} pins should be strapped closely together. It is strongly recommended that V_{CC} pins are connected to a common power plane and V_{SS} pins are connected to a common ground plane in the PC board.

4.2 Power Decoupling Recommendations

Decoupling capacitors should be placed near the 82961KA. The 82961KA can cause transient power surges when multiple, loaded outputs switch simultaneously. Proper power decoupling is required to avoid "ground lift" or "ground bounce" induced by these power surges.

4.3 Connection Recommendations

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the PC board traces between the processor and decoupling capacitors as much as possible.

For reliable operation, always connect unused inputs to an appropriate signal level. **No unused input pin should be left floating.** Connect unused pins directly to V_{SS} or to V_{CC} through a pull-up resistor. Recommended value of the pull-up resistor is approximately 20 KΩ for each pin tied high.

Output drivers for $\overline{RAS3:0}$, $\overline{CAS3:0}$, $\overline{WE3:0}$ and MA9:0 are designed to directly drive the heavy capacitive loads of DRAM arrays. To prevent outputs from ringing in the system, it is necessary to match the output driver's output impedance to that of the DRAM array. This is accomplished by placing a resistor in series with each signal. Place the series resistor near the 82961KA. Resistor value is dependent on DRAM loading and is best determined by experimentation at the prototype level.

All open-drain outputs require a pull-up termination connected to the output pin. Signals $\overline{READY}$, $\overline{IRQ}$ and $\overline{CBSY}$ are open-drain outputs on the 82961KA.

While in most cases a simple pull-up resistor is adequate, a network consisting of pull-up and pull-down resistors may be necessary for the $\overline{READY}$ pin, since timing on this signal is critical.

Figure 4 shows recommendations for low and high current drive network which assumes the circuit board has a characteristic impedance of 100Ω. The resistor network should bias the output to a valid HIGH level ($V_{IH} \geq 2.0V$). To minimize signal reflection, termination should be placed close to the end of the PC board trace. Pull-up and pull-down resistor value should be chosen such that network impedance closely matches the characteristic impedance of the PC board trace.

Figure 4 also shows a simple pull-up termination which can be used to terminate the open-drain outputs.

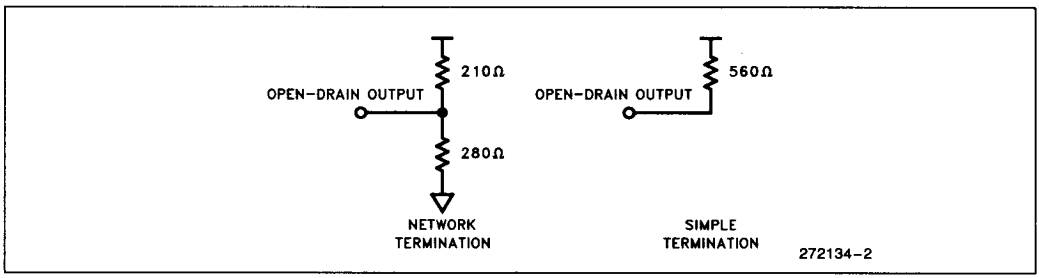


Figure 4. Network and Simple Termination Examples

5.0 ABSOLUTE MAXIMUM RATINGS

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 12. Absolute Ratings

KU82961KA-20, -16 (20, 16 MHz Specification)				
Parameter/Description	**Absolute Ratings**			
	Min	**Max**	**Units**	**Conditions**
Storage Temperature	−65	150	°C	
Case Temperature Under Bias	−65	110	°C	
Supply Voltage with Respect to V_{SS}	−0.5	6.5	V	
Voltage on Other Pins with Respect to V_{SS}	−0.5	V_{CC} + 0.5	V	

Table 13. Targeted Operating Conditions

KU82961KA-20, -16 (20, 16 MHz Specification)					
Symbol	**Parameter/Description**	**Min**	**Max**	**Units**	**Conditions**
V_{CC}	Supply Voltage				
	KU82961KA-20	4.75	5.25	V	(Note 1)
	KU82961KA-16	4.5	5.5		(Note 2)
f_C	Input Clock (CLK2) Frequency				
	KU82961KA-20	1	40	MHz	(Note 1)
	KU82961KA-16	1	32		(Note 2)
T_C	Case Temperature Under Bias				
	KU82961KA-20	0	85	°C	(Note 1)
	KU82961KA-16	0	85		(Note 2)

NOTES:
1. 82961KA-20 is tested with voltage supplies set to ±5%.
2. 82961KA-16 is tested with voltage supplies set to ±10%.

6.0 TARGETED DC CHARACTERISTICS

Table 14. Targeted DC Characteristics

82961KA-20, -16 (20, 16 MHz Specification)					
Symbol	**Parameter/Description**	**Min**	**Max**	**Units**	**Conditions**
V_{IL}	Input Low Voltage	−0.3	0.8	V	(Note 1)
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	(Note 1)
V_{OL}	Output Low Voltage		0.45	V	(Note 2)
V_{OH}	Output High Voltage	2.4		V	(Note 3)
I_{CC}	Power Supply Current 82961KA-20 82961KA-16		 250 200	 mA mA	(Note 4)
I_{LI}	Input Leakage Current		±10	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45 \le V_O \le V_{CC}$
C_{IN}	Input Capacitance		8	pF	f_C = 1 MHz(5)
C_{IO}	I/O or Output Capacitance		10	pF	f_C = 1 MHz(5)

NOTES:
1. RESET, $\overline{\text{FSYNC}}$, $\overline{\text{LSYNC}}$, $\overline{\text{SBSY}}$, and $\overline{\text{STS}}$ are Schmitt trigger inputs. Hysteresis on these pins is approximately 200 mV, but is not tested for each device.
2. V_{OL} is measured under the following conditions:
   I_{OL} = 6 mA — LAD31:0, MAD31:16, MD15:0, $\overline{\text{IOCS}}$, $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{ROMOE}}$, $\overline{\text{ROMCS1:0}}$, $\overline{\text{RAS3:0}}$, $\overline{\text{CAS3:0}}$, $\overline{\text{WE3:0}}$, MA9:0
   I_{OL} = 12 mA — $\overline{\text{CCLK}}$, $\overline{\text{CMD/STS}}$, $\overline{\text{CBSY}}$, $\overline{\text{VIDEO}}$, $\overline{\text{PRINT}}$
   I_{OL} = 24 mA — $\overline{\text{READY}}$, $\overline{\text{IRQ}}$
3. V_{OH} is measured under the following conditions:
   I_{OH} = 6 mA — LAD31:0, MAD31:16, MD15:0, $\overline{\text{IOCS}}$, $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{ROMOE}}$, $\overline{\text{ROMCS1:0}}$, $\overline{\text{RAS3:0}}$, $\overline{\text{CAS3:0}}$, $\overline{\text{WE3:0}}$, MA9:0
   I_{OH} = 12 mA — $\overline{\text{CCLK}}$, $\overline{\text{CMD/STS}}$, $\overline{\text{VIDEO}}$, $\overline{\text{PRINT}}$
   V_{OH} is not measured for open-drain outputs, $\overline{\text{IRQ}}$, $\overline{\text{READY}}$, and $\overline{\text{CBSY}}$
4. Measured at worst case frequency, V_{CC}, and temperature, with device operating and outputs loaded to the test conditions shown in Figure 5.
5. Capacitance values are not tested.

3

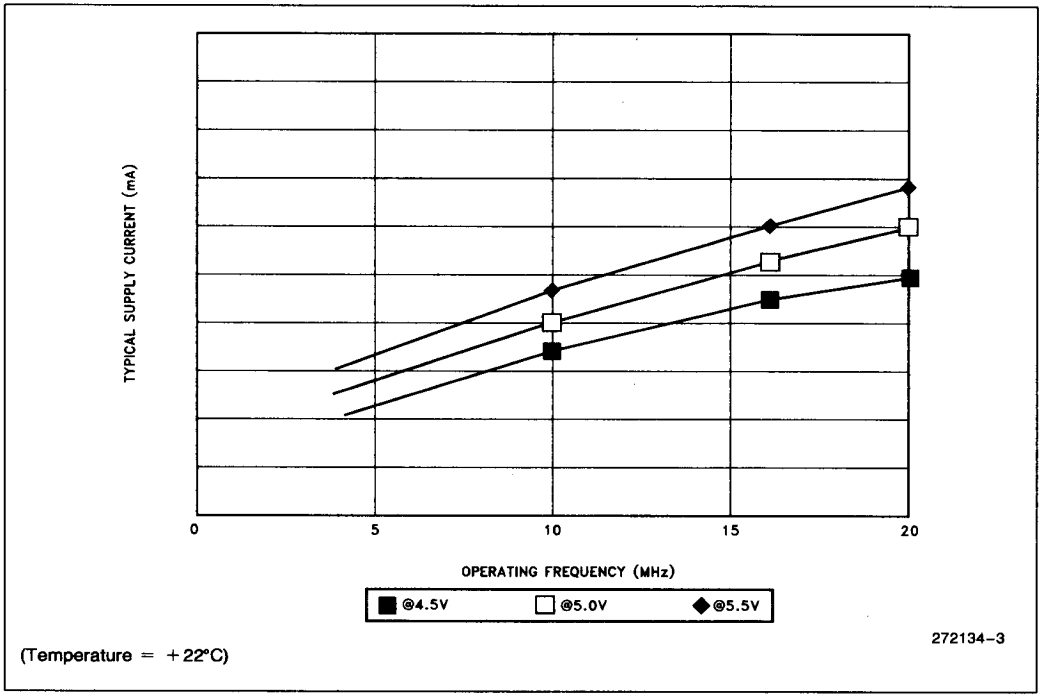


Figure 5. Typical Supply Current (I_{CC}) vs Frequency (f_C)

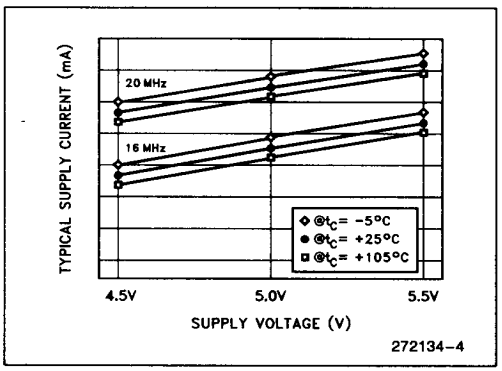


Figure 6. Typical Supply Current (I_{CC}) vs Supply Voltage (V_{CC})

7.0 TARGETED AC CHARACTERISTICS

AC Specifications presented in this document are tested with loading on output pins as shown in Figure 7. Output test load (C_L) is never less than 50 pF unless specifically stated in the AC Specifications.

Figure 8 shows output valid delay as a function of load capacitance. Output valid delays given in the AC Specifications must be adjusted using data in Figure 8 when pin loading in the system exceeds test load, C_L. Derating information is verified at all operating conditions using a sampling of components which represent process extremes. Derating information is not tested for each device.

AC Specifications relating to outputs are measured at the 1.5V crossing point of the output signal unless otherwise indicated. Input signals are driven during test with a rise and fall time of ≤ 2 ns. AC Specifications relating to inputs are measured from the 1.5V crossing point of the input waveform.

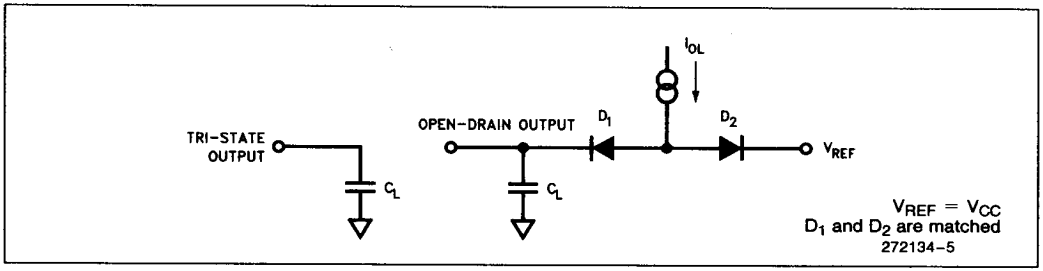
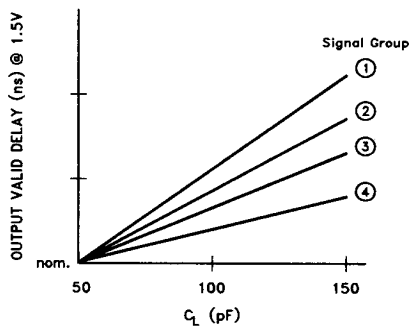


Figure 7. AC Test Loads



GROUP ① LAD31:0, MD15:0, MAD31:16, $\overline{IOWR}$, $\overline{IORD}$, $\overline{IOCS}$, $\overline{ROMOE}$, $\overline{ROMCS1:0}$
GROUP ② $\overline{CBSY}$, $\overline{CMD/STS}$, CCLK, $\overline{VIDEO}$, $\overline{PRINT}$
GROUP ③ MA9:0, $\overline{RAS3:0}$, $\overline{CAS3:0}$, $\overline{WE3:0}$
GROUP ④ $\overline{READY}$, $\overline{IRQ}$

Figure 8. Output Valid Delay (t_{OV}) vs Load Capacitance

3

Table 15. Input Clock Specifications

Symbol	Parameter/Description	Min	Max	Units	Conditions
82961KA-20 (20 MHz Specification)					
f_C	CLK2 Frequency	1	40	MHz	(Note 1)
t_C	CLK2 Period	25	1000	ns	(Note 1)
t_{CH}	CLK2 High Time	10		ns	(Note 1)
t_{CL}	CLK2 Low Time	10		ns	(Note 1)
t_{CR}	CLK2 Rise Time		6	ns	(Note 1)
t_{CF}	CLK2 Fall Time		6	ns	(Note 1)
82961KA-16 (16 MHz Specification)					
f_C	CLK2 Frequency	1	32	MHz	(Note 1)
t_C	CLK2 Period	31.25	1000	ns	(Note 1)
t_{CH}	CLK2 High Time	12.5		ns	(Note 1)
t_{CL}	CLK2 Low Time	12.5		ns	(Note 1)
t_{CR}	CLK2 Rise Time		6	ns	(Note 1)
t_{CF}	CLK2 Fall Time		6	ns	(Note 1)

NOTE:
1. See Figure 7 for waveforms and specifications.

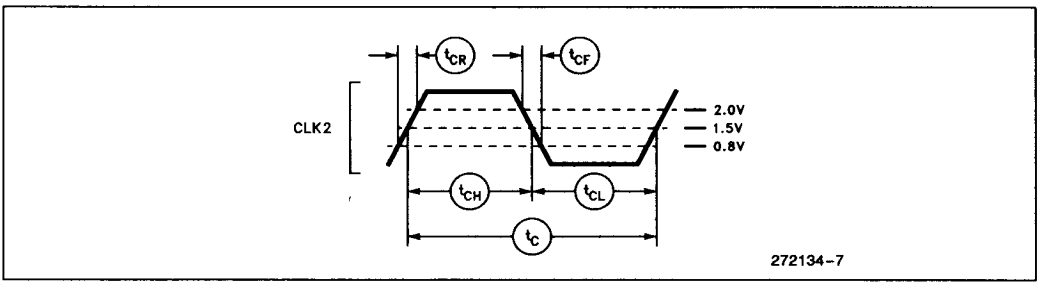


Figure 9. Clock Input Waveforms

Table 16. Synchronous Input and Output Specifications

Symbol	Parameter/Description		Min	Max	Unit	Conditions
82961KA-20 (20 MHz Specification)						
t_{OV} t_{OH}	Output Valid Delay (Maximum Value) Output Hold Delay (Minimum Value)					
	t_{OV1}, t_{OH1}	LAD31:0	5	37	ns	Notes 1, 3, 7
	t_{OV2}, t_{OH2}	LAD31:0 (register read only)	5	59	ns	Notes 1, 2, 7
	t_{OV3}, t_{OH3}	$\overline{IRQ}$	5	37	ns	Notes 1, 2
	t_{OV4}, t_{OH4}	$\overline{READY}$	5	37	ns	Notes 1, 2
	t_{OV5}, t_{OH5}	MD15:0	5	33	ns	Notes 1, 3, 10
	t_{OV6}, t_{OH6}	MAD31:16 (I/O cycles only)	5	34	ns	Notes 1, 3, 9
	t_{OV7}, t_{OH7}	MAD31:16 (ROM cycles only)	5	31	ns	Notes 1, 2, 9
	t_{OV8}, t_{OH8}	MAD31:29 (auto-poll only)	5	37	ns	Notes 1, 6, 9
	t_{OV9}, t_{OH9}	MA9:0	5	32	ns	Notes 1, 4, 8
	t_{OV10}, t_{OH10}	$\overline{RAS3:0}$, $\overline{CAS3:0}$	5	26	ns	Notes 1, 4
	t_{OV11}, t_{OH11}	$\overline{WE3:0}$	5	34	ns	Notes 1, 5
	t_{OV12}, t_{OH12}	$\overline{ROMCS1:0}$, $\overline{ROMOE}$	5	24	ns	Notes 1, 2
	t_{OV13}, t_{OH13}	$\overline{IOCS}$, $\overline{IORD}$, $\overline{IOWR}$	5	27	ns	Notes 1, 3
	t_{OV14}, t_{OH14}	$\overline{IOCS}$, $\overline{IORD}$ (auto-poll only)	5	31	ns	Notes 1, 3
	t_{OV15}, t_{OH15}	$\overline{PRINT}$		28	ns	Notes 1, 2
t_{OF}	Output Float Delay					
	t_{OF1}	MD15:0		33	ns	Notes 1, 11
	t_{OF2}	MAD31:16		37	ns	Notes 1, 11
t_{IS}	Input Setup Time					
	t_{IS1}	$\overline{ADS}$, W/$\overline{R}$, $\overline{BE3:0}$, $\overline{DEN}$	42		ns	Notes 1, 2
	t_{IS2}	LAD31:0	10		ns	Notes 1, 2, 12
	t_{IS3}	MD15:0	8		ns	Notes 1, 3, 13
	t_{IS4}	MAD31:16	8		ns	Notes 1, 3, 14
	t_{IS5}	RESET	0		ns	Notes 1, 3
	t_{IS6}	$\overline{ROMCS1:0}$ (on RESET)	0		ns	Notes 1, 3
t_{IH}	Input Hold Time					
	t_{IH1}	$\overline{ADS}$, W/$\overline{R}$, $\overline{BE3:0}$, $\overline{DEN}$	2		ns	Notes 1, 2
	t_{IH2}	LAD31:0	2		ns	Notes 1, 2, 12
	t_{IH3}	MD15:0	8		ns	Notes 1, 3, 13
	t_{IH4}	MAD31:16	10		ns	Notes 1, 3, 14
	t_{IH5}	RESET	5		ns	Notes 1, 3
	t_{IH6}	$\overline{ROMCS1:0}$ (on RESET)	8		ns	Notes 1, 3
82961KA-16 (16 MHz Specification)						
TBD						

3

NOTES:
1. See Figure 8 for waveforms and specifications.
2. Signal is synchronous to the CLK2 A edge.
3. Signal is synchronous to the CLK2 A or C edge.
4. Signal is synchronous to any rising or falling edge of CLK2 (CLK2 A, B, C or D edge).
5. Signal is synchronous to the CLK2 B edge.
6. Signal is synchronous to the CLK2 C edge.
7. LAD31:0 are synchronous outputs when presenting data for an internal register read, or any I/O read cycle in which rising $\overline{IORD}$ precedes rising $\overline{IOCS}$. LAD15:0 are synchronous outputs for the first half of a packed I/O or DRAM access. For all other accesses, data is driven on LAD31:0 combinatorially, and is described by the t_{MDLD} parameter.
8. MA9:0 signals are synchronous outputs when presenting the DRAM row address when a page miss or a video FIFO read occurs, or when switching from the DRAM row address to the DRAM column address. MA1:0 are synchronous during DRAM burst cycles, and MA7 is synchronous during 16-bit cycles. For all other accesses, MA9:0 are driven combinatorially as described by the t_{LAMA} parameter.
9. MAD31:16 signals are synchronous outputs for all I/O and PROM accesses. For DRAM accesses these signals are driven combinatorially as described by the t_{LDMD} parameter.
10. MD15:0 outputs are synchronous outputs during the second half of a packed I/O or DRAM write access. For all other accesses, data is driven combinatorially as described by the t_{LDMD} parameter.
11. For DRAM write accesses, each byte in the MAD31:16 and MD15:0 bus is enabled only when the corresponding write enable ($\overline{WE3:0}$) signal is active. Bytes in this bus which are not selected are floated to avoid contention on the DRAM data bus. At the end of a DRAM access the data bus (MAD31:16, MD15:0) stays valid until the CLK2 A edge of the T_r state, and float when $\overline{WE3:0}$ are deasserted at the CLK2 B edge of the T_r state.
For I/O and ROM accesses, MAD31:16 signals are enabled in the first T_w state of an access synchronous to the CLK2 A edge. After ROM accesses, MAD31:16 are floated in the T_r state, synchronous to the CLK2 A edge. After I/O accesses, the MAD31:29 signals are floated later on the CLK2 C edge, preventing glitches in external decoding logic. Note for I/O, the MAD28:16 signals are also floated on the CLK2 C edge, but only stay valid until the CLK2 A edge of the T_r state.
12. LAD31:0 are synchronous inputs only for internal register writes.
13. MD15:0 are synchronous inputs on the first half of a packed I/O or DRAM read access, any I/O access in which rising $\overline{IORD}$ precedes rising $\overline{IOCS}$, auto-poll accesses, and when the video FIFO is being filled.
14. MAD31:16 are synchronous inputs only when the video FIFO is being filled.

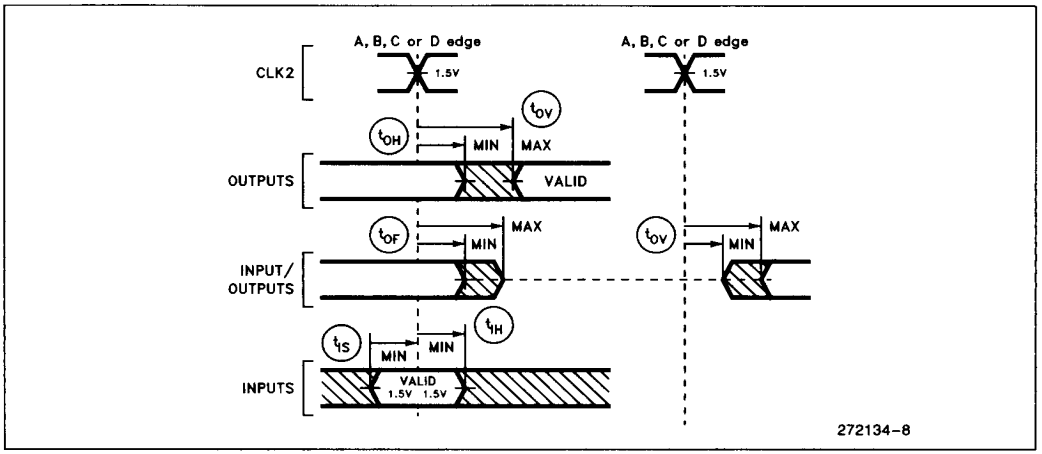


Figure 10. Synchronous Input/Output Waveforms

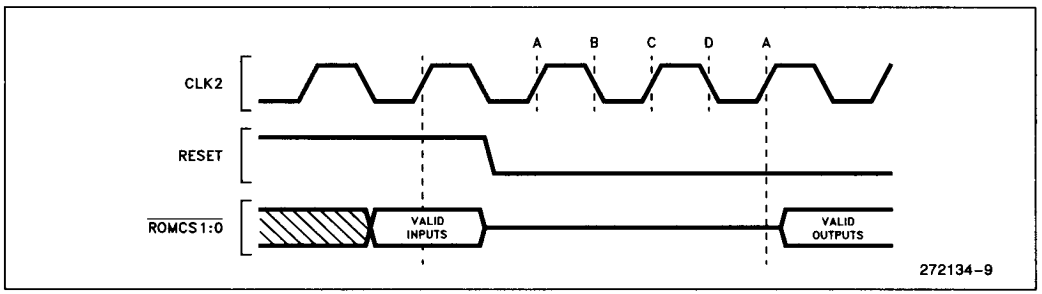


Figure 11. Reset Timing

3

7.1 Targeted L-Bus Timing Specifications

Table 17. L-Bus Relative Timing Specifications

Symbol	Parameter/Description	Min	Max	Units	Conditions
82961KA-20 (20 MHz Specification)					
t_{AVLH}	LAD Address Valid to $\overline{ALE}$ High	5		ns	Note 1
t_{LHAX}	LAD Address Hold from $\overline{ALE}$ High	3		ns	Note 1
t_{LLLH}	$\overline{ALE}$ Low to $\overline{ALE}$ High	10		ns	Note 1
t_{ELQD}	$\overline{DEN}$ Low to LAD Data Bus Driven		28	ns	Note 1
t_{EHQF}	$\overline{DEN}$ High to LAD Data Floating		28	ns	Note 1
t_{LAMA}	Local Address to Memory Address		52	ns	Note 1
t_{LDMD}	Local Data to Memory Data	5	22	ns	Note 1
t_{MDLD}	Memory Data to Local Data	5	22	ns	Note 1
t_{RHRL}	RESET High to RESET Low	41		2x Clocks(2)	Note 1
82961KA-16 (16 MHz Specification)					
TBD					

NOTES:
1. See Figure 10 for waveforms and specifications.
2. A 2x clock cycle is equal to a CLK2 period, t_C.

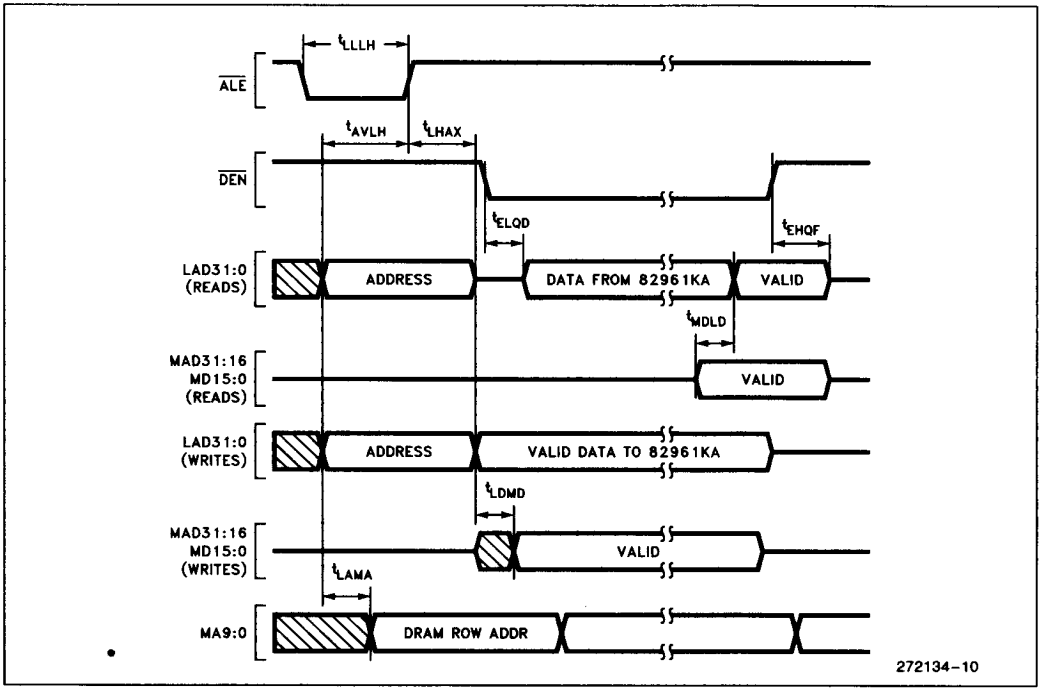


Figure 12. L-Bus Relative Timings

7.2 L-Bus Operational Waveforms

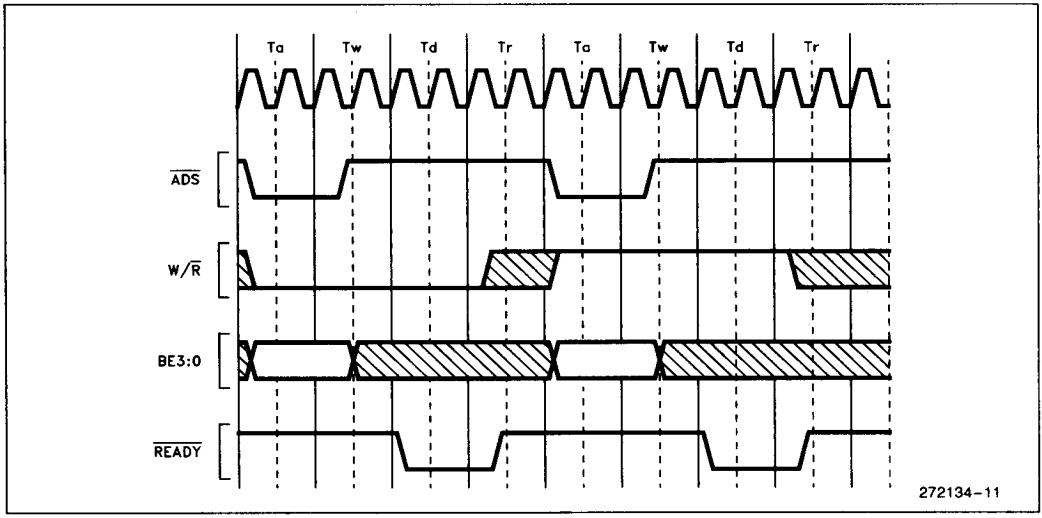


Figure 13. L-Bus Operation

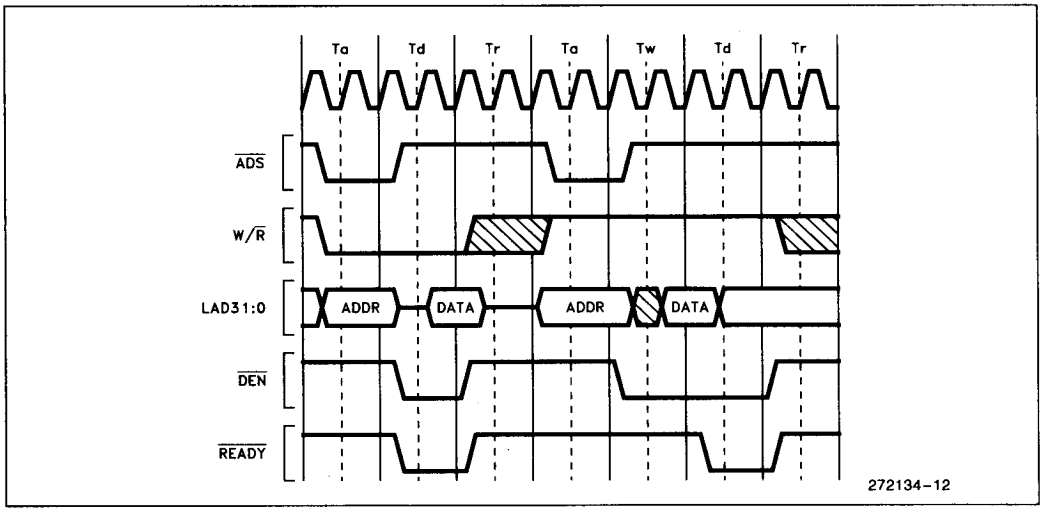


Figure 14. Internal Register Read/Write

7.3 Targeted DRAM Controller Timing Specifications

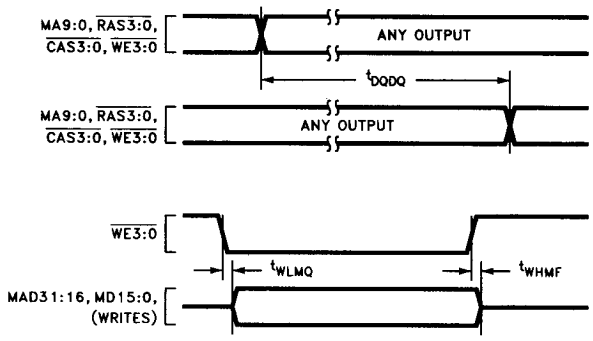
Table 18. DRAM Controller Relative Timings

82961KA-20, -16 (20, 16 MHz Specification)					
Symbol	**Parameter/Description**	**Min**	**Max**	**Units**	**Conditions**
t_{DQDQ}	Output to Output Delay	n4x * (t_C/2) ±4		ns	(Notes 1, 2, 3)
t_{WLMQ}	$\overline{WE3:0}$ Low to Memory: data bus enabled	+4		ns	(Notes 1, 4)
t_{WHMF}	$\overline{WE3:0}$ High to Memory: data bus float	+4		ns	(Notes 1, 4)

NOTES:
1. See Figure 15 for waveforms and specifications.
2. The t_C parameter refers to the CLK2 period. The value for t_C is given in Table 15. n4x is the number of 4x clock cycles between DRAM outputs. The number of 4x clock cycles is selected by programming the DRAM controller.
3. When the value for n4x is an odd number, an error term is required if the CLK2 duty cycle is asymmetric. For example, if CLK2 has a 40%–60% duty cycle, the falling edge varies ±10% from a perfect 50% duty cycle. The error term in this case, which is added to the DRAM timing, is calculated as follows:

$$\text{Error} = \pm(0.10)\ (t_C)$$

4. For non-aligned DRAM writes, each byte in the transfer is enabled and disabled onto the MAD31:16 and MD15:0 data bus by the corresponding $\overline{WE}$. This guarantees no contention between the 82961KA and DRAM for bytes not selected for a particular write cycle.



NOTE:
t_{DQDQ} describes delay between signals which are output synchronously to the rising or falling edge of CLK2x.

Figure 15. DRAM Relative Timings

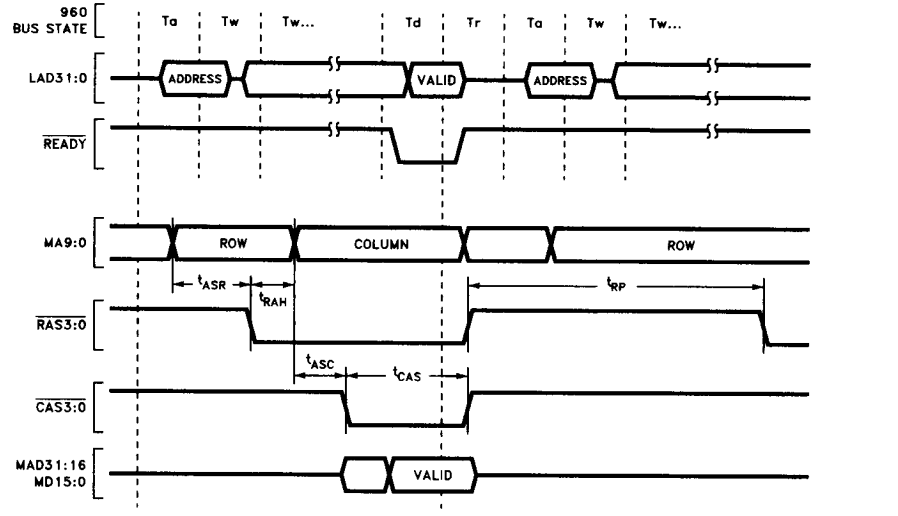
7.4 DRAM Controller Operational Waveforms

The following bus waveforms describe the operation of the DRAM controller on the 82961KA. The DRAM controller provides registers to configure timings and to optimize the DRAM interface to many varieties of DRAM designs (for example, fast-page vs. static column mode DRAMs). The DRAM Operations Waveforms show only the timing parameters which may be adjusted by programming the 82961KA. These parameters are described in Table 19.

Table 19. DRAM Controller Programmable Timings

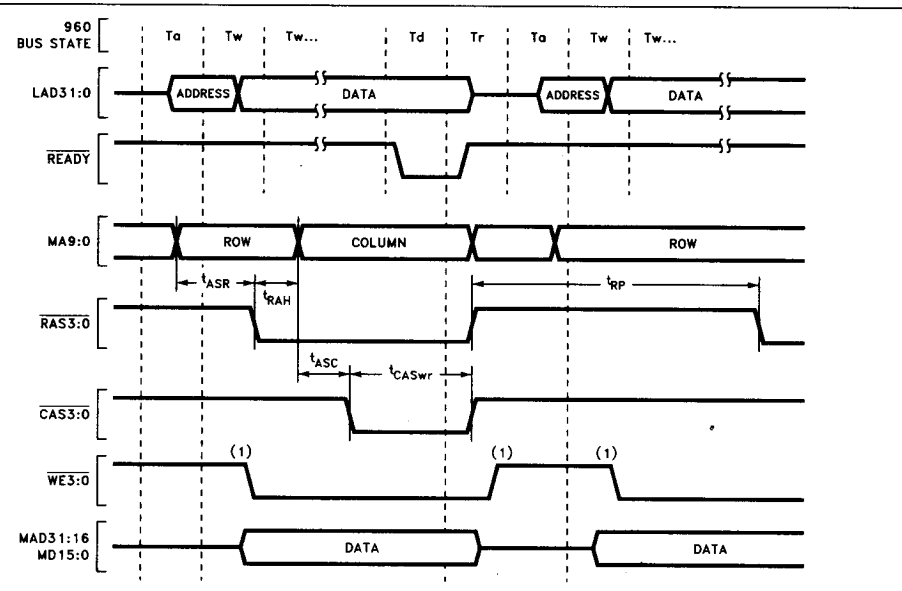
Symbol	Description	Min	Max	Units
t_{ASR}	Row Address Setup to $\overline{RAS3:0}$ Active	2	15	4x Clocks
t_{RAH}	Row Address Hold after $\overline{RAS3:0}$ Active	2	15	4x Clocks
t_{ASC}	Column Address Setup to $\overline{CAS3:0}$ Active	1	15	4x Clocks
t_{CASrd}	$\overline{CAS3:0}$ Pulse Width for Reads	1	15	4x Clocks
t_{CASwr}	$\overline{CAS3:0}$ Pulse Width for Writes	1	15	4x Clocks
t_{CPrd}	$\overline{CAS3:0}$ Precharge for Reads	0	15	4x Clocks
t_{CPwr}	$\overline{CAS3:0}$ Precharge for Writes	2	15	4x Clocks
t_{RP}	$\overline{RAS3:0}$ Precharge	2	15	4x Clocks
t_{RPC}	$\overline{RAS3:0}$ Hold to $\overline{CAS3:0}$ Precharge (Refresh)	0	7	2x Clocks
t_{CSR}	$\overline{CAS3:0}$ Setup Time (Refresh)	0	7	2x Clocks
t_{CHR}	$\overline{CAS3:0}$ Hold Time (Refresh)	0	7	2x Clocks

NOTE:
A 4x clock is equal to 0.5 (t_C), or half the CLK2 period. A 2x clock is equal to t_C, or the CLK2 period. When the value for n4x is an odd number, an error term is required if the CLK2 duty cycle is asymmetric. For example, if CLK2 has a 40%–60% duty cycle, the falling edge varies ±10% from a perfect 50% duty cycle. The error term in this case, which is added to the DRAM timing, is calculated as follows: Error = ±(0.10) (t_C).



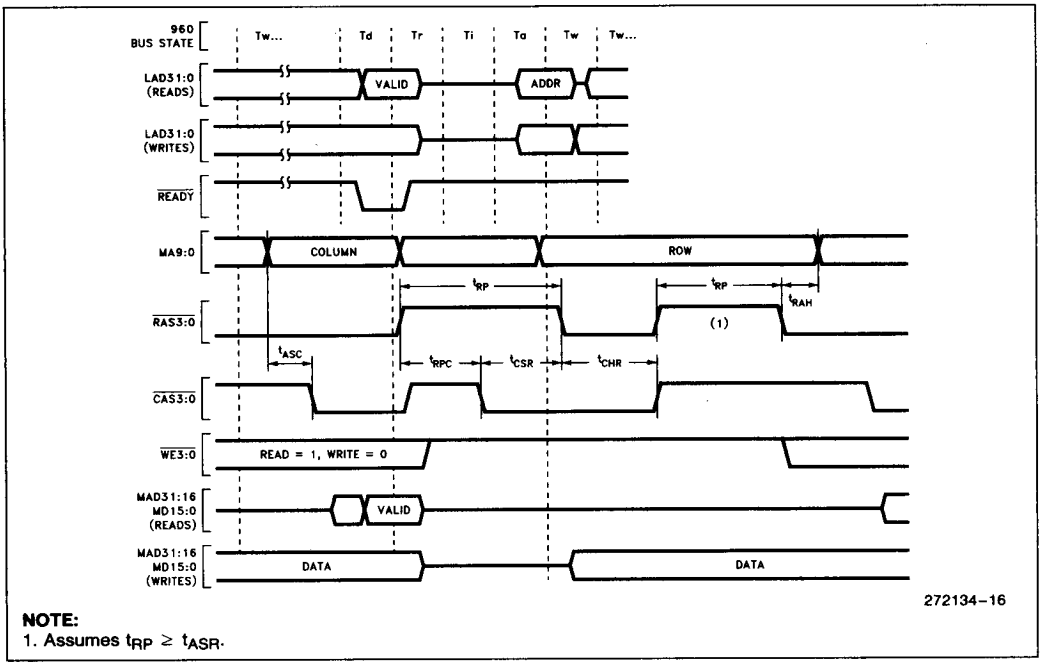
NOTE:
1. $\overline{WE3:0}$ = HIGH

Figure 16. DRAM Non-Page Read Cycle



NOTE:
1. $\overline{WE3:0}$ Synchronous to CLK2 B-edge.

Figure 17. DRAM Non-Page Write Cycle



NOTE:
1. Assumes $t_{RP} \geq t_{ASR}$.

Figure 18. DRAM $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

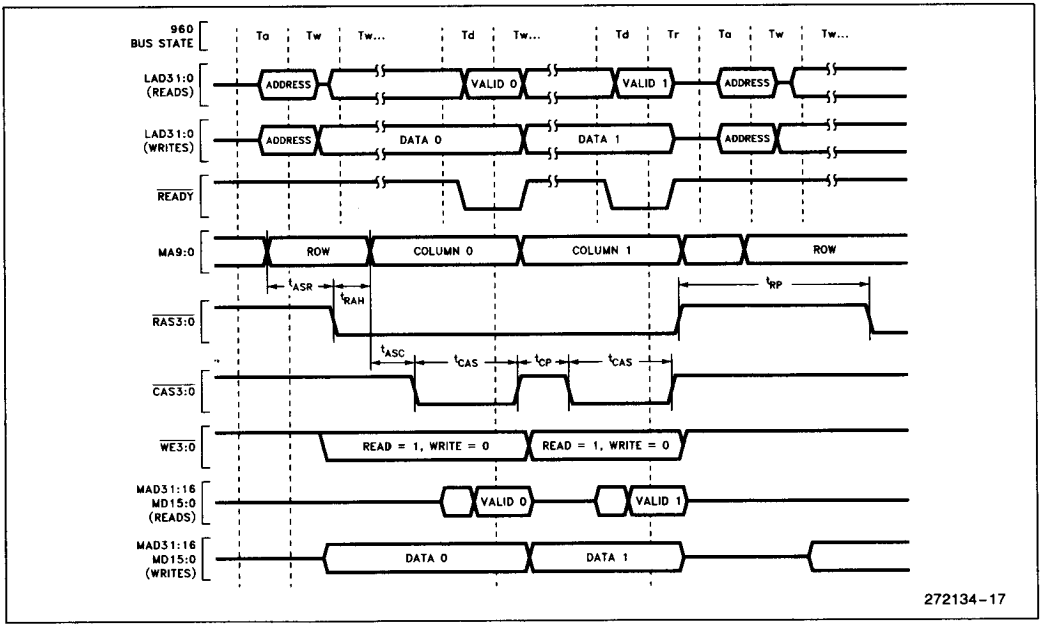


Figure 19. DRAM Page Read/Write

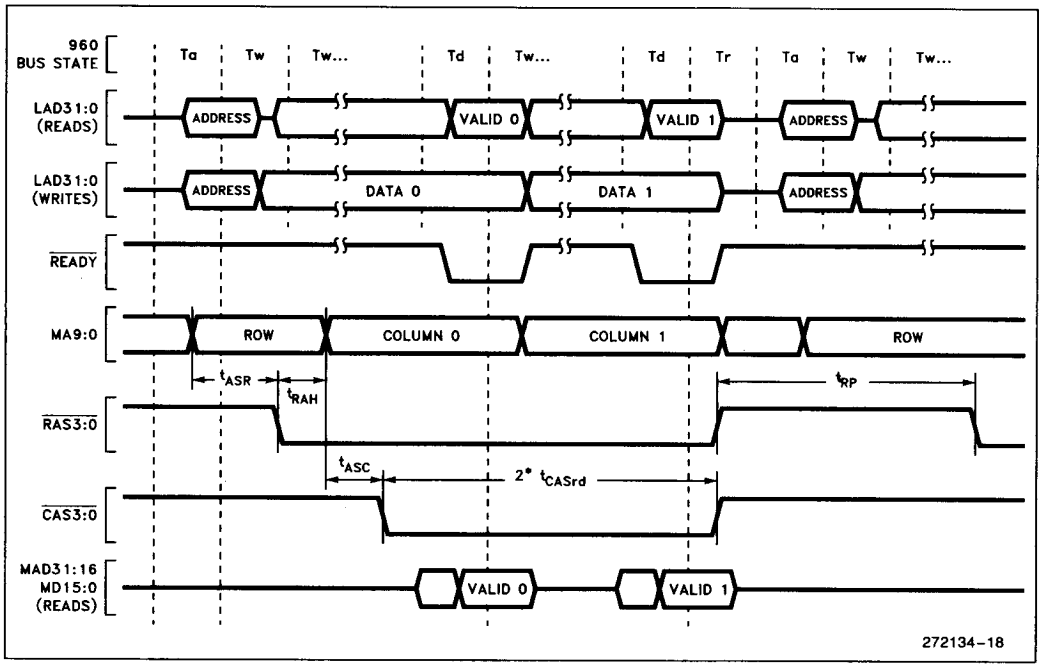
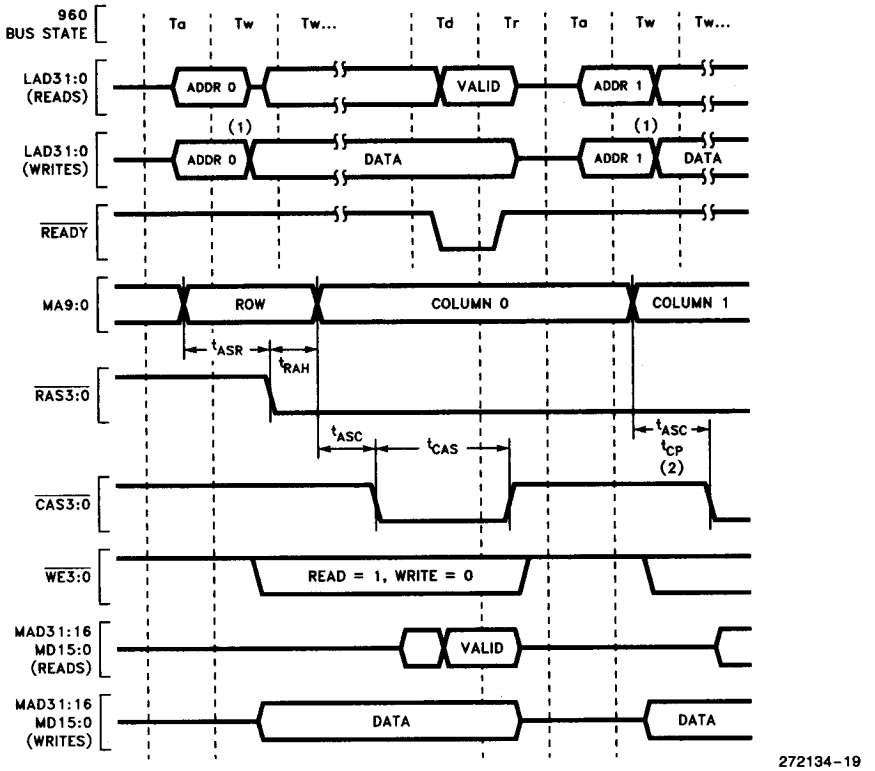


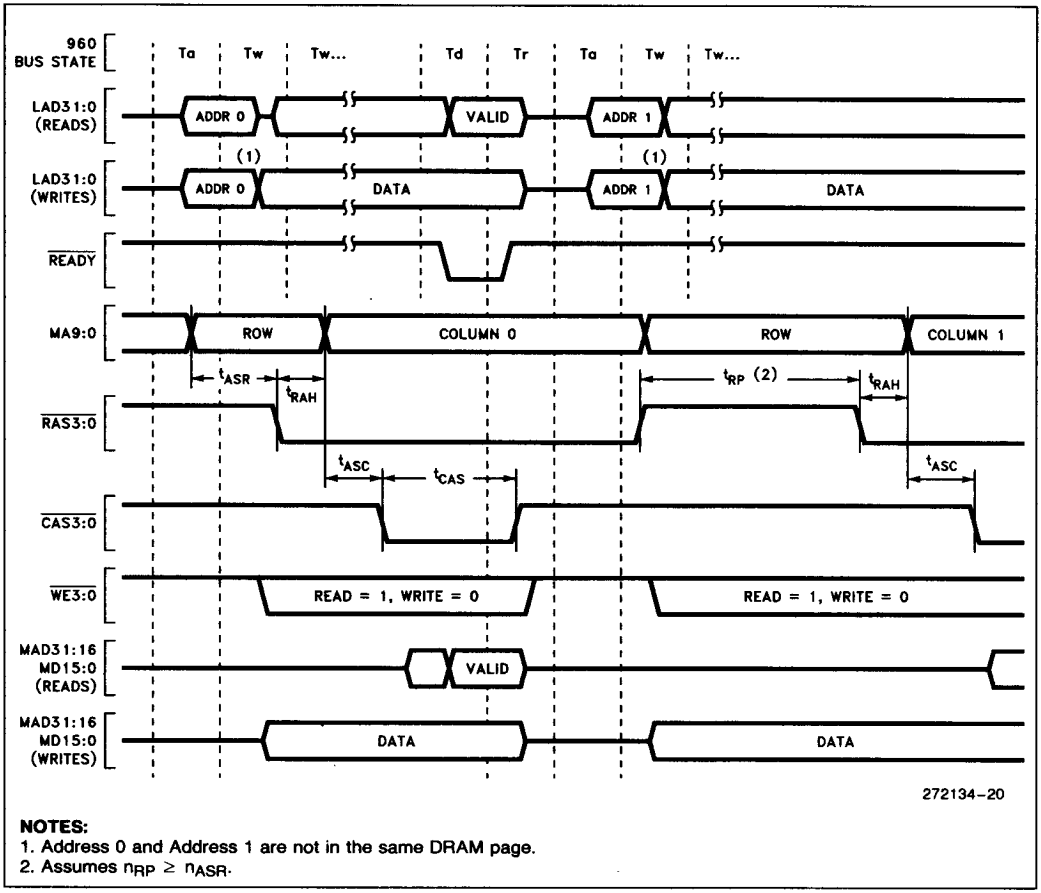
Figure 20. Static Column Mode Read Cycle

3



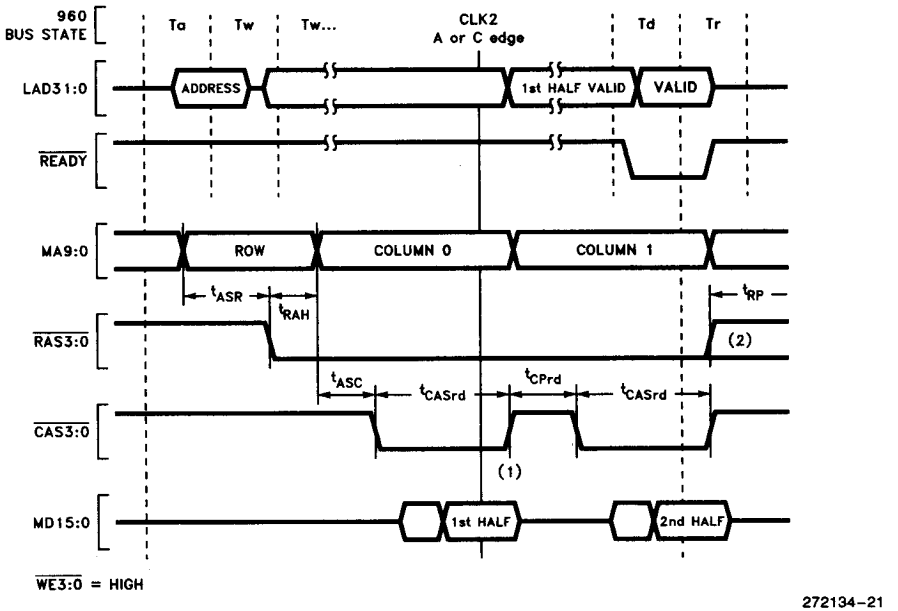
NOTES:
1. Address 0 and Address 1 are in the same DRAM page.
2. Timing shown is greater of t_{ASC} and t_{CP}.

Figure 21. DRAM Page Hit



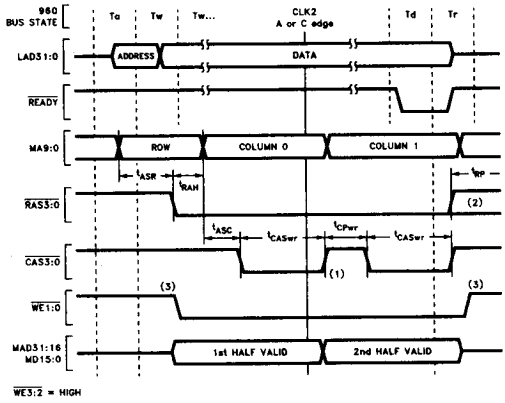
NOTES:
1. Address 0 and Address 1 are not in the same DRAM page.
2. Assumes $n_{RP} \geq n_{ASR}$.

Figure 22. DRAM Page Miss



NOTES:
1. Rising $\overline{CAS3:0}$ synchronous to CLK2 A- or C-edge on 1st half of packed read.
2. $\overline{RAS3:0}$ remains active if page cache is enabled.

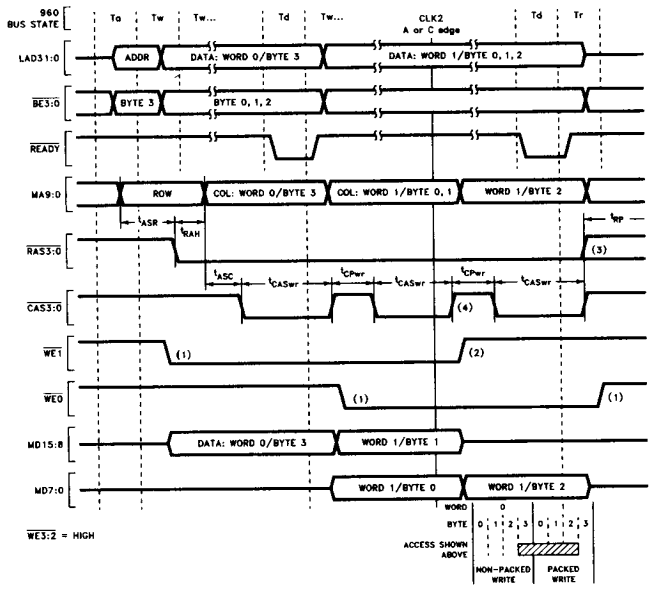
Figure 23. DRAM 16-Bit Page Mode Read Cycle



272134-22

NOTES:
1. Rising $\overline{CAS3:0}$ synchronous to CLK2 A- or C-edge on 1st half of packed write.
2. $\overline{RAS3:0}$ remains active if page cache is enabled.
3. $\overline{WE1:0}$ synchronous to CLK2 B-edge.

Figure 24. DRAM Aligned 16-Bit Page Mode Write Cycle



272134-23

NOTES:
1. $\overline{WE1:0}$ synchronous to CLK2 B-edge.
2. $\overline{WE1:0}$ synchronous to CLK2 B- or D-edge following rising $\overline{CAS3:0}$.
3. $\overline{RAS3:0}$ remains active if page cache is enabled.
4. $\overline{CAS3:0}$ rising edge synchronous to CLK2 A- or C-edge for first half of packed write.

Figure 25. DRAM Non-Aligned 16-Bit Write Cycle

7.5 ROM and I/O Controller Operational Waveforms

The following bus waveforms describe the operation of the ROM and I/O controller on the 82961KA. The ROM and I/O controller provides registers to configure timings and to optimize the ROM and I/O interface to many varieties of ROM and I/O. The ROM and I/O Operations Waveforms show only the timing parameters which may be adjusted by programming the 82961KA. These parameters are described in Table 20.

Table 20. ROM and I/O Controller Programmable Timings

Symbol	Description	Min Value	Max Value	Min Timing	Max Timing	Units
n_{ROMRDY}	READY Timing for ROM Accesses	0	15	1	16	1x Clocks
n_{RDWT}	$\overline{IORD}$ Wait High Time	0	31	0	32	1x Clocks
n_{RDACC}	$\overline{IORD}$ Access Low Time	0	31	1	32	1x Clocks
t_{WRWT}	$\overline{IOWR}$ Wait High Time	0	31	0	31	1x Clocks
n_{WRACC}	$\overline{IOWR}$ Access Low Time	0	31	1	32	1x Clocks
n_{IOREC}	I/O Recovery Time	0	31	0	31	1x Clocks
n_{IOCS}	$\overline{IOCS}$ Low Period	1	31	2	32	1x Clocks

NOTE:
A 1x clock is equal to $2*(t_C)$, or twice the CLK2 period.

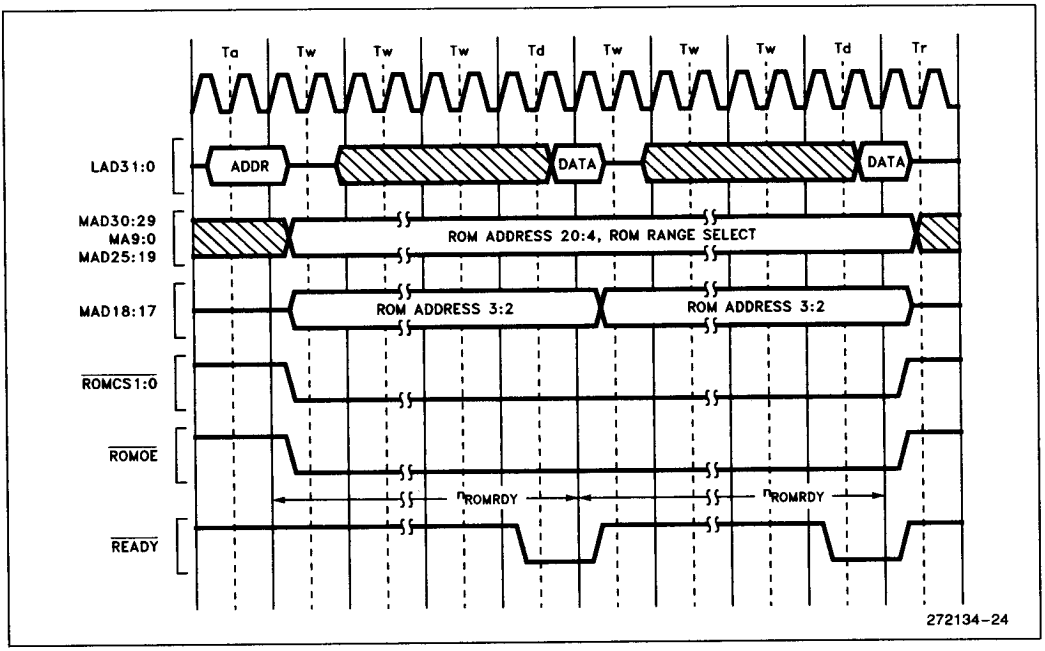


Figure 26. ROM Burst Read

3

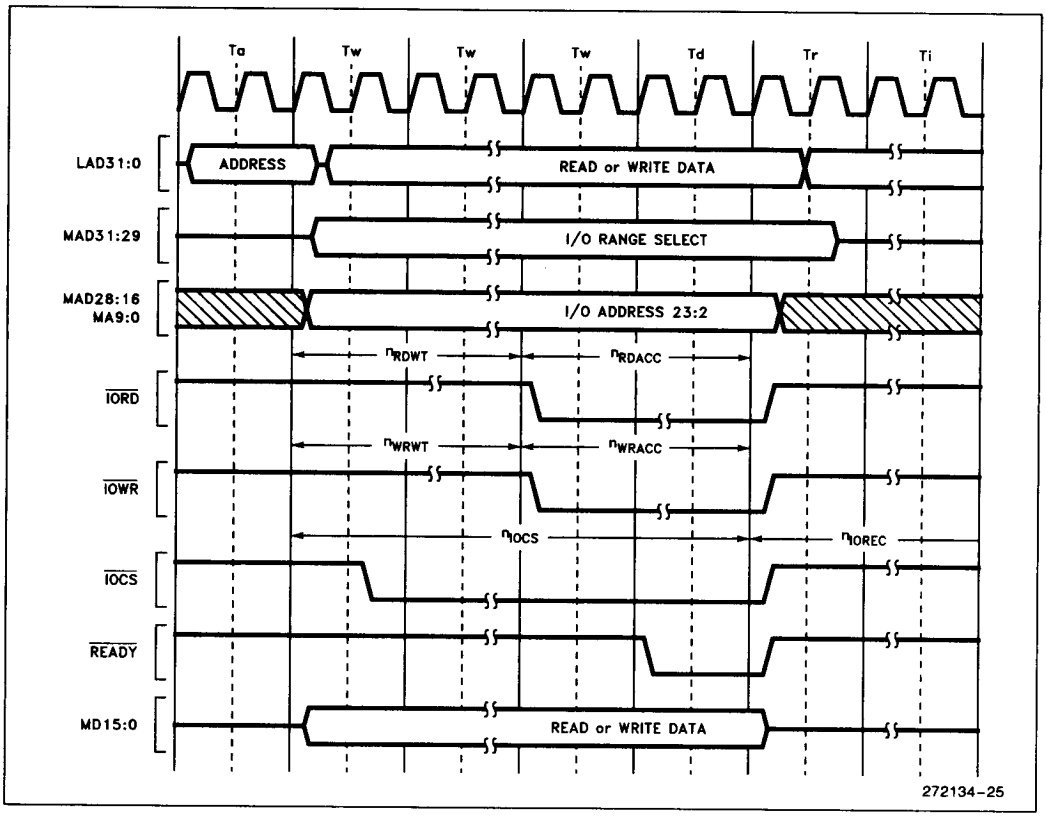


Figure 27. I/O Aligned Read or Write

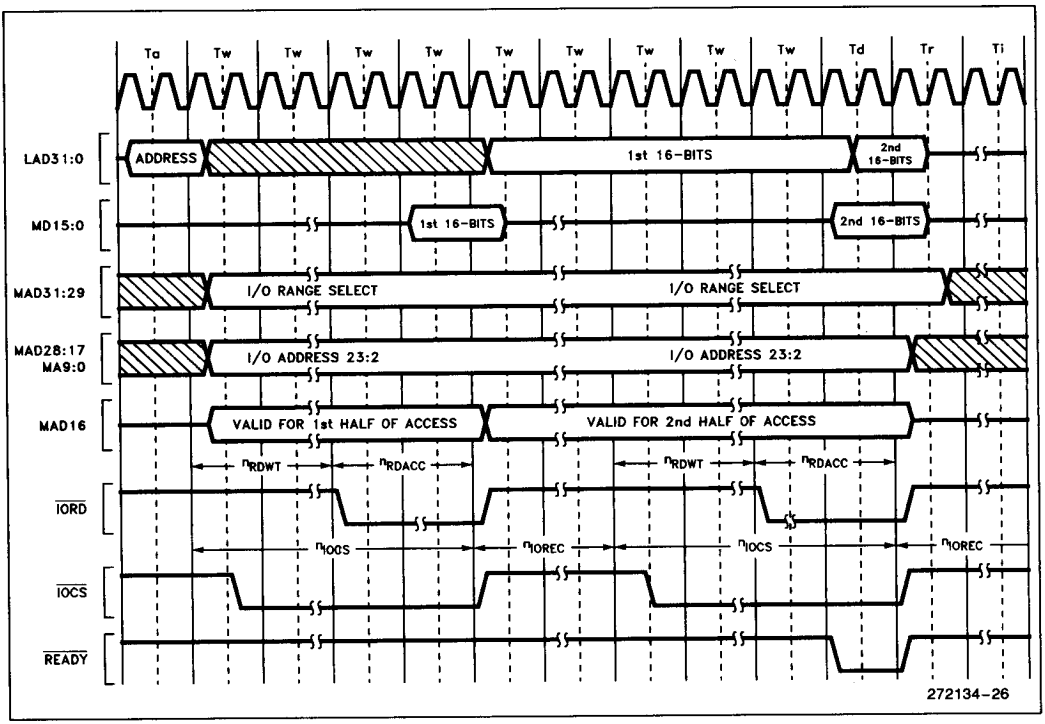


Figure 28. I/O Packed Read

3

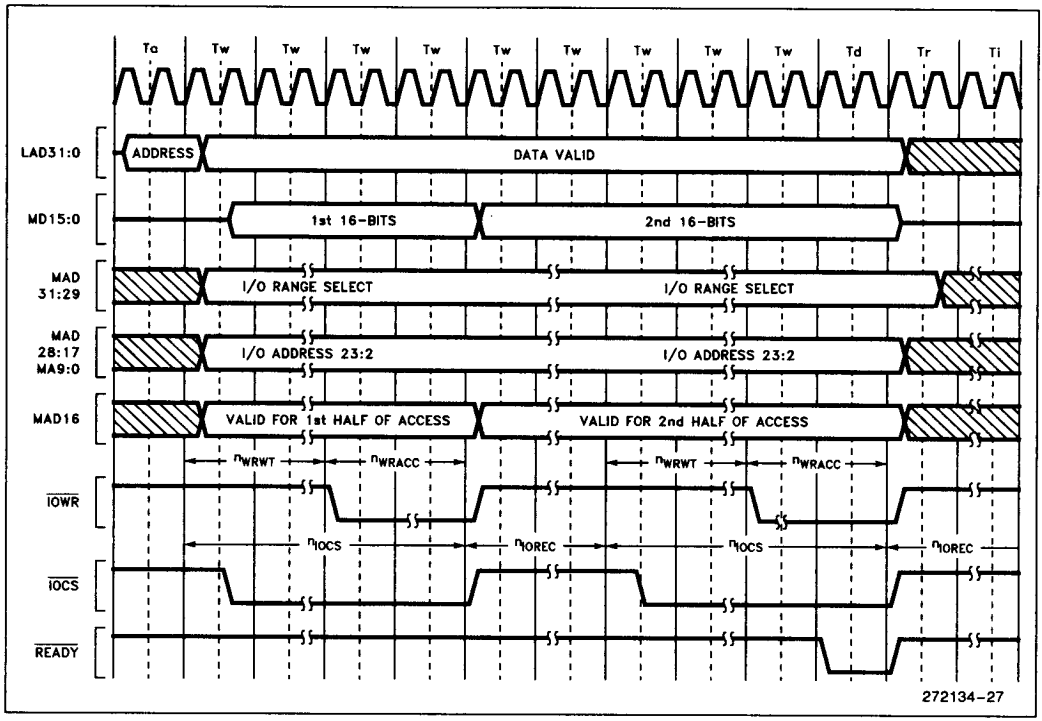


Figure 29. I/O Packed Write

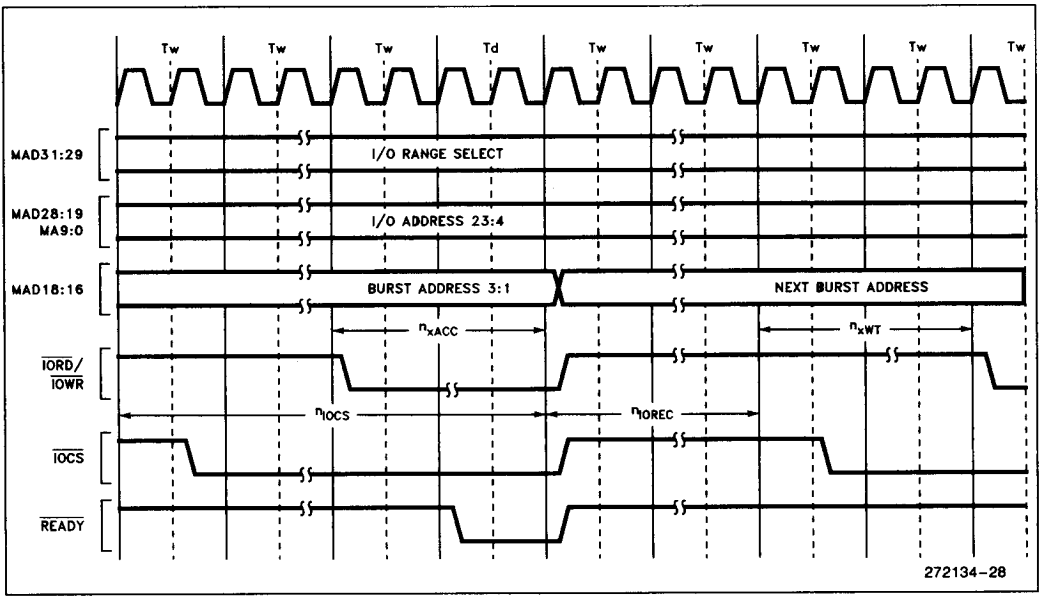


Figure 30. I/O Address Transition in Burst Mode

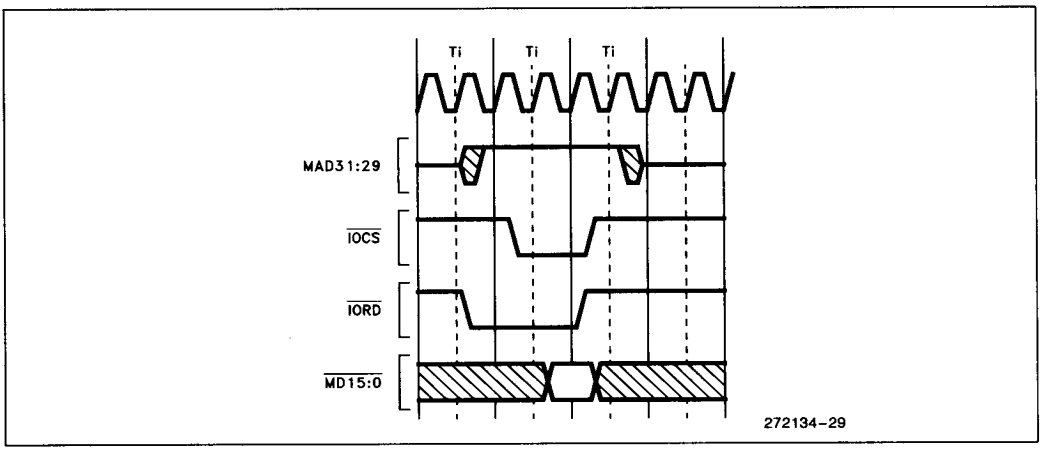


Figure 31. I/O Auto-Poll Cycle

7.6 Targeted Printer Video and Communications Timing Specifications

Table 21. Printer Video Interface Timings

82961KA-20, -16, -10 (20, 16, 10 MHz Specification)					
Symbol	**Parameter/Description**	**Min**	**Max**	**Units**	**Conditions**
t_{VC1}	$\overline{VCLK}$ Frequency, 1x Clock Mode		25	MHz	(Note 1)
t_{VC8}	$\overline{VCLK}$ Frequency, 8x Clock Mode		66	MHz	(Note 1)
t_{VCH}	$\overline{VCLK}$ High Time			ns	(Note 1)
t_{VCL}	$\overline{VCLK}$ Low Time			ns	(Note 1)
t_{VOV1}	$\overline{VIDEO}$ Output Valid, 1x Clock Mode		27	ns	(Note 1)
t_{VOV8}	$\overline{VIDEO}$ Output Valid, 8x Clock Mode		30	ns	(Note 1)
t_{VIS}	$\overline{LSYNC}$ Input Setup, 1x Clock Mode	0		ns	(Note 1)
t_{VIH}	$\overline{LSYNC}$ Input Hold, 1x Clock Mode	9		ns	(Note 1)
t_{VW1}	$\overline{FSYNC}$ Input Pulse Width, 1x Clock Mode	2		t_{VC1}	(Note 1)
t_{VW8}	$\overline{LSYNC}$, $\overline{FSYNC}$ Input Pulse Width, 8x Clock Mode	16		t_{VC8}	(Note 1)

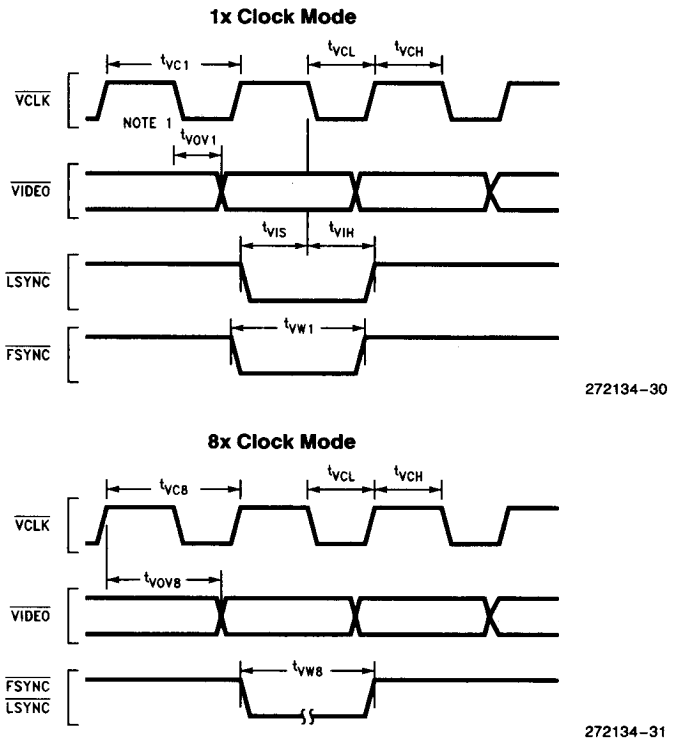
NOTE:
1. See Figure 30 for waveforms and specifications.

Table 22. Printer Communications Interface Timings

Symbol	Parameter/Description	Min	Max	Units	Conditions
82961KA Supplies $\overline{CCLK}$					
t_{PV}	$\overline{CMD}$ Output Valid Delay		4	2x Clocks	(Note 1)
t_{PS}	$\overline{STS}$ Input Setup	0		ns	(Note 1)
t_{PH}	$\overline{STS}$ Input Hold	4		2x Clocks	(Note 1)
t_{PSC}	$\overline{SBSY}$ Valid to $\overline{CCLK}$ Driven	0	6	2x Clocks	(Note 1)
	Programmable Parameters				
n_{PCK}	$\overline{CCLK}$ High and Low Time	1	4096	16 2x Clocks	(Notes 1, 2)
$\overline{CCLK}$ Supplied Externally					
t_{PV}	$\overline{CMD}$ Output Valid Delay		8	2x Clocks	(Note 1)
t_{PS}	$\overline{STS}$ Input Setup	0		2x Clocks	(Note 1)
t_{PH}	$\overline{STS}$ Input Hold	8		2x Clocks	(Note 1)
t_{PC}	$\overline{CCLK}$ Period	16		2x Clocks	(Note 1)
t_{PCH}	$\overline{CCLK}$ High Time	8		2x Clocks	(Note 1)
t_{PCL}	$\overline{CCLK}$ Low Time	8		2x Clocks	(Note 1)
t_{PCS}	$\overline{SBSY}$ Setup to $\overline{CCLK}$ Valid	0		2x Clocks	(Note 1)
	Programmable Parameters				
n_{PF}	$\overline{CMD}$ and $\overline{CBSY}$ Float Time	1	4096	16 2x Clocks	(Notes 1, 2)

NOTES:
1. See Figures 31 and 32 for waveforms and specifications.
2. n_{PCK} and n_{PF} are programmed through the $\overline{CCLK}$ divisor register; parameter is programmed in (n*16) 2x clocks.

3



NOTE:
1. t_{VDV1} is referenced to the edge of $\overline{VCLK}$ that is programmed for video data output.

Figure 32. Printer Video Interface Timing

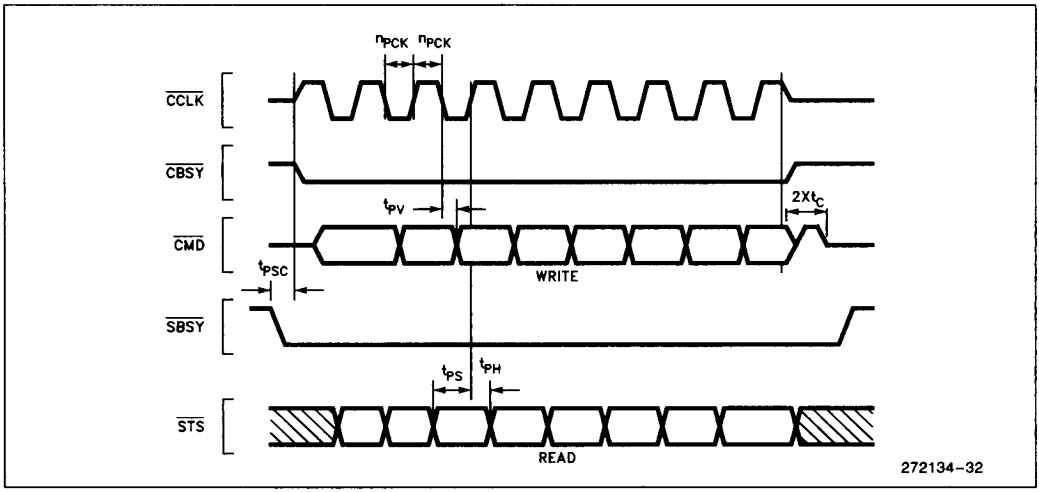


Figure 33. Printer Communications Interface Timing (82961KA Supplies $\overline{\text{CCLK}}$)

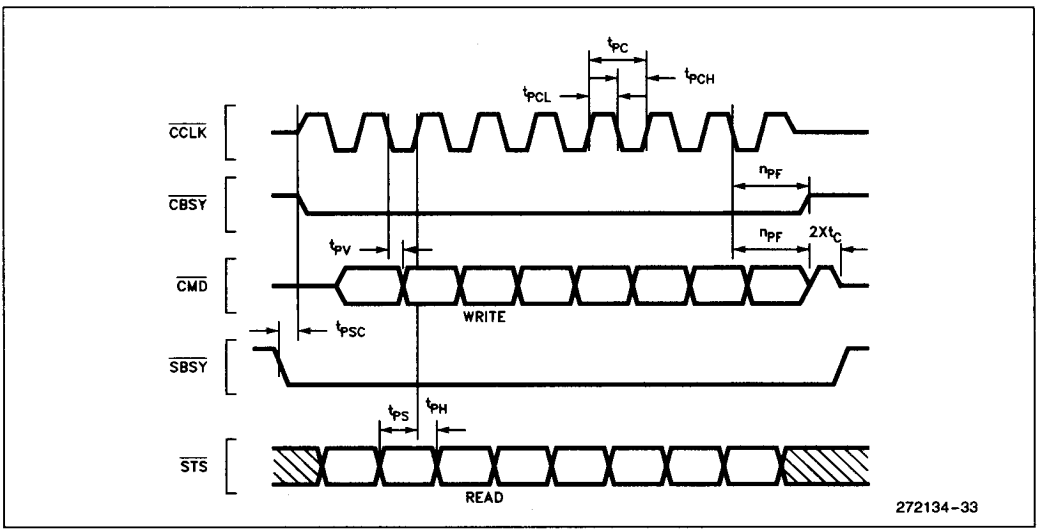


Figure 34. Printer Communications Interface Timing ($\overline{\text{CCLK}}$ Supplied Externally)