FEATURES/BENEFITS

- High-speed CMOS equivalent to Bipolar PAL
- CMOS UV-erasable EPROM cell to allow reprogrammability
- Low power (35 mA Max. I_{CC}) and Standard (70 mA Max. I_{CC}) versions
- Four speed grades (t_{PD} = 15ns Max, t_{PD}=20ns Max, t_{PD}=25ns Max, and t_{PD} = 35ns Max)
- Available over both commercial and industrial temperature ranges
- >2000V ESD input and output protection
- 100% functional and AC tested
- 100% programming tested
- Programmable security bit to prevent pattern duplication
- Register preload for register initialization
- Programmable three-state outputs

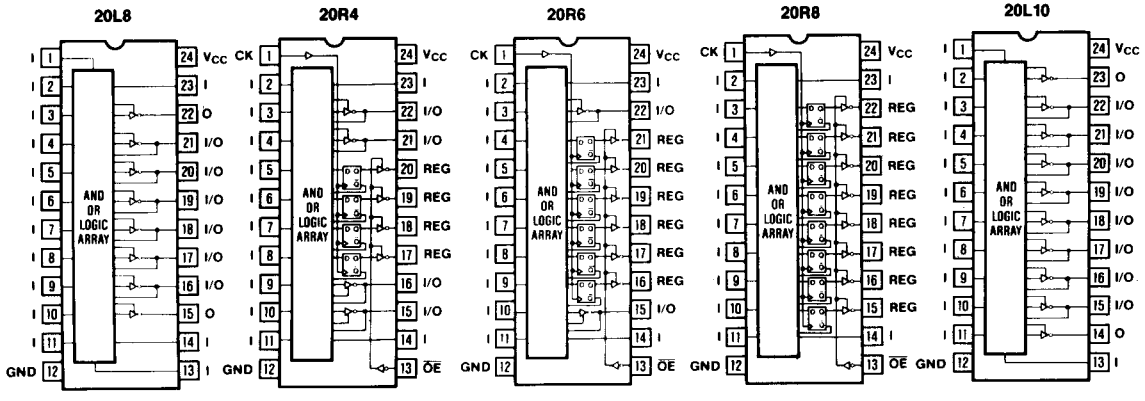
DESCRIPTION

The CPL24 Series devices are high-speed, UV-erasable, electrically programmable CMOS logic replacements of the Bipolar 24-pin PAL20R8 family and PAL20L10 devices. They utilize the familiar sum-of-products form (AND array followed by an OR array) allowing the user to customize logic to his/her needs.

Five devices are offered in the CPL24 Series. They are: the CPL20L10, the CPL20L8, the CPL20R4, the CPL20R6, and the CPL20R8. Each of these devices has 20 array inputs. The CPL20L10 has 10 outputs and the others have 8 outputs. All the outputs to the CPL20L8 and CPL20L10 are combinatorial, while all outputs to the CPL20R8 are registered. In contrast, the CPL20R4 has 4 registered and 4 combinatorial outputs and the CPL20R6 has 6 registered and 2 combinatorial outputs. Each combinatorial output in the CPL20R6 and CPL20R4 devices serves as an I/O pin. The CPL20L10 device has 8 I/O pins, and the CPL20L8 device has 6 I/O pins.

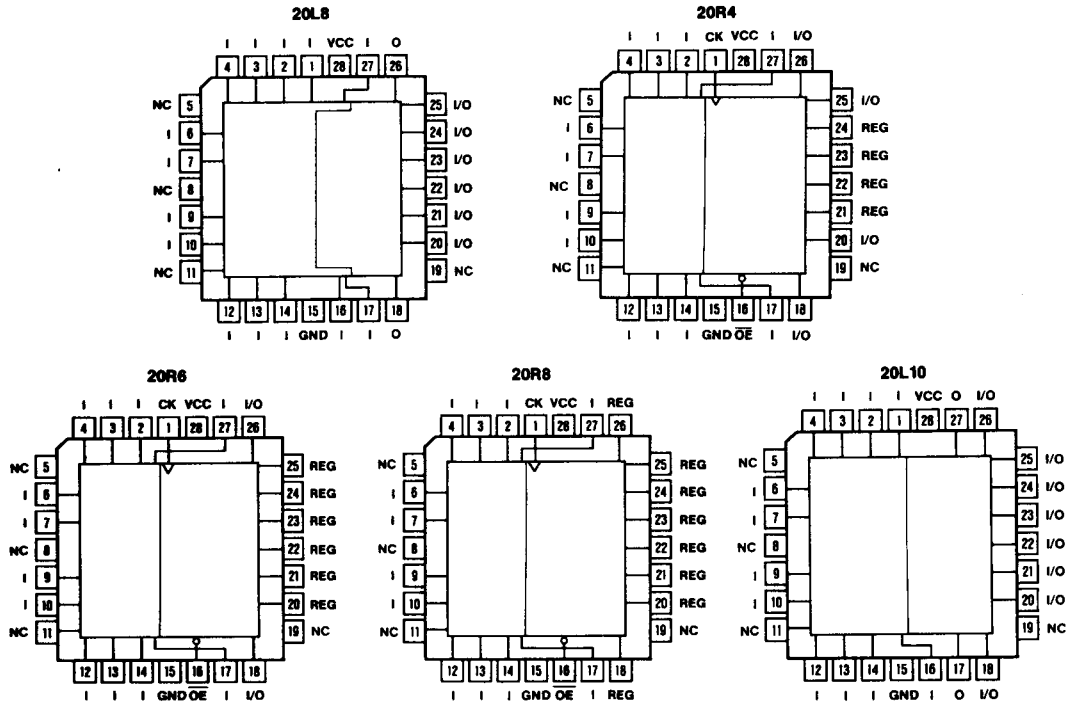
3

LOGIC SYMBOLS AND PINOUTS



DIP PACKAGES

LOGIC SYMBOLS AND PINOUTS (Continued)



PLCC PACKAGES (NL)

DESCRIPTION (Continued)

The CPL devices are manufactured using a 1.2 micron EPROM technology which offers low power dissipation (45/70 mA maximum I_{CC}) combined with high performance (15ns maximum propagation delay). Because the CPL devices are erasable, they can be thoroughly tested for programming, functional and AC integrity, resulting in high-reliability and 100% programming yields.

The CPL24 devices are housed in 24-pin plastic DIP, and windowed CERDIP packages, as well as a 28-pin PLCC package. The windowed CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The plastic DIP, and PLCC devices are one-time-programmable (OTP) and may not be erased.

Register Preload

The register preload feature of the CPL24 Series allows output pins to be loaded with arbitrary states, making functional testing easier than ever.

Security Bit

All CPL24 devices feature a security bit. The security bit allows the user to protect his/her design against unauthorized duplication. When the security bit is set, the contents of the programmable-cell array may not be accessed in Read or Verify modes. Since the CPL devices do not have visible fuses, they offer enhanced security over what is available in bipolar PAL devices.

Test Array

Another feature of the devices in the CPL24 Series is the on-chip test array. It is programmed for final functional and AC testing of the devices after they have been packaged (even if the security bits have been programmed). In the normal operation of the device, the test arrays are not accessed. In the test mode of operation, only the input terms in the shaded portion of the functional block diagram are accessed. The test array facilitates high-reliability as well as simple and short testing.

ERASURE (windowed-CERDIP only)

The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:

Wavelength of 2537 Angstroms
(minimum dose -- 25 Wsec/cm^2)

If an ultraviolet lamp with a 12mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

3

CPL24 ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leqq$ 20mA)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage	V_{PP}	14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS For all CPL24, except CPL24-15

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Industrial	T_A	-40 to +105	°C

RECOMMENDED OPERATING CONDITIONS For CPL24-15

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.75 to 5.25	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Industrial	T_A	-40 to +105	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions

Parameter	Symbol	Test Conditions		Min	Max	Unit
Low Level Input Voltage	V_{IL}				0.8	V
High Level Input Voltage	V_{IH}			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$		-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24mA		0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.2mA	2.4		V
Off-State Output Leakage Current	I_{OZL}	V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL}	V_O = 0.4V		-100	μA
	I_{OZH}		V_O = 2.4V		100	
Power Supply Current	I_{CC}	All inputs = GND, V_{CC} = Max, I_{OUT} = 0mA	"L" STD "L-15"		35 70 45	mA mA mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

CPL24 AC ELECTRICAL CHARACTERISTICS, CPL20L10 only

Over Recommended Operating Conditions (Note 5)

		Commercial (0 to +70°C)								Industrial (-40 to +105°C)								
		-15		-20		-25		-30		-15*		-20		-25		-30		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input or Feedback to Non-Registered Output, 20L10	t_{PD}		15		20		25		30		15		20		25		30	ns
Input to Output Enabled, 20L10	t_{PZX}		15		20		25		30		15		20		25		30	ns
Input to Output Disabled, 20L10	t_{PXZ}		15		20		25		30		15		20		25		30	ns
Clock Width (High or Low)	t_W	10		15		15		18		10		15		15		18		ns
Clock Period	t_P	24		30		35		40		24		30		35		40		ns
Maximum Frequency	f_{MAX}	41.6		33.3		28.5		25		41.6		33.3		28.5		25		MHz

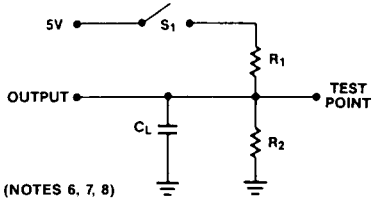
CPL24 AC ELECTRICAL CHARACTERISTICS, except CPL20L10

Over Recommended Operating Conditions (Note 5)

Parameter	Symbol	Commercial (0 to +70°C)								Industrial (-40 to +105°C)								Unit
		-15		-20		-25		-35		-15		-20		-25		-35		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input or Feedback to Non-Registered Output, 20R6, 20R4, 20L8	t_{PD}		15		20		25		35		15		20		25		35	ns
Clock to Registered Output or Feedback, 20R8, 20R6, 20R4	t_{CO}		12		15		15		25		12		15		15		25	ns
Pin 13 to Output Enabled, 20R8, 20R6, 20R4	t_{PZX13}		12		15		20		25		12		15		20		25	ns
Pin 13 to Output Disabled, 20R8, 20R6, 20R4	t_{PXZ13}		12		15		20		25		12		15		20		25	ns
Input to Output Enabled, 20R6, 20R4, 20L8	t_{PZX}		15		20		25		35		15		20		25		35	ns
Input to Output Disabled, 20R6, 20R4, 20L8	t_{PXZ}		15		20		25		35		15		20		25		35	ns
Setup Time from Input or Feedback to Clock, 20R8, 20R6, 20R4	t_{SU}	12		15		20		30		12		20		20		30		ns
Hold Time, 20R8, 20R6, 20R4	t_H	0		0		0		0		0		0		0		0		ns
Clock Width (High or Low)	t_W	10		15		15		20		10		15		15		20		ns
Clock Period	t_P	24		30		35		55		24		30		35		55		ns
Maximum Frequency	f_{MAX}	41.6		33.3		28.5		18		41.6		33.3		28.5		18		MHz

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6$ns.

AC Test Circuit



Resistor Values (Ω)

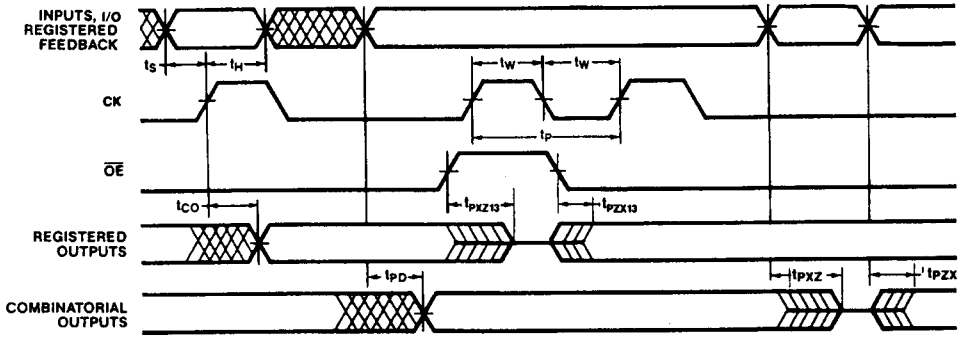
R1	R2
200	390

Note 6: C_L includes load and test jig capacitance.

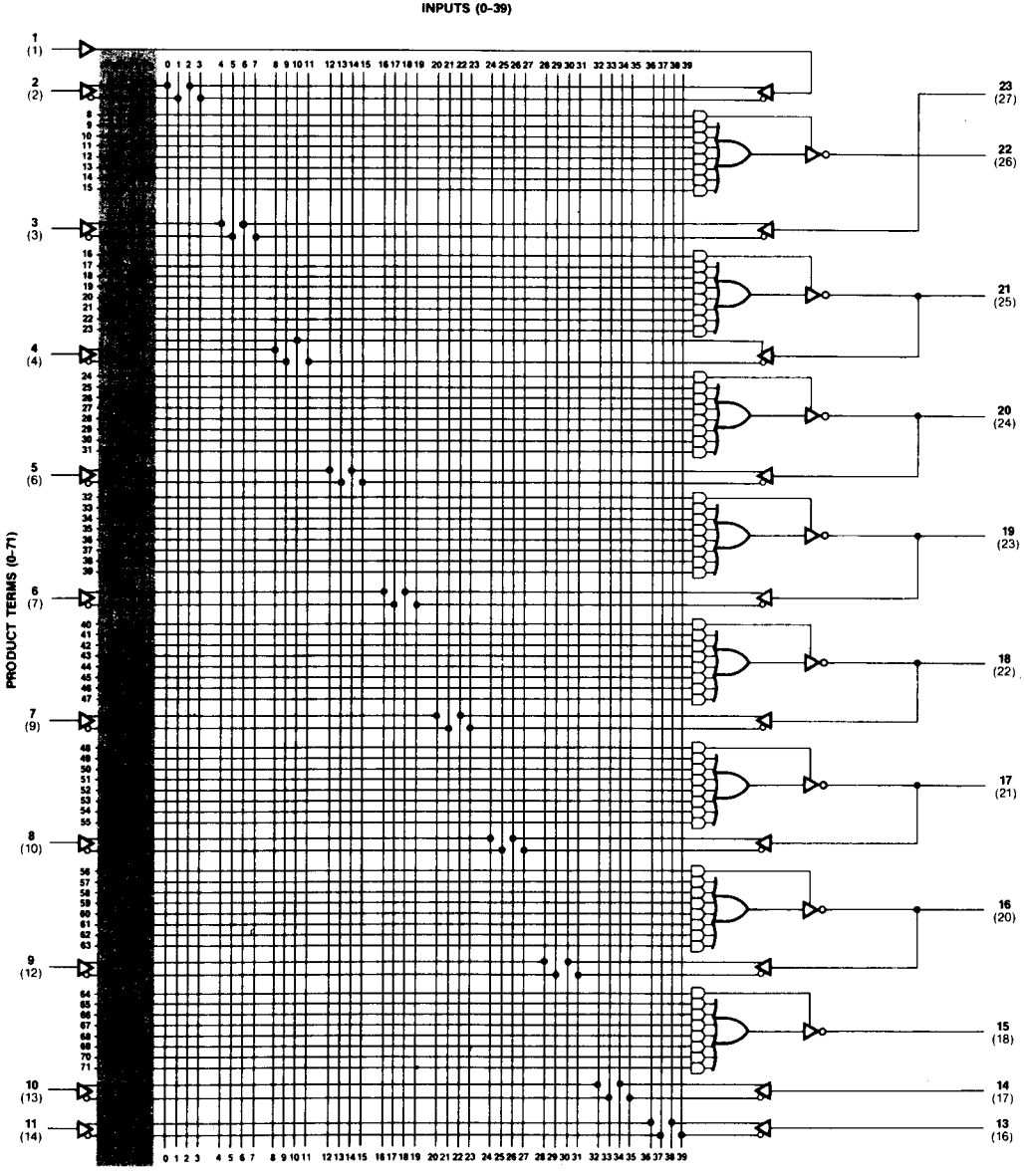
Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

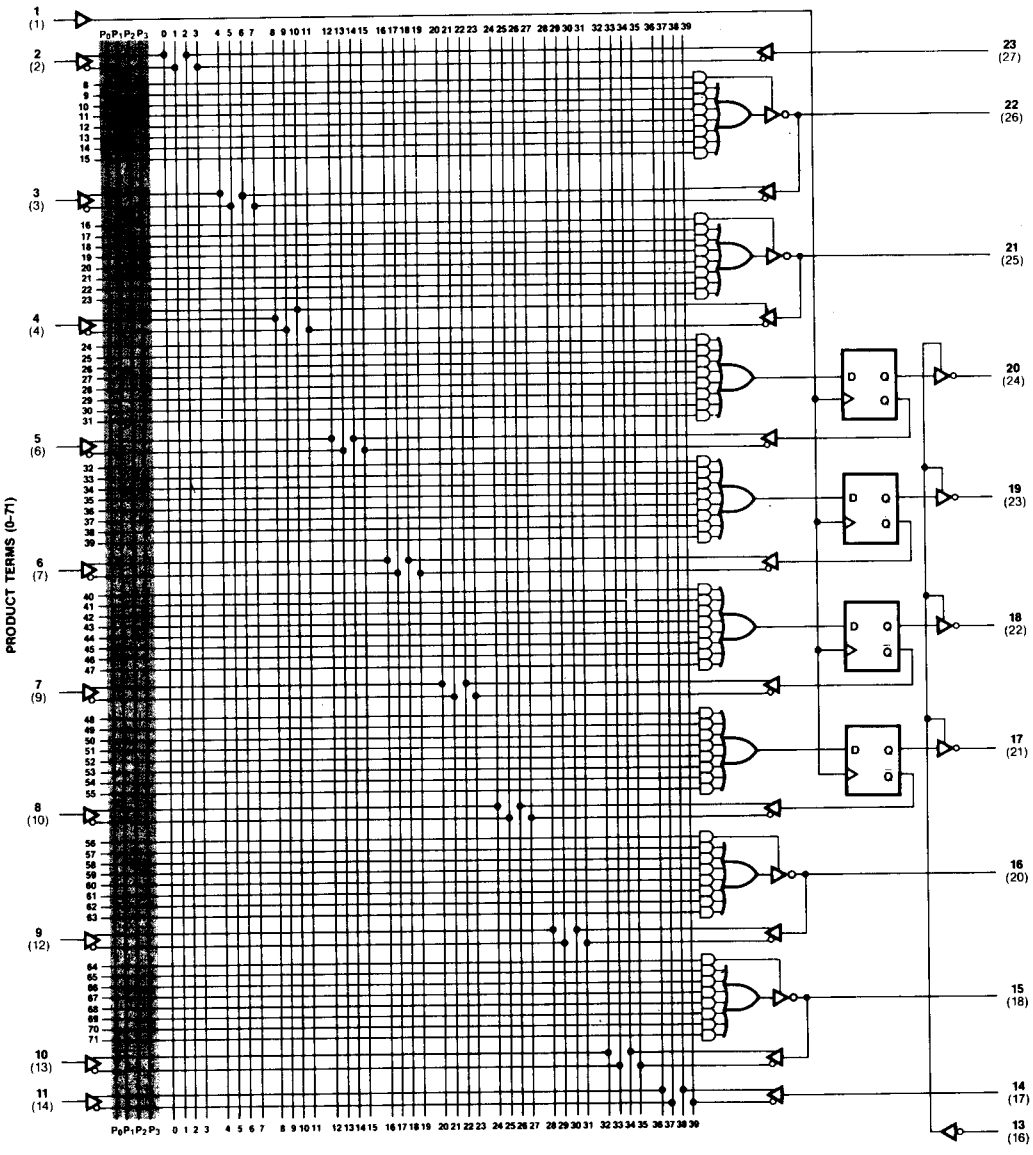
CPL24 WAVEFORMS



CPL20L8

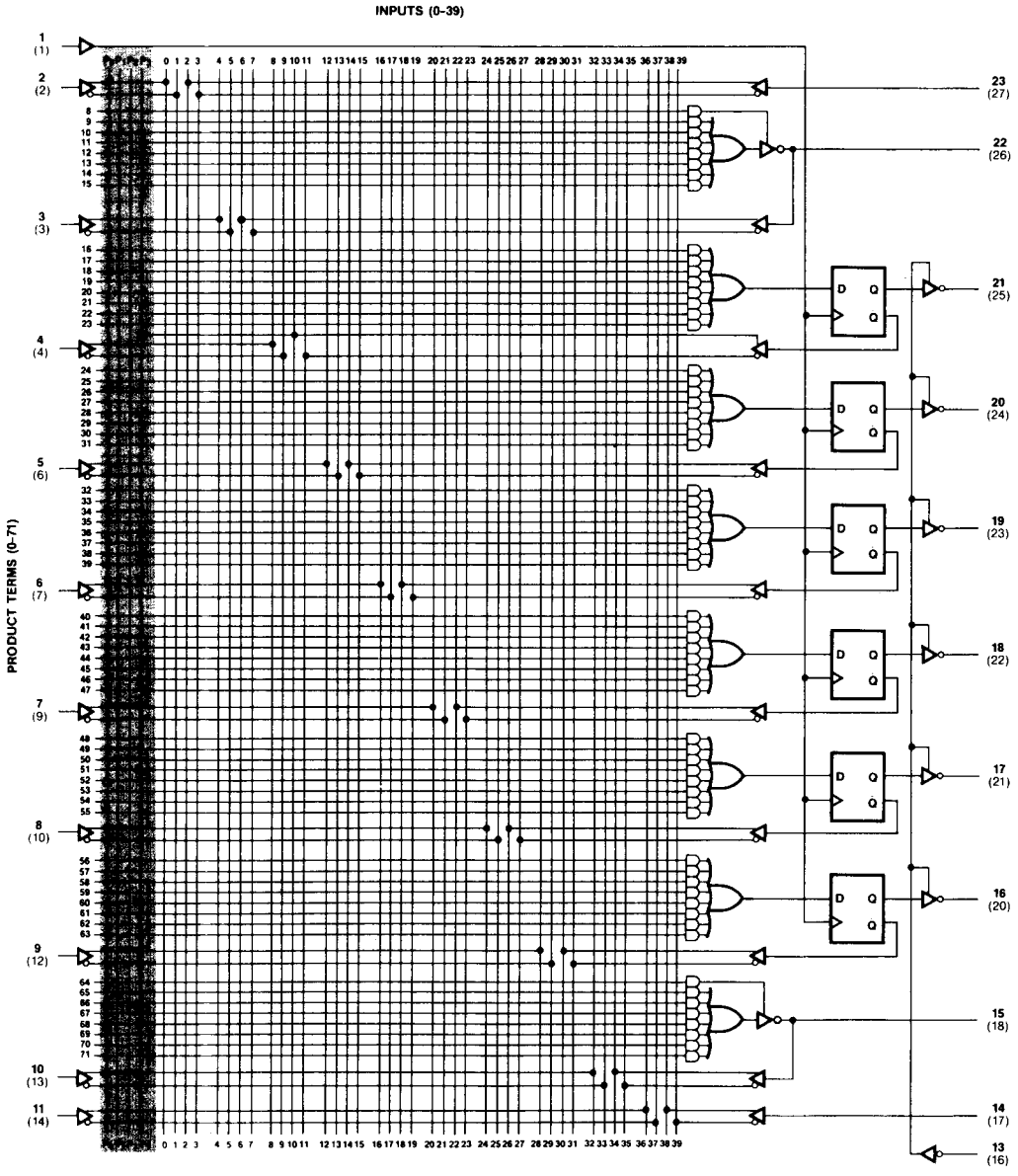

INPUTS (0-39)
PRODUCT TERMS (0-71)
1 (1)
2 (2)
3 (3)
4 (4)
5 (6)
6 (7)
7 (9)
8 (10)
9 (12)
10 (13)
11 (14)
23 (27)
22 (26)
21 (25)
20 (24)
19 (23)
18 (22)
17 (21)
16 (20)
15 (18)
14 (17)
13 (16)

CPL20R4

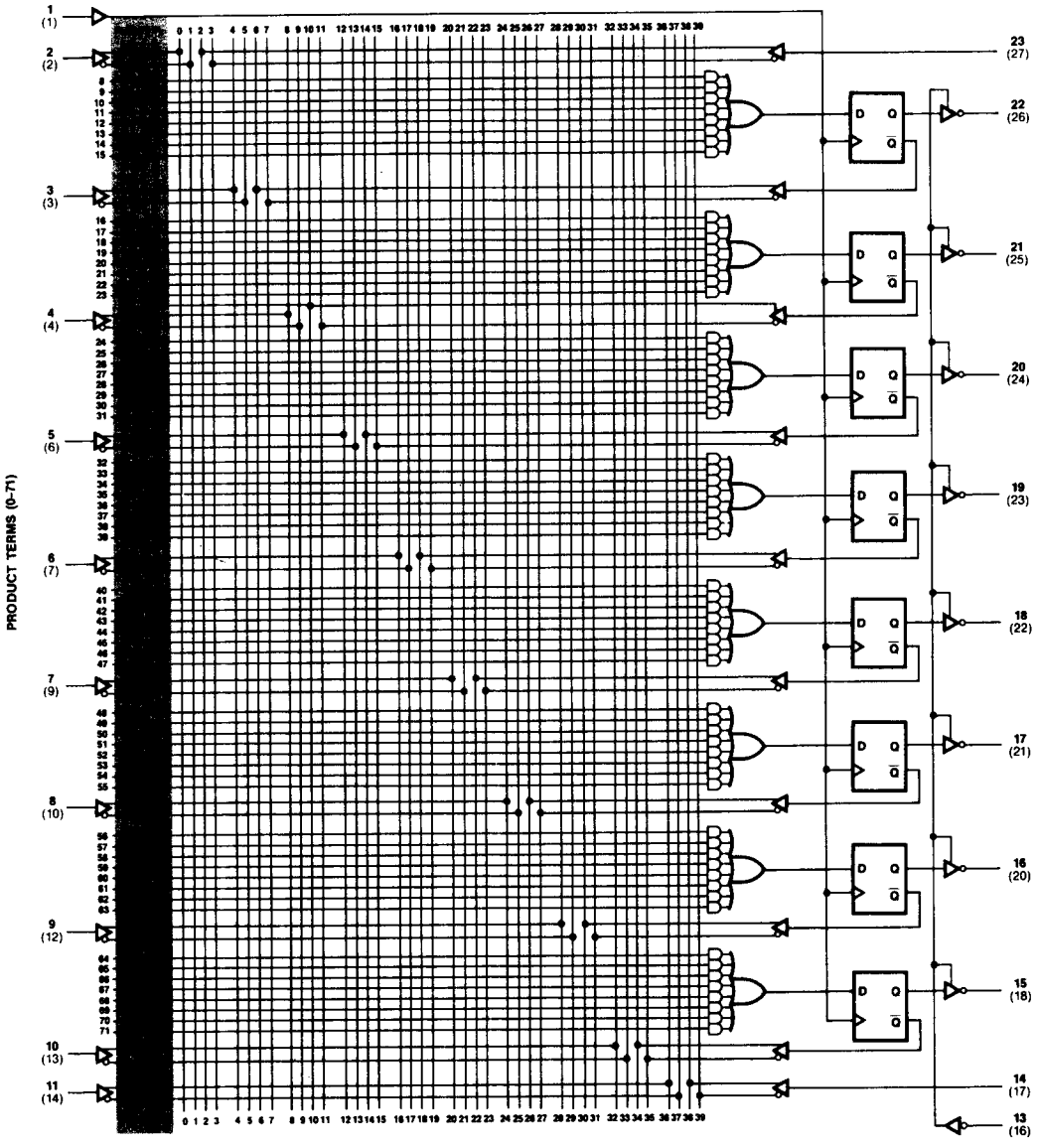

INPUTS (0-39)
PRODUCT TERMS (0-71)
1 (1)
2 (2)
3 (3)
4 (4)
5 (6)
6 (7)
7 (9)
8 (10)
9 (12)
10 (13)
11 (14)
23 (27)
22 (26)
21 (25)
20 (24)
19 (23)
18 (22)
17 (21)
16 (20)
15 (18)
14 (17)
13 (16)
D Q
Q

CPL24 FUNCTIONAL LOGIC DIAGRAMS (Continued)
DIP AND PLCC PINOUTS

CPL20R6

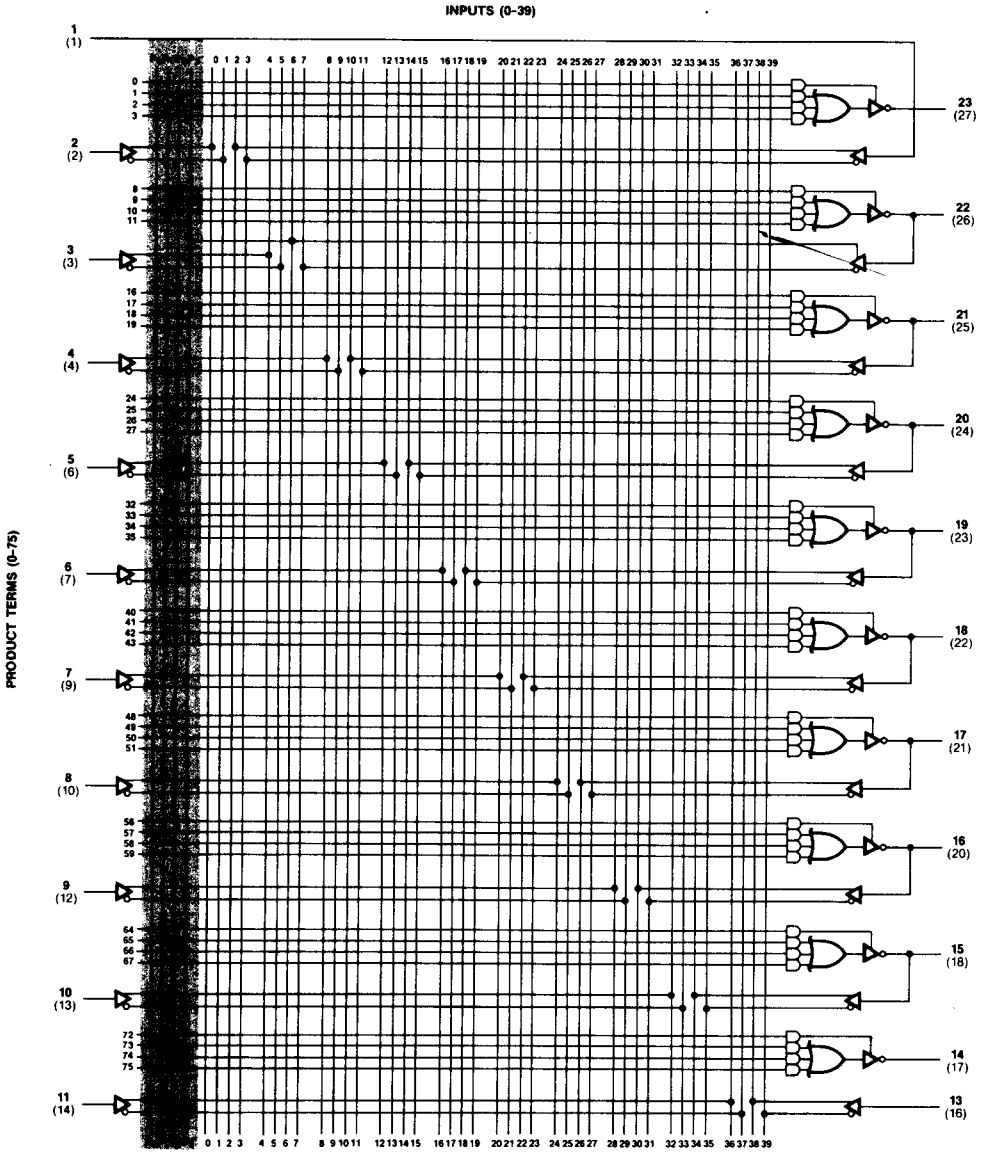


CPL20R8


INPUTS (0-39)
PRODUCT TERMS (0-71)
1 (1)
2 (2)
3 (3)
4 (4)
5 (6)
6 (7)
7 (9)
8 (10)
9 (12)
10 (13)
11 (14)
23 (27)
22 (26)
21 (25)
20 (24)
19 (23)
18 (22)
17 (21)
16 (20)
15 (18)
14 (17)
13 (16)
D
Q

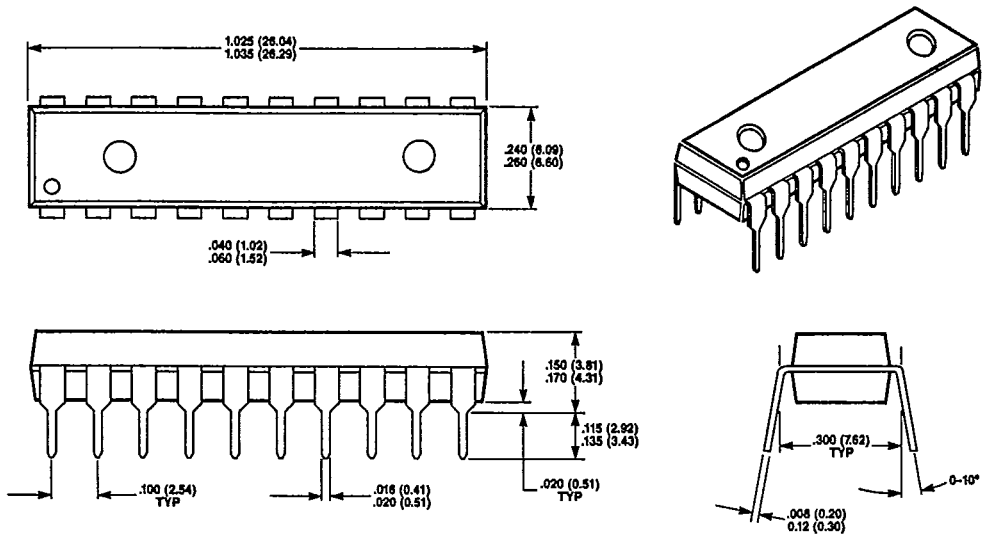
CPL24 FUNCTIONAL LOGIC DIAGRAMS
DIP AND PLCC PINOUTS

CPL20L10



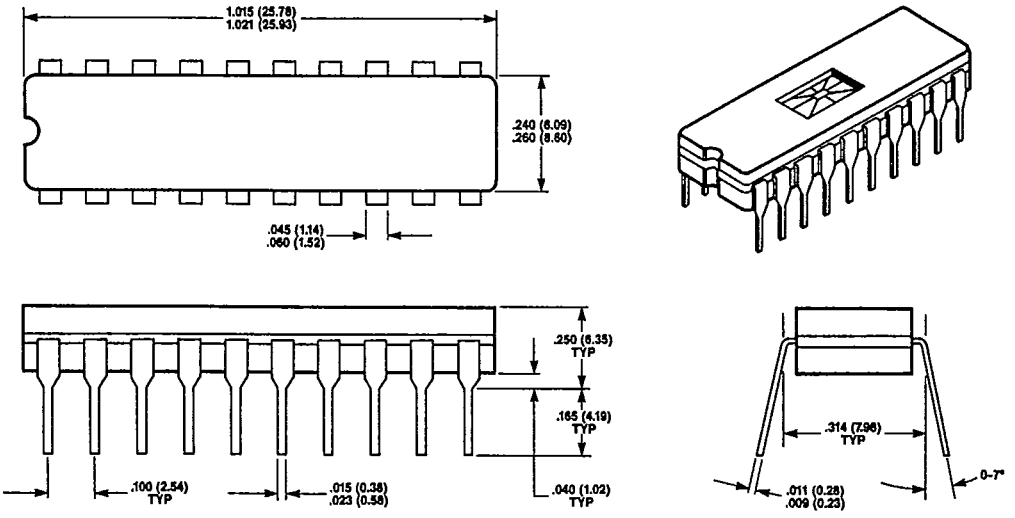
T-90-20

20 PIN PLASTIC DIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

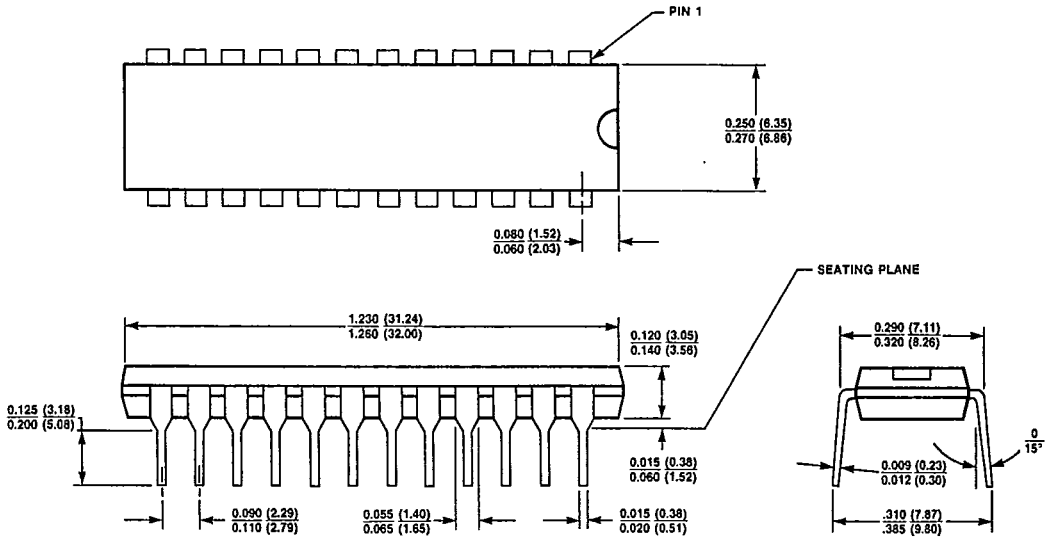
20 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

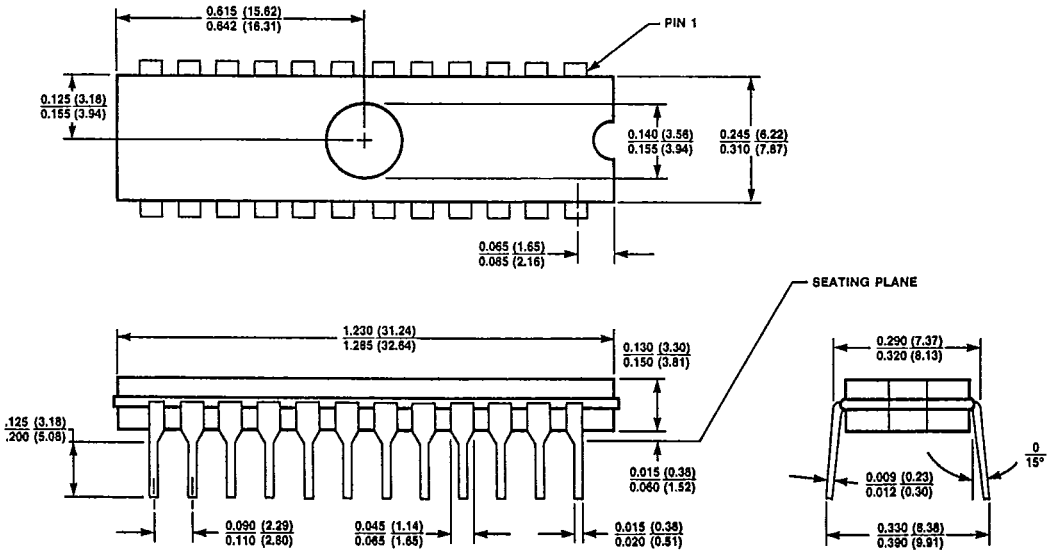
7

24 PIN PLASTIC DIP



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

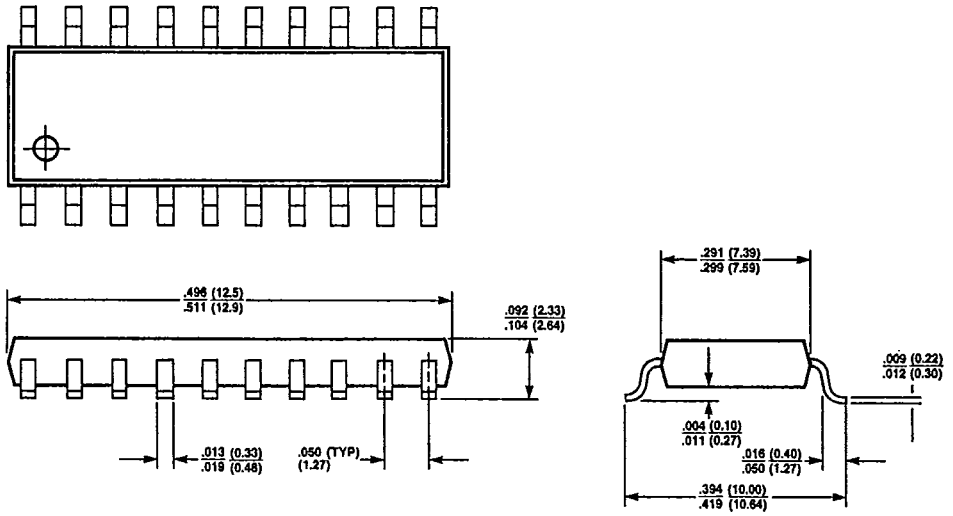
24 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

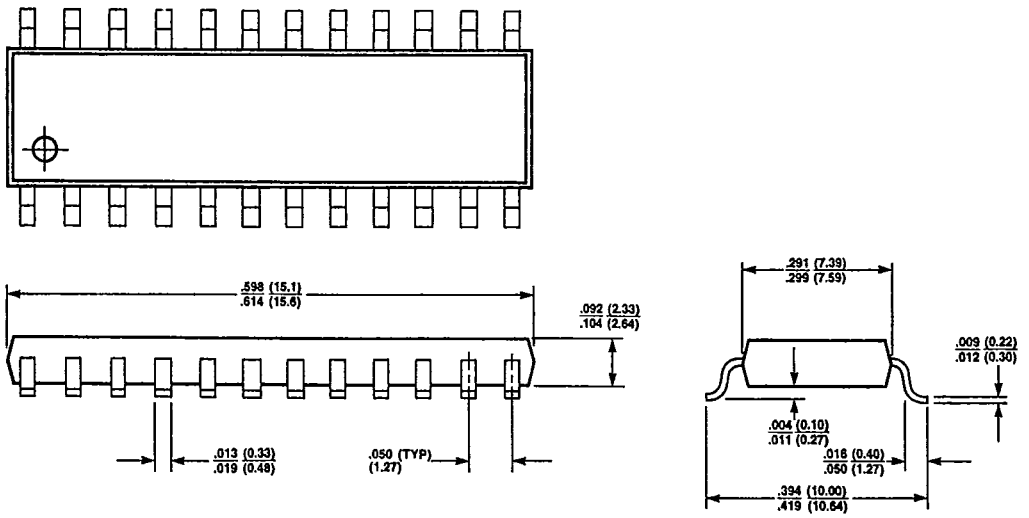
T-90-20

20 PIN SOIC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

24 PIN SOIC

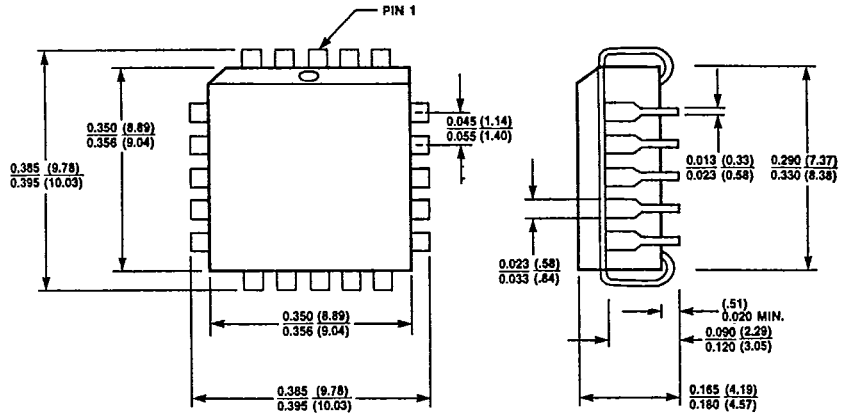


DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

7

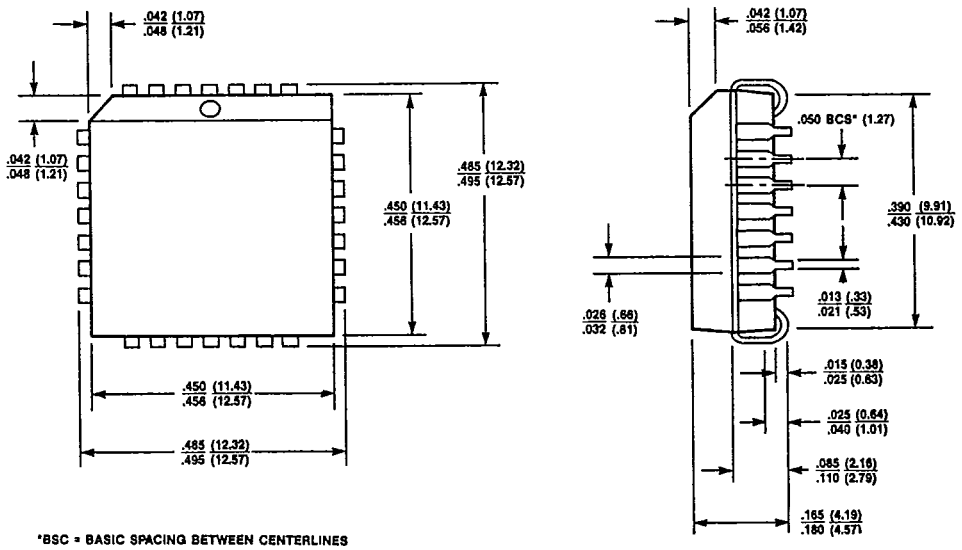
T-90-20

20 PIN PLCC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

28 PIN PLCC



*BSC = BASIC SPACING BETWEEN CENTERLINES

DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.