AVX KYOCERA

KXO-HC/KHO-HC Series Crystal Clock Oscillators

HCMOS Drive - TTL or CMOS Compatible

f_O: 1 to 80 MHz

FEATURES

1) High speed CMOS clock oscillator
2) High power drive level
3) Low current consumption
4) Output available with TTL or CMOS compatibility
5) Enable/disable option
6) KHO-HC in 8 pin DIP

HOW TO ORDER

KXO-HC 1 -T S E - 32.0000M T

① ② ③ ④ ⑤ ⑥

①Type: KXO = 14 pin DIP; KHO = 8 pin DIP

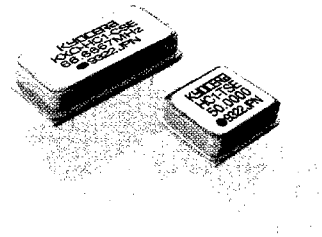
②Frequency precision:
S = ±25ppm (special), 0 = ±50ppm, 1 = ±100ppm

③Output level/Duty cycle:
TS = TTL compatible/45 to 55%
CS = CMOS compatible/45 to 55%

④Enable/Disable function:
□ = without function, E = with function

⑤Frequency

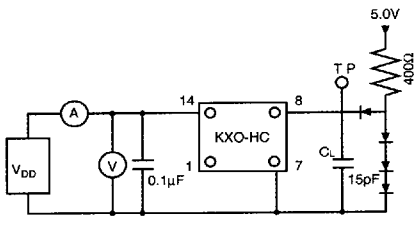
⑥Packaging:
T = tube



SPECIFICATIONS (KXO-HC-T/KHO-HC-T TTL COMPATIBLE)

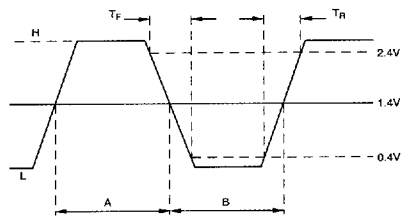
Classification		Code	Rating		Unit	Remarks
Output Frequency		f_{OUT}	1 to 50	>50	MHz	
Frequency Precision		$\Delta f/f_O$	S:±25 0:±50 1:±100	S:±25 0:±50 1:±100	ppm ppm ppm	0 to 70°C 4.5V to 5.5V
Operating Temperature Range		T_{OPR}	0 to +70	0 to +70	°C	
Voltage		V_{DD}	5±0.5	5±0.25	V	
Electrical Current Consumption		I_{DD}	50 max	70 max	mA	f=50MHz, C_L=15pF (10TTL load)
Output	Duty Cycle	S_Y	45 to 55	45 to 55	%	1.4V DC level
	"0" Level	V_{OL}	0.4 max	0.4 max	V	At I_{OL}=16mA
	"1" Level	V_{OH}	2.4 min	2.4 min	V	At I_{OH}=-1mA
	Rise and Fall Time	T_R, T_F	5 max	3.5 max	nsec	0.4V to 2.4V, C_L=15pF (10TTL load)
Fan Out			TTL 10 gates	TTL 10 gates		CMOS level OK
Time to Enable/Disable			100 max	100 max	nsec	Tristate output
Input Current		I_{IH} I_{IL}	10 max -150 max	10 max -150 max	µA µA	
Input Voltage		V_{IH} V_{IL}	2.2 min 0.8 max	2.2 min 0.8 max	V V	

TEST CIRCUIT (KXO-HC-T/KHO-HC-T)



CL=15pF max
(Inclusive of test jig and probe capacitance)

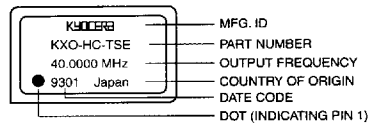
SHAPE OF OUTPUT WAVE (KXO-HC-T/KHO-HC-T)



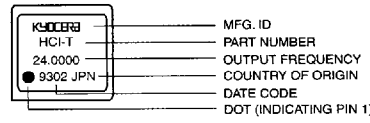
Duty Ratio= $\frac{A}{A+B}$

MARKINGS

KXO-HC



KHO-HC



KXO-HC/KHO-HC Series Crystal Clock Oscillators

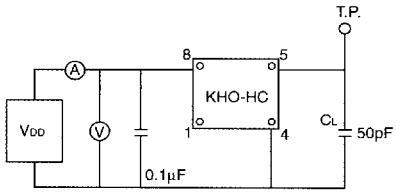
HCMOS Drive - TTL or CMOS Compatible

f_o: 1 to 80 MHz

SPECIFICATIONS (KXO-HC-C/KHO-HC-C CMOS COMPATIBLE)

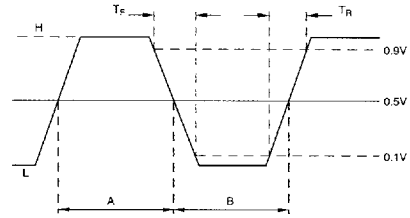
Classification		Code	Rating		Unit	Remarks
Output Frequency		f_{OUT}	1 to 50	>50	MHz	
Frequency Precision		$\Delta f/f_O$	S:±25 0:±50 1:±100	S:±25 0:±50 1:±100	ppm ppm ppm	 0 to 70°C 4.5V to 5.5V
Operating Temperature Range		T_{OPR}	0 to +70	0 to +70	°C	
Voltage		V_{DD}	5±0.5	5±0.25	V	
Electrical Current Consumption		I_{DD}	50 max	80 max	mA	f=>50MHz, C_L=15pF f=<50MHz, C_L=50pF
Output	Duty Cycle	S_Y	45 to 55	45 to 55	%	1/2V_{DD} level
	"0" Level	V_{OL}	0.1 V_{DD} max	0.1 V_{DD} max	V	At I_{OL}=16mA
	"1" Level	V_{OH}	0.9 V_{DD} min	0.9 V_{DD} min	V	At I_{OH}=-1mA
	Rise and Fall Time	T_R, T_F	10 max	6 max	nsec	10% V_{DD} to 90% V_{DD} C_L=50pF
Time to Enable Disable			100 max	100 max	nsec	Tristate Output
Input Current		I_{IH} I_{IL}	10 max -150 max	10 max -150 max	µA µA	
Input Voltage		V_{IH} V_{IL}	2.2 min 0.8 max	2.2 min 0.8 max	V V	

TEST CIRCUIT (KXO-HC-C/KHO-HC-C)



CL=50pF max
(Inclusive of test jig and probe capacitance)

SHAPE OF OUTPUT WAVE (KXO-HC-C/KHO-HC-C)



Duty Cycle= $\frac{A}{A+B}$

PIN CONNECTION

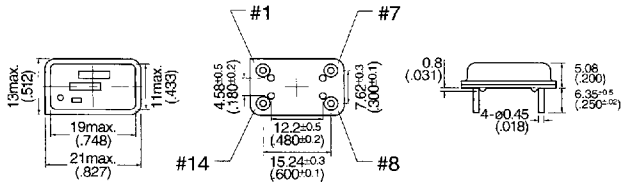
KXO	KHO	
1	1	N.C. or Control
7	4	Case /GND
8	5	Output
14	8	+5.0V D.C.

ENABLE/DISABLE FUNCTION CHART

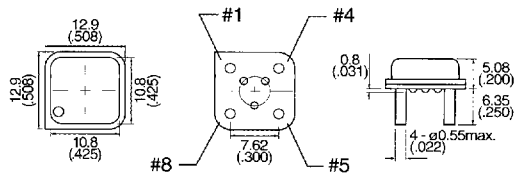
Pin 1	Pin 8
High or Open	Oscillation
Low	High Impedance

DIMENSIONS

KXO-HC



KHO-HC



Unit: mm (inch)