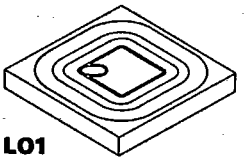
TAG SEMICONDUCTORS LTD

L0100BV – L0100MV LASCR'S

0.8 A 200–400 V

The L0100 series light activated silicon controlled rectifiers chips are high performance planar PNPN devices. These parts are intended for the high speed, high voltage requirements of solid state relay applications.



L01

Absolute Maximum Ratings $T_A = 25\,°C$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	**L0100BV**	V_{DRM}	200		V	Tj = −40 °C to 125 °C
	L0100DV	V_{RRM}	400		V	$R_{GK} = 1\,K\Omega$
	(L0100MV)		600		V	(Available on special request)
On-State Current		$I_{T(RMS)}$	1.0		A	All Conduction Angles $T_C = 85\,°C$
Average On-State Current		$I_{T(AV)}$	0.5		A	$T_C = 85\,°C$, Half Cycle, $\Theta = 180\,°C$
Nonrept. On-State Current		I_{TSM}	16.5		A	Half Cycle, 60 Hz $T_C = 85\,°C$
Nonrept. On-State Current		I_{TSM}	15		A	Half Cycle, 50 Hz $T_C = 85\,°C$
Fusing Current		I^2t	1.0		A^2s	t = 10 ms, Half Cycle
Peak Reverse Gate Voltage		V_{GRM}	8		V	$I_{GR} = 10\,\mu A$
Peak Gate Current		I_{GM}	1		A	10μs max.
Peak Gate Dissipation		P_{GM}	2		W	10μs max.
Gate Dissipation		$P_{G(AV)}$	0.1		W	20 ms max.
Operating Temperature		Tj	−40	125	°C	
Storage Temperature		T_{stg}	−40	125	°C	
Eutectic Die Attach Temp.		T_{attach}	390	420	°C	Au backing Al front (Bondable)
Case Temperature		T_C			°C	Temp. measured on substrate immediately adjacent to chip.

L01

Electrical Characteristics $T_A = 25\,°C$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}		200	μA	Tj = 125 °C, V_{DRM}, $R_{GK} = 1\,K\Omega$
Off-State Leakage Current	I_{RRM}		200	μA	Tj = 125 °C, V_{RRM}, $R_{GK} = 1\,K\Omega$
On-State Voltage	V_T		1.35	V	at $I_T = 1.0\,A$, Tj = 25 °C
On-State Threshold Voltage	$V_{T(TO)}$		1.0	V	Tj = 125 °C
On-State Slope Resistance	r_T		350	mΩ	Tj = 125 °C
Gate Trigger Voltage	V_{GT}		0.8	V	$V_D = 7\,V$
Holding Current	I_H		5	mA	$R_{GK} = 1\,K\Omega$
Latching Current	I_L		6	mA	$R_{GK} = 1\,K\Omega$
Critical Rate of Voltage Rise	dv/dt	20		V/μs	$V_D = .67 \times V_{DRM}$ $R_{GK} = 1\,K\Omega$ Tj = 125 °C
Critical Rate of Current Rise	di/dt	100		A/μs	$I_G = 1\,mA$ $di_G/dt = 4\,mA/\mu s$ Tj = 125 °C
Gate Controlled Delay Time	t_{gd}		500	ns	$I_G = 10\,mA$ $di_G/dt = 0.1\,A/\mu s$
Commutated Turn-Off Time	t_q		15	μs	$T_C = 85\,°C$ $V_D = .67 \times V_{DRM}$ $V_R = 35\,V$ $I_T = I_{T(AV)}$
Effective Trigger Irradiance	H_{ET}	70		mW/cm^2	GaAs source at 945 nm
Effective Trigger Irradiance	H_{ET}	210		mW/cm^2	Tungsten Source at 2870 K
Thermal Resistance junc. to case	$R_{\Theta jc}$		75	K/W	
Thermal Resistance junc. to amb.	$R_{\Theta ja}$		180	K/W	