DEVICES INCORPORATED

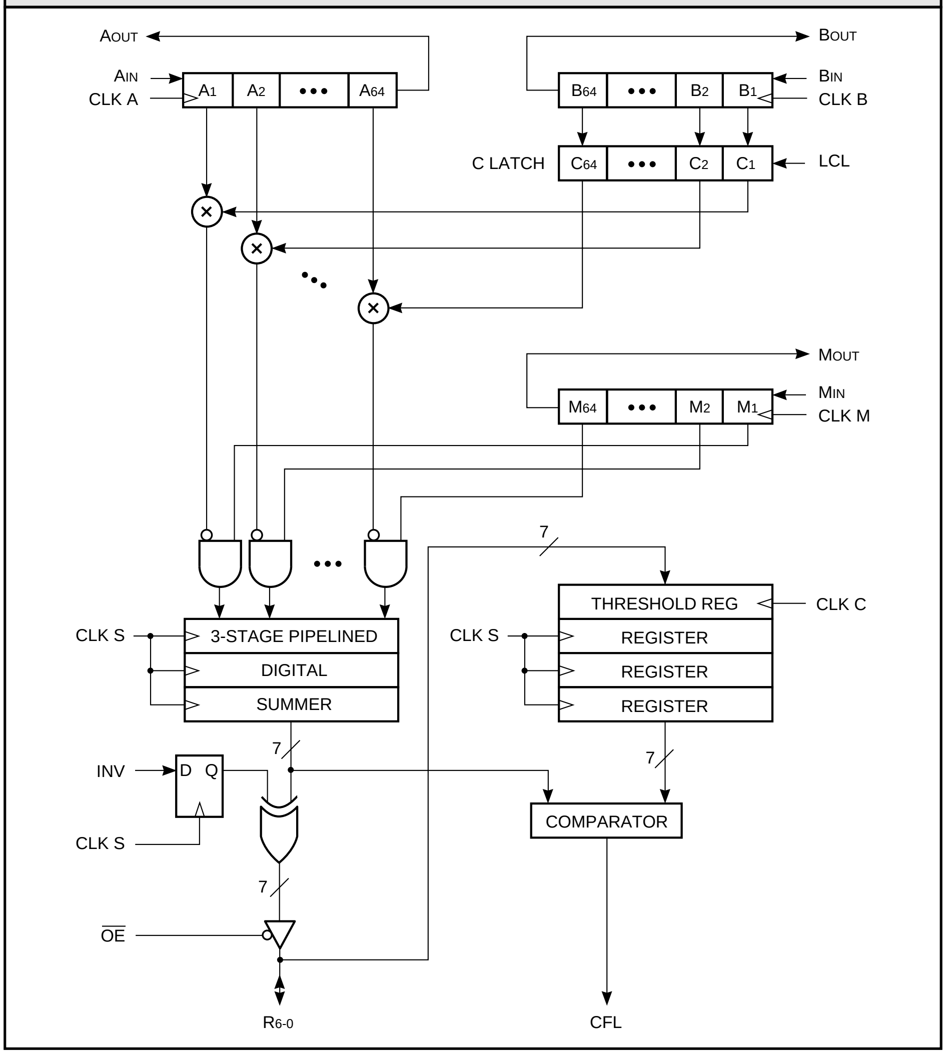
L10C23

64-bit Digital Correlator

FEATURES

- ❑ High Speed (50 MHz), Low Power (125 mW), CMOS 64-bit Digital Correlator
- ❑ Replaces Fairchild TDC1023/TMC2023
- ❑ Bit Can be Selectively Masked
- ❑ Three-State Outputs
- ❑ 24-pin PDIP

L10C23 BLOCK DIAGRAM



DESCRIPTION

The **L10C23** is a high speed CMOS 64-bit digital correlator. It is pin-for-pin equivalent to the Fairchild TDC1023/TMC2023. The L10C23 operates over the full military ambient temperature range using advanced CMOS technology.

The L10C23 produces the 7-bit correlation score of two input words of up to 64 bits, denoted A and B. The A and B inputs are serially shifted into two independently clocked 64-bit registers. The A register is clocked on the rising edge of CLK A, and the B register is clocked on the rising edge of CLK B.

The outputs of the B register drive a 64-bit transparent latch, denoted the C latch. The C latch is controlled by the LCL (Load C Latch) input. A HIGH level on the LCL input causes the C latch to be transparent, allowing the contents of the B register to be applied directly to the correlator array. When the LCL input is LOW, the data in the C latch is held, so that the B input may be loaded with a new correlation reference without affecting the current reference value stored in C.

Each bit in the A register is exclusive NOR'ed with the corresponding bit in the C latch, implementing a single bit multiplication at each bit position.

The mask register, denoted by M, is a third 64-bit register, which is serially loaded from the M input on the rising edge of CLK M. Bit positions in the M register which are set to zero mask the corresponding bits in the A and C registers from participating in the correlation score. This can be used to reduce the effective length of the correlation, or to correlate against only one channel of a bit-multiplexed datastream without deinterleaving the data.

The output of the masking process is a 64-bit vector which contains ones in the locations in which A and B data match, and which are unmasked (M register contains a '1'). This 64-bit vector is applied to a pipelined digital summer which calculates the total number of ones in the vector (the correlation score). The summer network contains three pipeline stages, which are clocked on the rising edge of CLK S. Calculation of a correlation score therefore requires three clock cycles, but a new result can be obtained on each cycle once the pipeline is filled.

Because a portion of the summer logic is located between the input registers and the first pipeline register, some timing restrictions exist between CLK S and CLK A, CLK B, or CLK M. CLK S may be tied to an input clock (usually CLK A) to obtain a continuously updated correlation score, delayed by three cycles from the data. Under this condition, CLK S may be skewed later than CLK A by no more than t_{SK} to assure that the A register outputs have not changed before the S clock occurs.

Alternatively, CLK S may be asyncronous to the input clocks, as long as data is stable at the pipeline register inputs prior to the CLK S rising edge. This condition can be met by assuring that CLK S occurs at least t_{PS} after the input clock.

The summer output represents a count of the number of matching positions in the input data streams. This 7-bit result can be inverted (one's complemented) by loading a '1' into the INV register.

Correlation values which exceed a predetermined threshold can be detected via the Threshold register and Comparator. The Threshold register is loaded with a 7-bit value via the R_{6-0} pins at the rising edge of CLK C and while $\overline{OE}$ is HIGH. To achieve synchronization with the digital summer, the Threshold register contents are fed into pipeline registers clocked by CLK S. The compare flag output (CFL) goes HIGH when the summer output is equal to or greater than the contents of the Threshold register.

Cascading the L10C23 devices for longer correlation lengths and more bits of reference or data precision is easily accomplished. The A, B, and M registers have serial outputs to directly drive the corresponding inputs of succeeding devices. The correlation scores of multiple devices in such a system should be added together to obtain the overall correlation score.

Correlation on data exceeding one bit of precision can be accomplished by first calculating single-bit correlation scores at each bit position, then adding the results after weighting them appropriately. Thus, one L10C23 would be used for each bit of precision in the data.

LOGIC Devices' L4C381 16-bit ALU can be used to assist in adding the outputs of several L10C23 correlators. When adding several 7-bit correlation scores, advantage can be taken of the fact that the sum of two 7-bit numbers will not exceed 8 bits. Thus the L4C381 can simultaneously perform two 7-bit additions. The first two operands are applied to A_{6-0} and B_{6-0}, with the result appearing on F_{7-0}. The second pair of operands are applied to A_{14-8} and B_{14-8}, with the result appearing in F_{15-8}. The unused inputs are tied to ground. If it can be guaranteed that at least one of the input scores will not reach its maximum value of 64, then this technique can also be applied in the second tier of adders. In this case, while the inputs have 8 bits of precision, the maximum value that their sum can assume is 255, which is expressable in 8 bits.

Alternatively, when performing long correlations on relatively slow datastreams, one L4C381 can be configured using its feedback mode to accumulate the correlation scores of a number of L10C23s. To accomplish this, the outputs of all the correlators are tied together on a three-state bus. Each one is sequentially enabled and clocked into the L4C381, which accumulates the total resulting score.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.75\text{ V} \le V_{CC} \le 5.25\text{ V}$
Active Operation, Military	–55°C to +125°C	$4.50\text{ V} \le V_{CC} \le 5.50\text{ V}$

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground $\le V_{IN} \le V_{CC}$ (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground $\le V_{OUT} \le V_{CC}$ (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		25	100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			0.5	mA

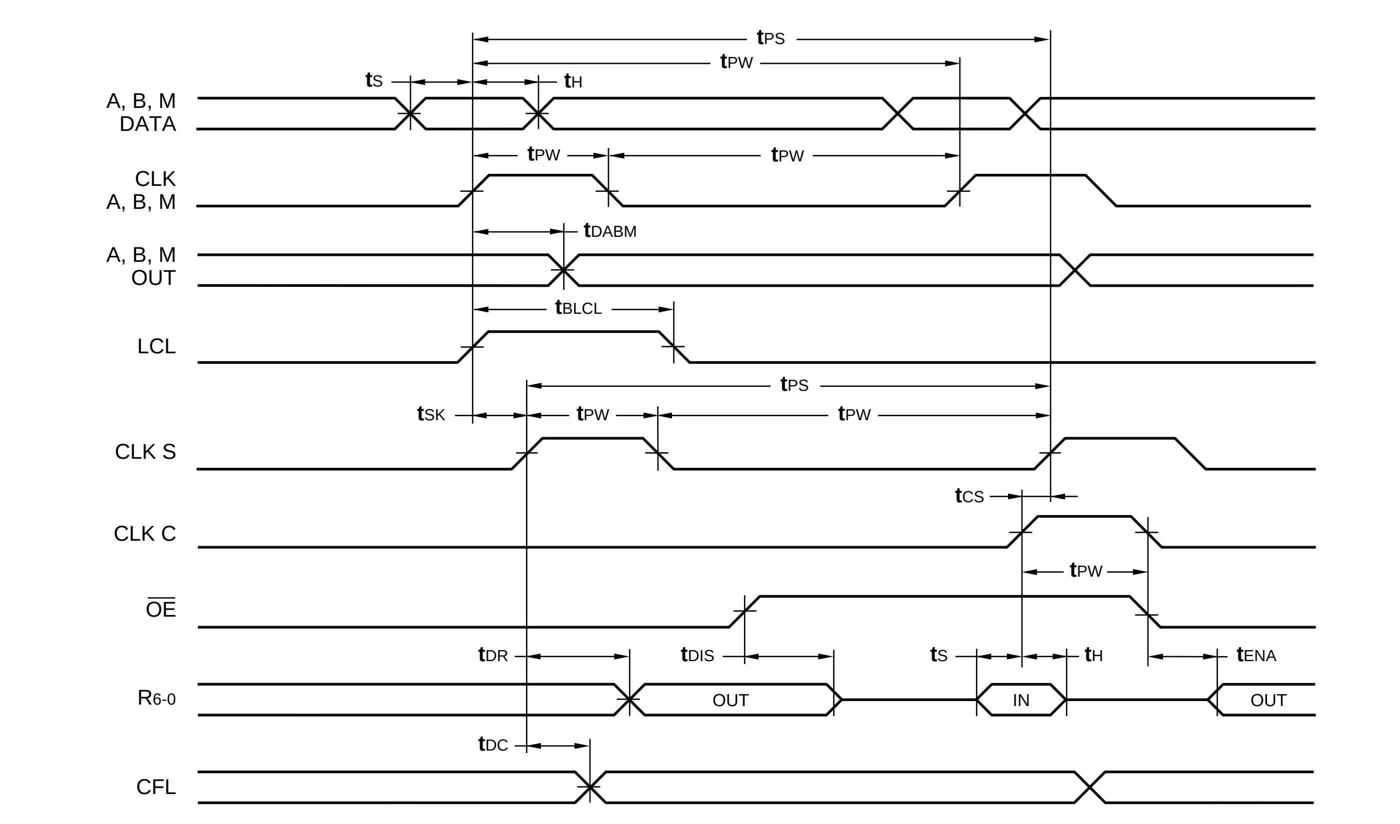
SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L10C23–					
		50*		30		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	50		28		20	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		12		8	
t_S	Input Setup Time	20		10		10	
t_H	Input Hold Time	0		0		0	
t_{BLCL}	B Clock to LCL Hold	20		12		8	
t_{CS}	C Clock to S Clock	50		28		20	
t_{DABM}	A, B, M Clock to A, B, M Out		25		20		18
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	50		28		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to $R_{6\text{-}0}$		35		30		22
t_{DC}	S Clock to CFL		25		20		18
t_{ENA}	Output Enable Time (Note 11)		30		18		16
t_{DIS}	Output Disable Time (Note 11)		35		16		14

*DISCONTINUED SPEED GRADE

SWITCHING WAVEFORMS



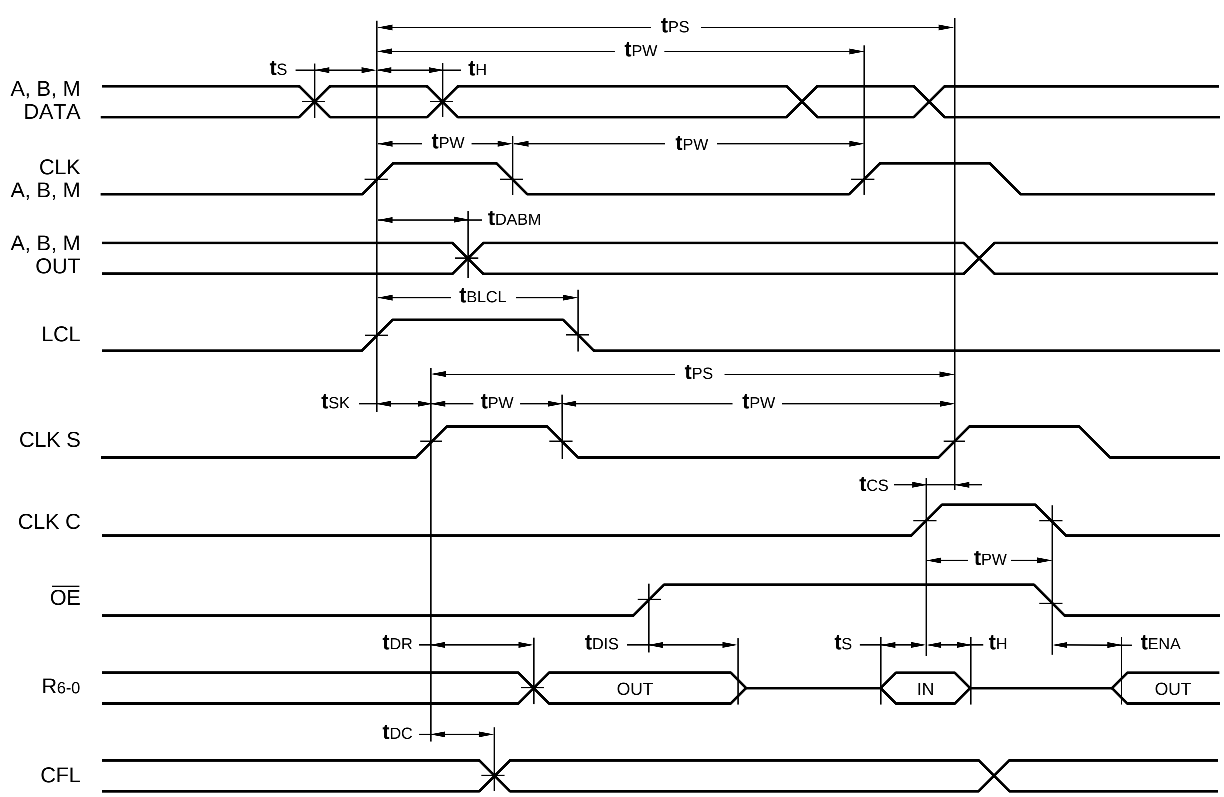
SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (-55°C to +125°C) *Notes 9, 10 (ns)*

		L10C23–					
		60*		35*		20*	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{PABM}	A, B, M Clock Period	58		33		20	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		14		8	
t_S	Input Setup Time	22		12		12	
t_H	Input Hold Time	0		0		0	
t_{BLCL}	B Clock to LCL Hold	20		14		8	
t_{CS}	C Clock to S Clock	58		33		20	
t_{DABM}	A, B, M Clock to A, B, M Out		30		23		20
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	58		33		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_{6-0}		40		35		27
t_{DC}	S Clock to CFL		30		23		18
t_{ENA}	Output Enable Time (Note 11)		35		20		18
t_{DIS}	Output Disable Time (Note 11)		40		18		16

*DISCONTINUED SPEED GRADE

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

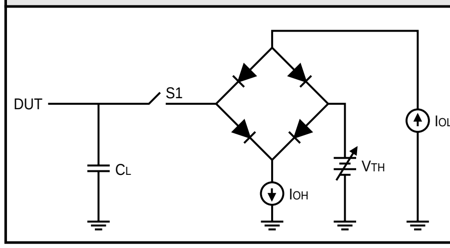
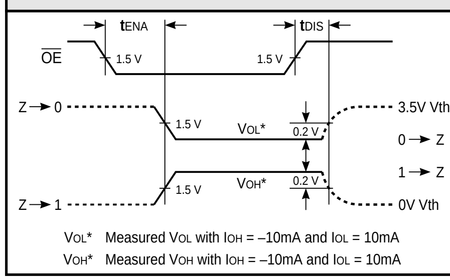
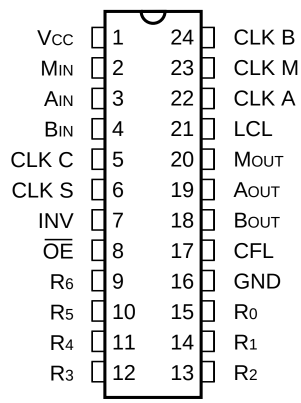


FIGURE B. THRESHOLD LEVELS

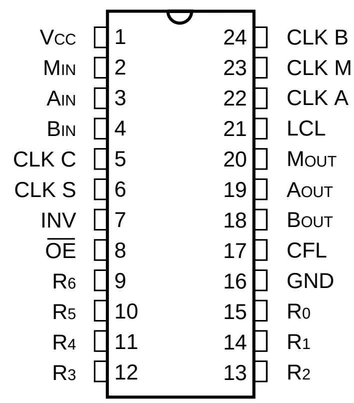


ORDERING INFORMATION

24-pin — 0.3" wide



24-pin — 0.6" wide



Speed	Plastic DIP (P2)	Plastic DIP (P1)	Ceramic DIP (C4)
	0°C to +70°C — Commercial Screening		
30 ns 20 ns	L10C23NC30 L10C23NC20	L10C23PC30 L10C23PC20	**Discontinued Package**
	–55°C to +125°C — Commercial Screening		
	–55°C to +125°C — MIL-STD-883 Compliant		