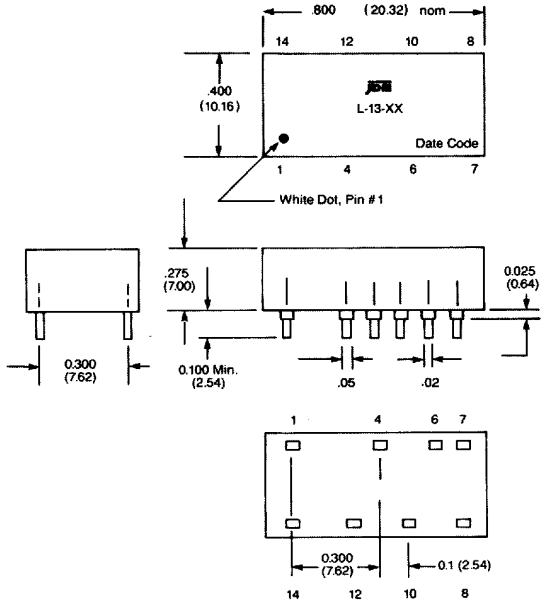
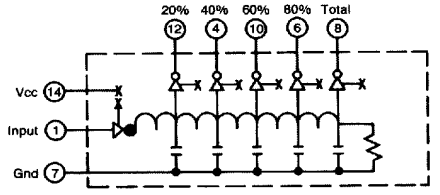
Delay Range 25 thru 1000 nsec

STYLE L-13 (14-pin outline)

5 equally-spaced taps

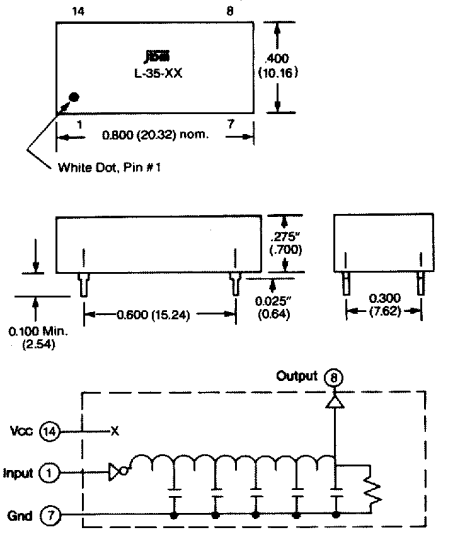




Delay Range 5 thru 1000 nsec

STYLE L-35 (14-pin outline)

Untapped



INPUT CONDITIONS

(See Page 2)

Operating Temp . . . . . 0°C to +70°C
Storage Temp . . . . . −55°C to +125°C
(All lines internally terminated)

I_{IH} Logic "1" Input Current . . . . 50μA Max.
I_{IL} Logic "0" Input Current . . . −2mA Max.
V_{OH} Logic "1" Voltage Out . . . . . 2.7V Min.
V_{OL} Logic "0" Voltage Out . . . . . 0.5V Max.

DRIVE CAPABILITIES

(TTL LOADS)

Logic "0" 10 Loads/Tap Max.
20 Loads/Unit Max.

Logic "1" 20 Loads/Unit Max.

Voltage Range: 4.75V to 5.25V
Supply Current: 75mA Max.

TOTAL DELAY (nsec±5%)	TAP INTERVALS (nsec*)	RISE TIME (ns MAX) (0.8 to 2.0V)	JBM P/N L-13-XXX
25	5 ± 3ns	2.0	L-13-50
30	6 ± 3ns	2.0	L-13-51
35	7 ± 3ns	2.0	L-13-52
40	8 ± 3ns	2.0	L-13-53
45	9 ± 3ns	2.0	L-13-54
50	10 ± 3ns	2.0	L-13-55
75	15 ± 3ns	2.0	L-13-56
100	20 ± 3ns	2.0	L-13-57
150	30 ± 3ns	2.5	L-13-58
200	40 ± 3ns	3.0	L-13-59
250	50 ± 3ns	3.0	L-13-60
300	60 ± 5%	3.5	L-13-250
350	70 ± 5%	3.5	L-13-251
400	80 ± 5%	4.0	L-13-252
450	90 ± 5%	4.0	L-13-253
500	100 ± 5%	4.0	L-13-254
600	120 ± 5%	4.5	L-13-255
700	140 ± 5%	4.5	L-13-256
750	150 ± 5%	4.5	L-13-257
800	160 ± 5%	5.0	L-13-258
900	180 ± 5%	5.0	L-13-259
1000	200 ± 5%	5.0	L-13-260

* 25n – 250ns TAP/TAP; 300ns – 1,000ns cumulative @ 25°C, 5.00VDC.

Delays may change 2% or 1ns for a respective 5% increase or decrease in supply voltage.

Consult factory for other delays, tolerances, and logic families.

TOTAL DELAY (nsec)	RISE TIME (ns MAX) (.8 to 2.0V)	JBM P/N L-35-XX
5 ± 1ns	2.0	L-35-00
7		L-35-01
10		L-35-02
15		L-35-03
20 ± 1ns		L-35-04
25 ± 5%		L-35-05
30		L-35-06
40		L-35-07
50		L-35-08
70		L-35-09
100		L-35-10
150	2.0	L-35-11
200	3.0	L-35-12
300	3.5	L-35-13
400	4.0	L-35-14
500	4.0	L-35-15
600	4.5	L-35-25
700	4.5	L-35-26
750	4.5	L-35-27
800	5.0	L-35-28
900	5.0	L-35-29
1000 ± 5%	5.0	L-35-30