CRYSTAL
Semiconductor Corporation

CS1232

Micromonitor

Features

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatic restart after power failure
- Monitors pushbutton for external reset
- Monitors microprocessor power supply to be within 5% or 10% of 5 V
- No discrete components needed
- 8-pin Mini-DIP or 16-pin SOIC
- Pin compatible with DS1232

General Description

The CS1232 is a monitor for microprocessors which checks program execution, power source quality, and external reset status.

The power status (V_{CC}) is monitored by a comparator and a precision temperature-compensated reference. Reset is forced active by an internal signal when V_{CC} goes out-of-tolerance. Reset signals stay active for a minimum for 250 ms after V_{CC} returns to an in-tolerance condition. This allows both power supply and processor to stabilize.

The pushbutton reset control input is debounced and the active reset minimum pulse width of 250 ms is guaranteed.

The internal watchdog timer forces the reset signals active if the strobe input is not driven low prior to time out. The CS1232 timer can be set to operate at time out settings of approximately 150ms, 600ms, and 1.2 seconds.

A surface mount 16-pin SOIC is available, as well as an 8-pin Plastic DIP.

ORDERING INFORMATION:

Model	Temp. Range	Package
CS1232-CP	0 °C to 70 °C	8-pin Plastic DIP
CS1232-IP	-40 °C to +85 °C	8-pin Plastic DIP
CS1232-CS	0 °C to 70 °C	16-pin SOIC
CS1232-IS	-40 °C to +85 °C	16-pin SOIC
Die Only:		
CS1232-YU		Unpackaged Die

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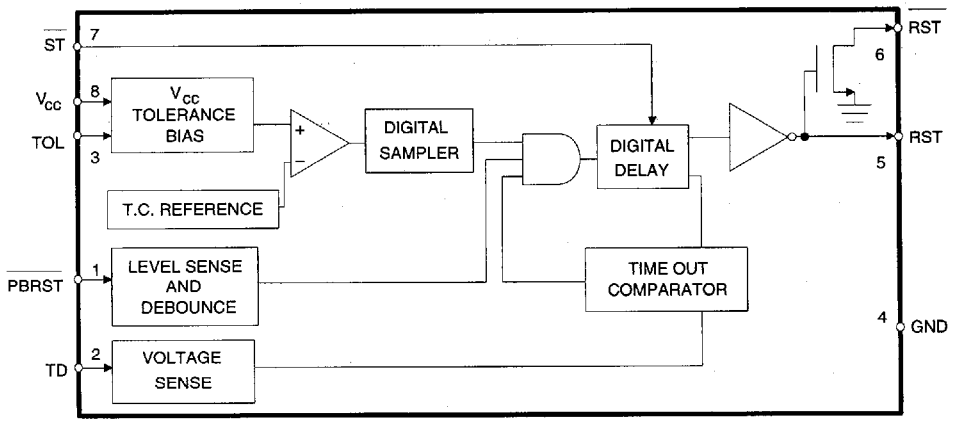

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ANALOG CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5 to 5.5V)

Parameter			Symbol	Min	Typ	Max	Units
V_{CC} Trip Point	(Note 1)	TOL = GND	V_{CCTP}	4.50	4.62	4.74	V
		TOL = V_{CC}	V_{CCTP}	4.25	4.37	4.49	V
Operating Current	(Note 2)		I_{CC}	-	0.4	2.0	mA

Notes: 1. All voltages referenced to ground.
2. Measured with outputs open.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
Operating Temperature	CS1232		0	-	+70	°C
	CS1232-I		-40	-	+85	°C
Supply voltage	(Note 1)	V_{CC}	4.5	5.0	5.5	V

DIGITAL CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5V to 5.5V)

Parameter		Symbol	Min	Typ	Max	Units
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	(Note 1)	V_{IH}	2.0	-	V_{CC}+0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	(Note 1)	V_{IL}	-0.3	-	+0.8	V
Output High Current at 2.4 V RST only		I_{OH}	-8.0	-10.0	-	mA
Output High Voltage at -500 µA RST only	(Note 3)	V_{OH}	V_{CC}-0.5	V_{CC}-0.1	-	V
Output Low Current at 0.4 V RST, $\overline{RST}$		I_{OL}	8.0	10.0	-	mA
Input Leakage	(Note 4)	I_{IL}	-1.0	-	+1.0	µA
Input Capacitance	T_A = 25°C	C_{IN}	-	-	5	pF
Output Capacitance	T_A = 25°C	C_{OUT}	-	-	7	pF

Notes: 3. On power-down, RST typically remains within 0.5V of V_{CC} (and $\overline{RST}$ typically remains within 0.5V of GND) until V_{CC} falls below 2.0V.
4. $\overline{PBRST}$ is internally pulled up to V_{CC} with a 100 kΩ resistor. TD is internally pulled up to V_{CC} with a 100 kΩ resistor and pulled down to ground with a 100 kΩ resistor.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

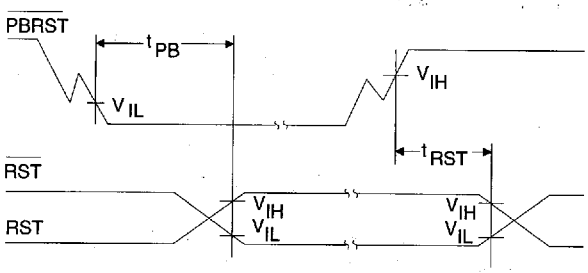
Parameter	Min	Typ	Max	Units
Voltage on Any Pin Relative to Ground	-1.0	-	+7.0	V
Input Current	-	-	±10	mA
Storage Temperature	-55	-	+125	°C
Soldering Temperature	260 °C for 10 sec			

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

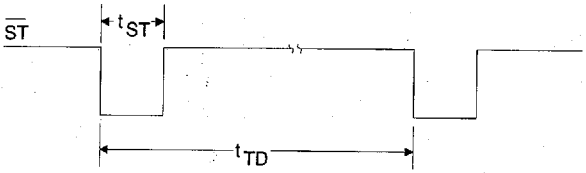
SWITCHING CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{PBRST}$ = V_{IL}	t_{PB}	-	20	-	ms
RESET Active Time	t_{RST}	250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	20	-	-	ns
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}	-	-	100	ns
V_{CC} Slew Rate from 4.75V - 4.25V	t_F	300	-	-	µs
V_{CC} Detect to RST and $\overline{RST}$ (Note 5)	t_{RPU}	250	610	1000	ms
V_{CC} Slew Rate from 4.25V - 4.75V	t_R	0	-	-	ns
$\overline{ST}$ Pulse Period (Note 6) TD pin at Ground	t_{TD}	50.0	150	250	ms
TD pin floating	t_{TD}	250	600	1000	ms
TD pin connected to V_{CC}	t_{TD}	400	1200	2000	ms

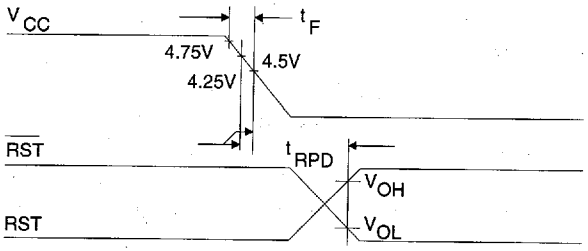
Note: 5. t_R = 5 µs
6. t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}.
7. $\overline{RST}$ is an N-channel open drain output.



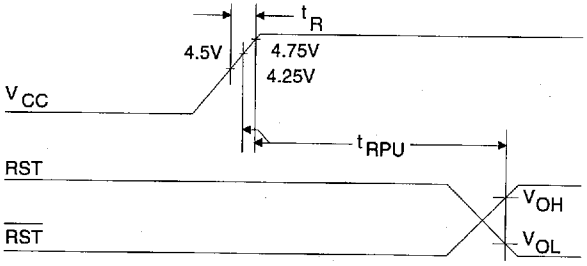
Timing Diagram—Pushbutton Reset



Timing Diagram—Strobe Input



Timing Diagram—Power Down



Timing Diagram—Power Up

POWER SUPPLY MONITOR

The CS1232 will detect out-of-tolerance power supplies for processor-based systems as well as warn of an impending power failure. The TOL digital input pin defines the threshold level for V_{CC}; when the V_{CC} level drops below the TOL defined level, the CS1232 asserts the signals RST and $\overline{RST}$. The threshold level is set to typically 4.37 V if TOL is connected to V_{CC}, and is set to typically 4.62 V if TOL is connected to GND. The processor is allowed to continue until the last possible moment that V_{CC} is valid. Upon return of power, RST and $\overline{RST}$ are active for 250 ms (minimum) to allow stabilization.

PUSHBUTTON RESET CONTROL

$\overline{PBRST}$ is normally connected to a reset pushbutton (see Figure 1). This active low signal is debounced and timed to generate signals of 250 ms (minimum) for RST and $\overline{RST}$. The delay begins when $\overline{PBRST}$ is released from from the low state. $\overline{PBRST}$ has an internal 100 kΩ pull-up resistor.

WATCHDOG TIMER

When RST and $\overline{RST}$ become inactive (normal CPU operation), the watchdog timer starts timing out, using the time set by TD. RST and $\overline{RST}$ are forced active when $\overline{ST}$ is not stimulated for this predetermined time. TD sets the time to be: 150 ms if TD is connected to ground, 600 ms is TD is not connected, or 1.2 seconds with TD connected to V_{CC}. RST and $\overline{RST}$ are driven active for 250 ms (minimum) if no high-to-low transition occurs on the $\overline{ST}$ input pin before time out. Microprocessor address signals, data signals, control signals, and output port bits can be used for the $\overline{ST}$ input pin. These signals cause the watchdog timer to be reset prior to time out indicating normal function of the microprocessor (see Figure 2).

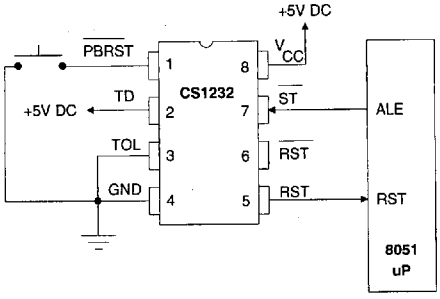


Figure 1. Pushbutton Reset

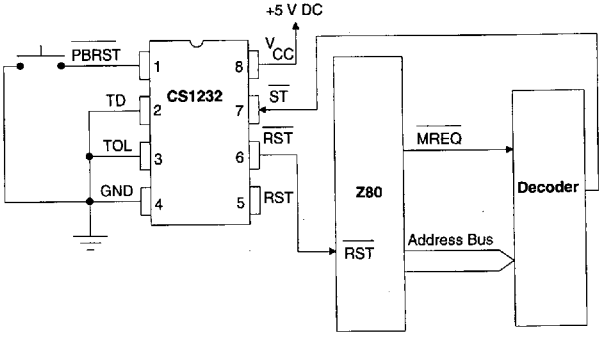


Figure 2. Watchdog Timer

PUSH BUTTON RESET INPUT	$\overline{\text{PBRST}}$	1	8	V_{CC}	+5 VOLT POWER
TIME DELAY SET	TD	2	7	$\overline{\text{ST}}$	STROBE INPUT
SELECTS V_{CC} DETECT LEVEL	TOL	3	6	$\overline{\text{RST}}$	RESET OUTPUT (Active Low, Open Drain)
GROUND	GND	4	5	RST	RESET OUTPUT (Active High)

NO CONNECTION	NC	1	16	NC	NO CONNECT
PUSH BUTTON RESET INPUT	$\overline{\text{PBRST}}$	2	15	V_{CC}	+5 VOLT POWER
NO CONNECT	NC	3	14	NC	NO CONNECTION
TIME DELAY SET	TD	4	13	$\overline{\text{ST}}$	STROBE INPUT
NO CONNECT	NC	5	12	NC	NO CONNECT
SELECTS V_{CC} DETECT LEVEL	TOL	6	11	$\overline{\text{RST}}$	RESET OUTPUT (Active Low, Open Drain)
NO CONNECT	NC	7	10	NC	NO CONNECT
GROUND	GND	8	9	RST	RESET OUTPUT (Active High)

DIE INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

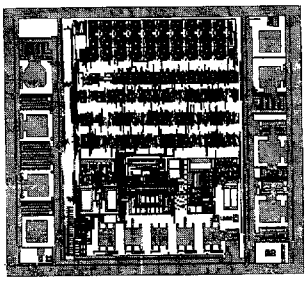
1. Die size: 0.061" by 0.069" (± 0.002").

2. The die is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to V_{CC}.

3. Die thickness shall be 0.0175" ± 0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 100.

5. The cavity dimensions for each die within the waffle pack are 0.080" by 0.080" (Waffle Pack Type H20-080).

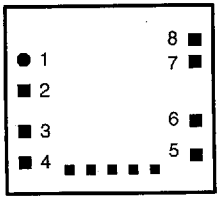


6. The CS1232-YU requires no particular bonding sequence.

7. Each pin of the CS1232 has ESD and latch-up protection circuitry.

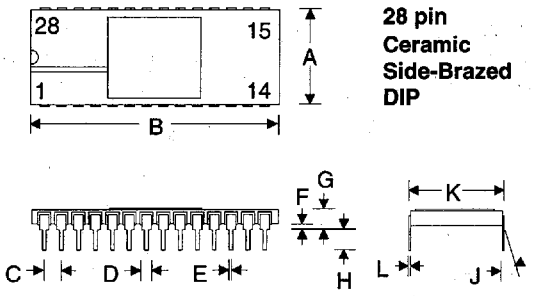
8. Technical constraints limit the viability of accurate performance measurements of precision analog IC's at wafer probe. Although high yield to the limits listed in the specification tables is anticipated, no guarantee is given for unpackaged die product.

CS1232-YU Bonding Diagram



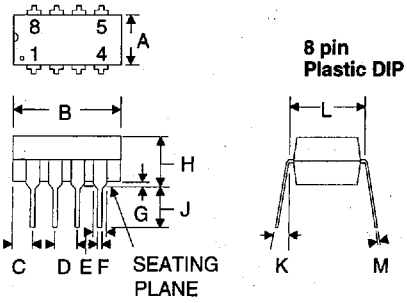
1	-	$\overline{\text{PBRST}}$	5	-	RST
2	-	TD	6	-	$\overline{\text{RST}}$
3	-	TOL	7	-	$\overline{\text{ST}}$
4	-	GND	8	-	VCC

MECHANICAL DATA



28 pin Ceramic Side-Brazed DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012

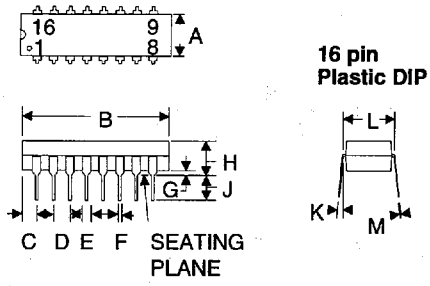


8 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

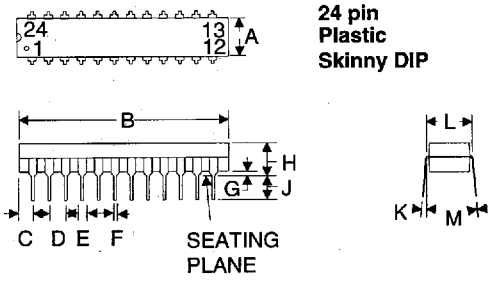


16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:

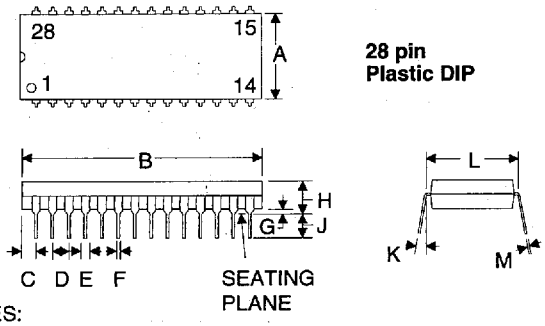
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

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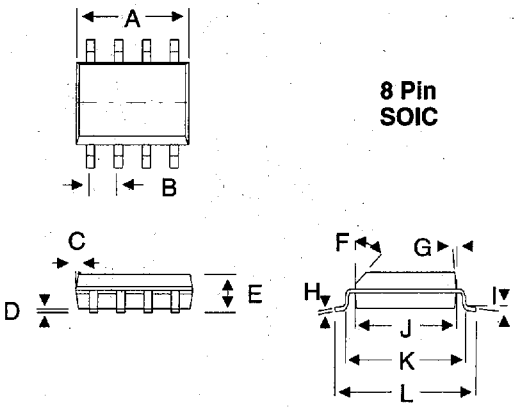
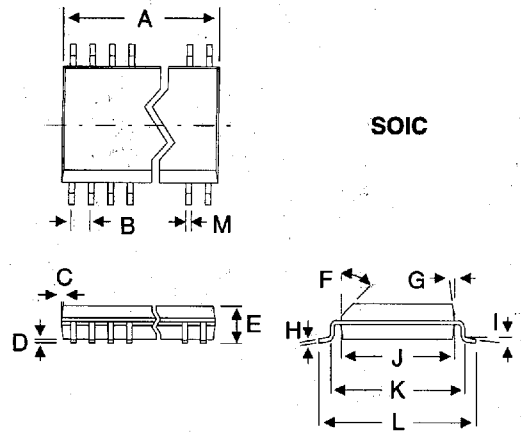


8 Pin
SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312

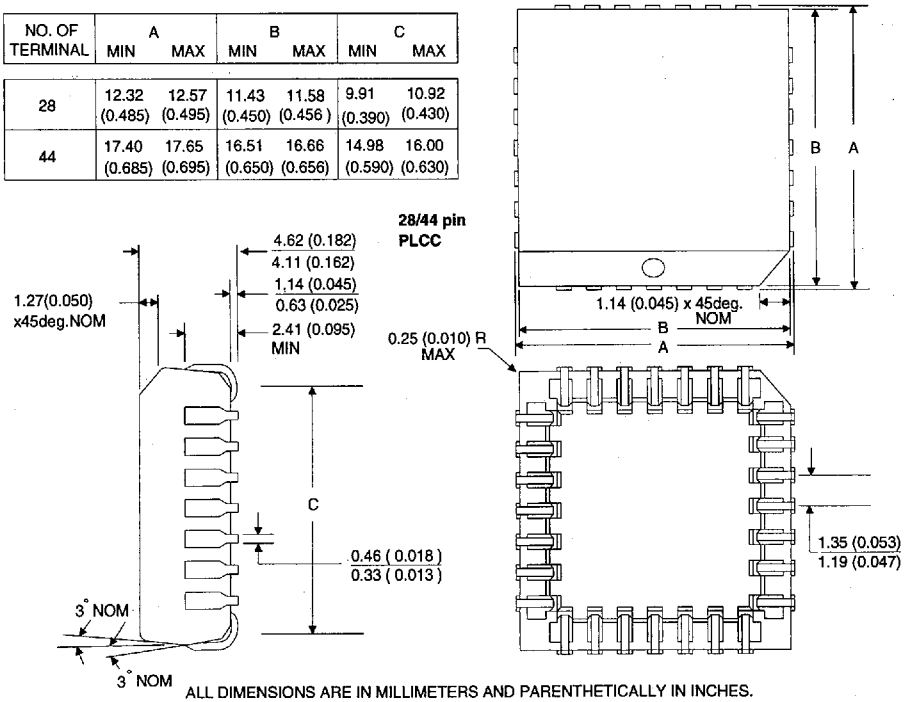


SOIC

pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

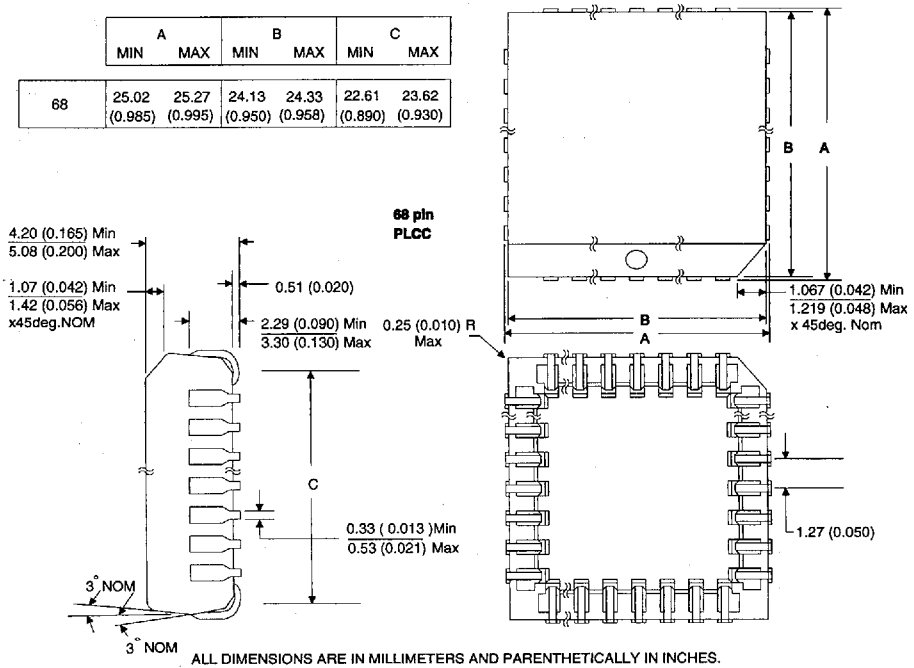
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

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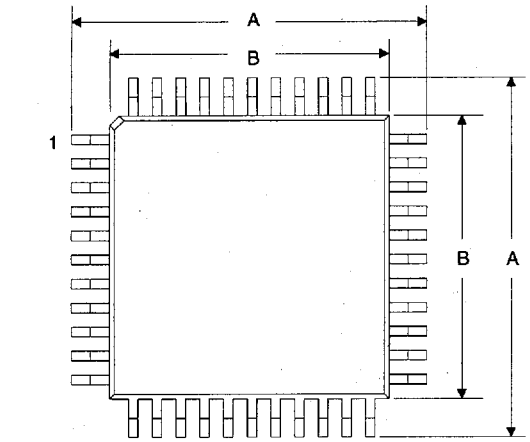
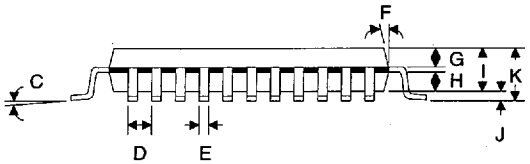
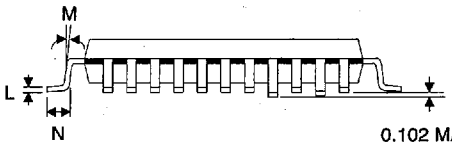
44 PIN QUAD FLATPACK

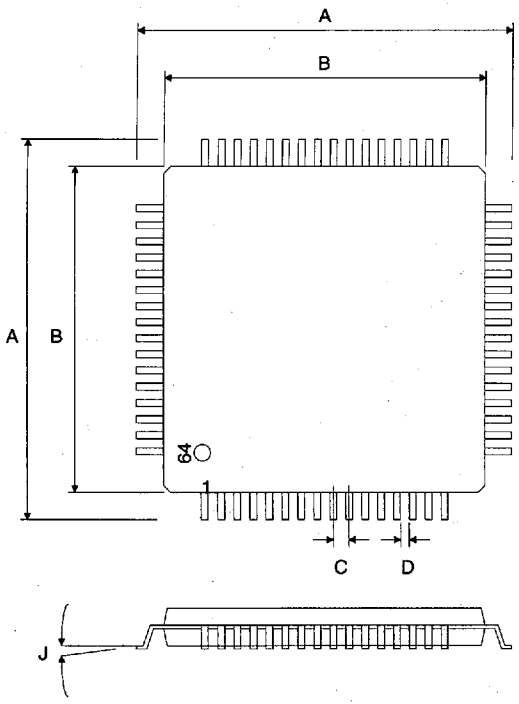


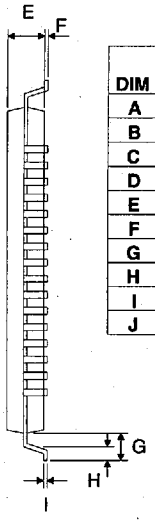
	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026





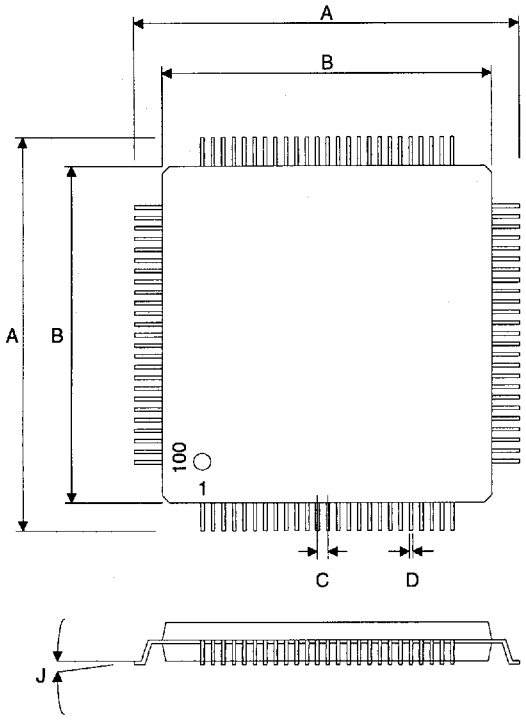
0.102 MAX
Lead Coplanarity

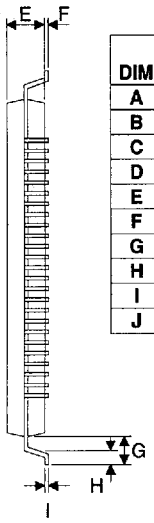




64 Pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

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