National Semiconductor

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LP38501/3-ADJ, LP38501A/3A-ADJ
3A FlexCap Low Dropout Linear Regulator for 2.7V to 5.5V Inputs

General Description

National's FlexCap LDO's feature unique compensation that allows the use of any type of output capacitor with no limits on minimum or maximum ESR. The LP38501/3 series of low-dropout linear regulators operates from a +2.7V to +5.5V input supply. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. Developed on a CMOS process, (utilizing a PMOS pass transistor), the LP38501/3 has low quiescent current that changes little with load current.

Ground Pin Current: Typically 2 mA at 3A load current.

Disable Mode: Typically 25 nA quiescent current when the Enable pin is pulled low.

Simplified Compensation: Stable with any type of output capacitor, regardless of ESR.

Precision Output: "A" grade versions available with 1.5% V_{ADJ} tolerance (25°C) and 3% over line, load and temperature.

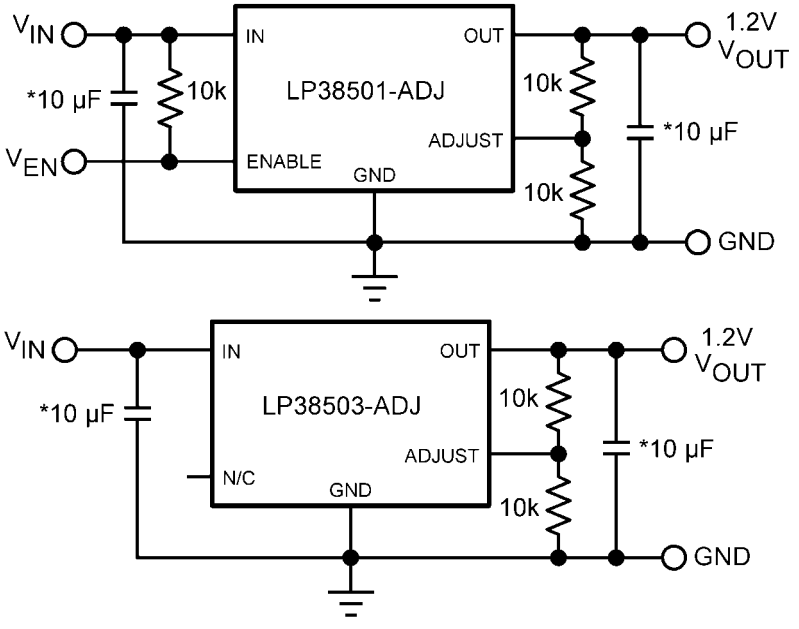
Features

- FlexCap: Stable with ceramic, tantalum, or aluminum capacitors
- Stable with 10 µF input/output capacitor
- Adjustable output voltage from 0.6V to 5V
- Low ground pin current
- 25 nA quiescent current in shutdown mode
- Guaranteed output current of 3A
- Available in TO-263, TO-263 THIN packages
- Guaranteed V_{ADJ} accuracy of ±1.5% @ 25°C (A Grade)
- Guaranteed V_{ADJ} accuracy of ±3.5% @ 25°C (STD)
- Over-Temperature and Over-Current protection
- –40°C to +125°C operating T_J range
- Enable pin (LP38501)

Applications

- ASIC Power Supplies In:
  Printers, Graphics Cards, DVD Players
  Set Top Boxes, Copiers, Routers
- DSP and FPGA Power Supplies
- SMPS Regulator
- Conversion from 3.3V or 5V Rail

Typical Application Circuit



*Minimum capacitance required (see Application Information)

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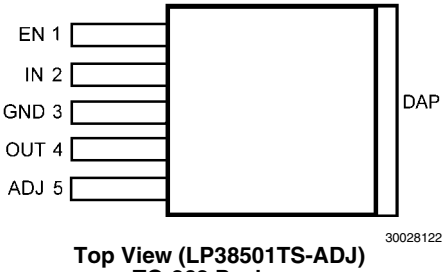
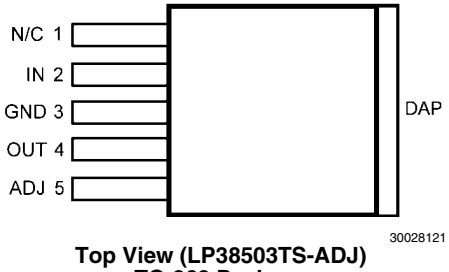
Connection Diagrams for TO-263 (TS) Package

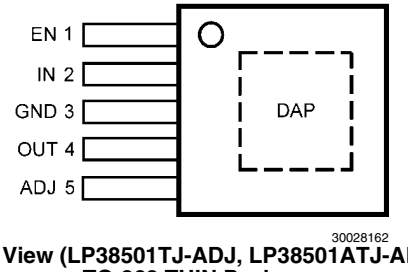


Top View (LP38501TS-ADJ)
TO-263 Package

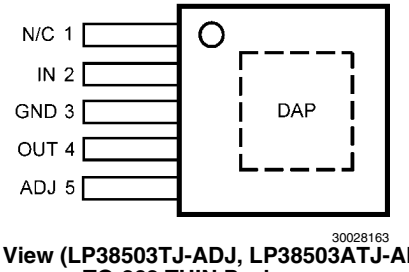


Top View (LP38503TS-ADJ)
TO-263 Package

Connection Diagrams for TO-263 THIN (TJ) Package



Top View (LP38501TJ-ADJ, LP38501ATJ-ADJ)
TO-263 THIN Package



Top View (LP38503TJ-ADJ, LP38503ATJ-ADJ)
TO-263 THIN Package

Pin Descriptions for TO-263 (TS) and TO-263 THIN (TJ) Packages

Pin #	Designation	Function
1	EN	Enable (LP38501 only). Pull high to enable the output, low to disable the output. This pin has no internal bias and must be either tied to the input voltage, or actively driven.
	N/C	In the LP38503, this pin has no internal connections. It can be left floating or used for trace routing.
2	IN	Input Supply Pin
3	GND	Ground
4	OUT	Regulated Output Voltage Pin
5	ADJ	Sets output voltage
DAP	DAP	The DAP is used as a thermal connection to remove heat from the device to the circuit board copper clad area which acts as the heatsink. The DAP is electrically connected to the backside of the die. The DAP must be connected to ground potential, but can not be used as the only ground connection.

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Number	Package Type	Package Marking	Supplied As:
ADJ	LP38501TSX-ADJ	TO-263	LP38501TS-ADJ	Tape and Reel of 500 Units
	LP38501TS-ADJ		LP38501TS-ADJ	Rail of 45 Units
	LP38503TSX-ADJ		LP38503TS-ADJ	Tape and Reel of 500 Units
	LP38503TS-ADJ		LP38503TS-ADJ	Rail of 45 Units
ADJ	LP38501TJ-ADJ	TO-263 THIN	LP38501TJ-ADJ	Tape and Reel of 1000 Units
	LP38503TJ-ADJ		LP38503TJ-ADJ	Tape and Reel of 1000 Units
	LP38501ATJ-ADJ		LP38501ATJ-AD	Tape and Reel of 1000 Units
	LP38503ATJ-ADJ		LP38503ATJ-AD	Tape and Reel of 1000 Units

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 5 sec.)	260°C
ESD Rating (Note 2)	±2 kV
Power Dissipation(Note 3)	Internally Limited
Input Pin Voltage (Survival)	−0.3V to +6.0V
Enable Pin Voltage (Survival)	−0.3V to +6.0V
Output Pin Voltage (Survival)	−0.3V to +6.0V
I_{OUT}(Survival)	Internally Limited

Operating Ratings (Note 1)

Input Supply Voltage	2.7V to 5.5V
Enable Input Voltage	0.0V to 5.5V
Output Current (DC)	0 to 3A
Junction Temperature(Note 3)	−40°C to +125°C
V_{OUT}	0.6V to 5V

Electrical Characteristics LP38501/3–ADJ

Unless otherwise specified: V_{IN} = 3.3V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = V_{IN}, V_{OUT} = 1.8V. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADJ}	Adjust Pin Voltage (Note 6)	2.7V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 3A	0.584 **0.575**	0.605	0.626 **0.635**	V
V_{ADJ}	Adjust Pin Voltage (Note 6) "A" GRADE	2.7V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 3A	0.596 **0.587**	0.605	0.614 **0.623**	V
I_{ADJ}	Adjust Pin Bias Current	2.7V ≤ V_{IN} ≤ 5.5V		50	**750**	nA
V_{DO}	Dropout Voltage (Note 7)	I_{OUT} = 3A		420	550 **665**	mV
$\Delta V_{OUT}/\Delta V_{IN}$	Output Voltage Line Regulation (Notes 4, 6)	2.7V ≤ V_{IN} ≤ 5.5V	—	0.04 **0.05**	—	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (Notes 5, 6)	10 mA ≤ I_{OUT} ≤ 3A	—	0.12 **0.24**	—	%/A
I_{GND}	Ground Pin Current In Normal Operation Mode	10 mA ≤ I_{OUT} ≤ 3A	—	2	4 **5**	mA
$I_{DISABLED}$	Ground Pin Current	V_{EN} < $V_{IL(EN)}$	—	0.025	0.125 **15**	µA
$I_{OUT(PK)}$	Peak Output Current	V_{OUT} ≥ $V_{OUT(NOM)}$ - 5%		6		A
I_{SC}	Short Circuit Current	V_{OUT} = 0V	**3.5**	6		A
Enable Input (LP38501 Only)						
$V_{IH(EN)}$	Enable Logic High	V_{OUT} = ON	**1.4**	—	—	V
$V_{IL(EN)}$	Enable Logic Low	V_{OUT} = OFF	—	—	**0.65**	
$t_{d(off)}$	Turn-off delay	Time from V_{EN} < $V_{IL(EN)}$ to V_{OUT} = OFF I_{LOAD} = 3A	—	25	—	µs
$t_{d(on)}$	Turn-on delay	Time from V_{EN} >$V_{IH(EN)}$ to V_{OUT} = ON I_{LOAD} = 3A	—	25	—	
$I_{IH(EN)}$	Enable Pin High Current	V_{EN} = V_{IN}	—	35	—	nA
$I_{IL(EN)}$	Enable Pin Low Current	V_{EN} = 0V	—	35	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AC Parameters						
PSRR	Ripple Rejection	V_{IN} = 3.0V, I_{OUT} = 3A f = 120Hz	—	58	—	dB
		V_{IN} = 3.0V, I_{OUT} = 3A f = 1 kHz	—	56	—	
$\rho_{n(l/f)}$	Output Noise Density	f = 120Hz, C_{OUT} = 10 µF CER	—	1.0	—	µV/$\sqrt{Hz}$
e_n	Output Noise Voltage	BW = 100Hz – 100kHz C_{OUT} = 10 µF CER	—	100	—	µV (rms)
Thermal Characteristics						
T_{SD}	Thermal Shutdown	T_J rising	—	170	—	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	T_J falling from T_{SD}	—	10	—	
θ_{J-A}	Thermal Resistance Junction to Ambient	TO-263, TO-263 THIN(Note 8) 1 sq. in. copper		37		°C/W
θ_{J-C}	Thermal Resistance Junction to Case	TO-263, TO-263 THIN	—	5	—	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 3: Operating junction temperature must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}). See Application Information.

Note 4: Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the voltage at the input.

Note 5: Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in the load current at the output.

Note 6: The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

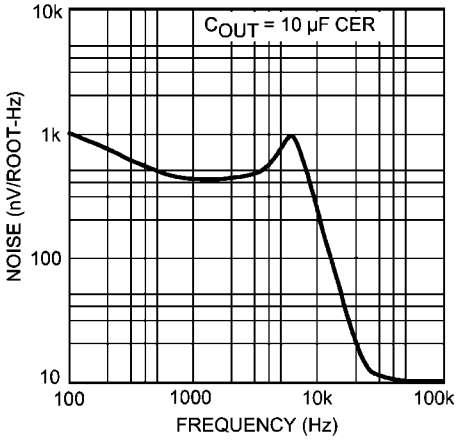
Note 7: Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. For any output voltage less than 2.5V, the minimum V_{IN} operating voltage is the limiting factor.

Note 8: The value of θ_{JA} for the TO-263 (TS) package and TO-263 THIN (TJ) package can range from approximately 30 to 60°C/W depending on the amount of PCB copper dedicated to heat transfer (See Application Information).

Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.7V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA, V_{OUT} = 1.8V

Noise Density



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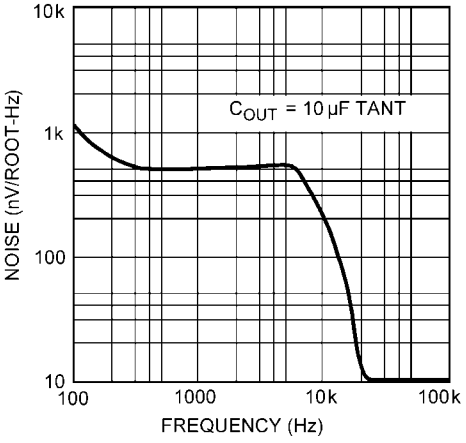
Noise Density



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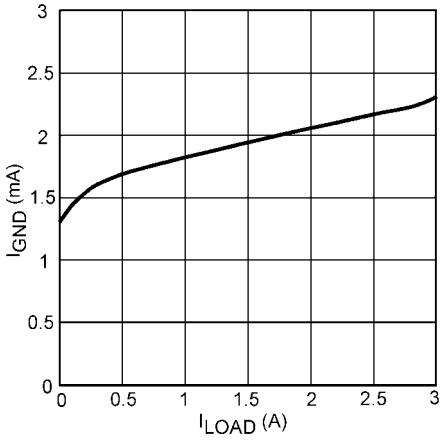
I_{GND} vs Load Current



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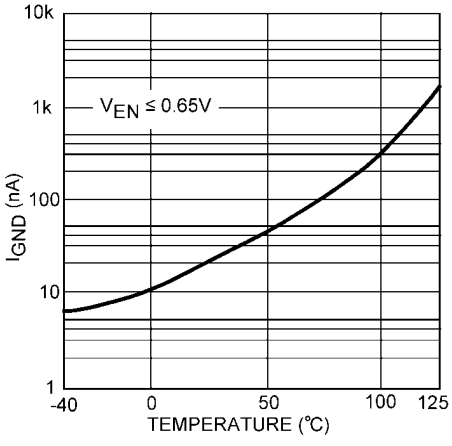
$I_{GND(OFF)}$ vs Temperature



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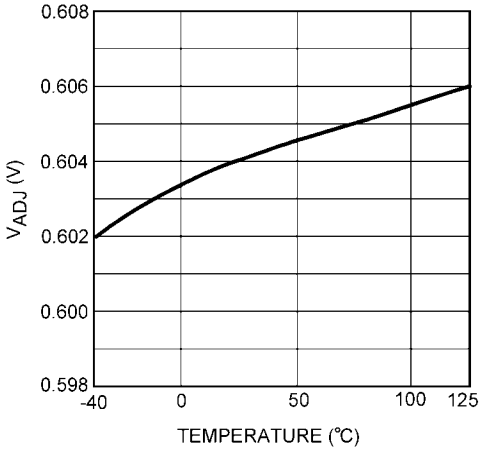
V_{ADJ} vs Temperature



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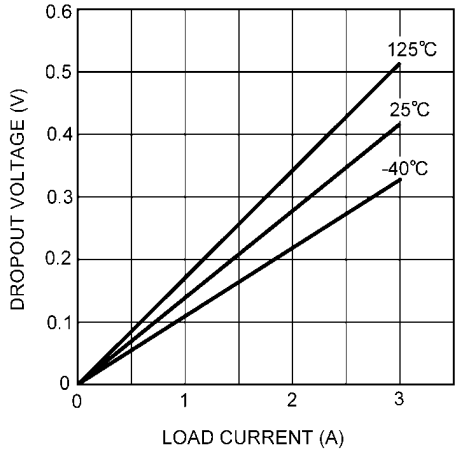
Dropout Voltage vs Load Current



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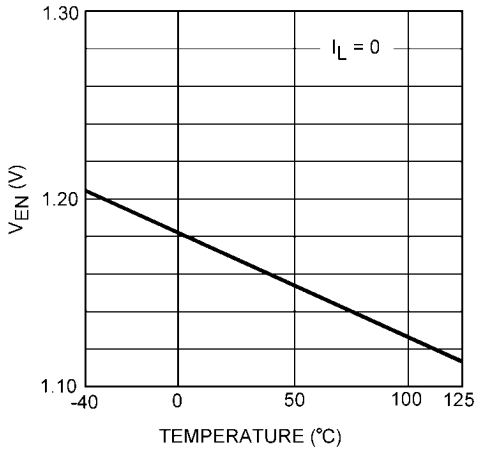
V_{EN} vs Temperature



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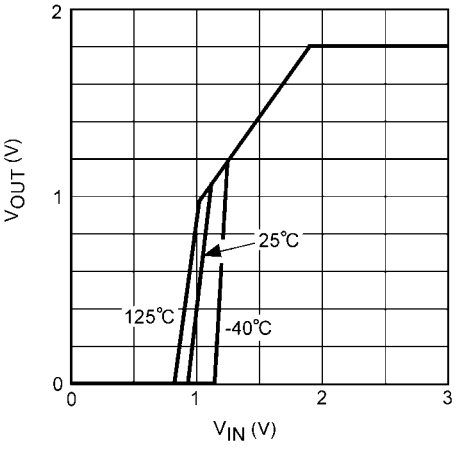
Turn-on Characteristics



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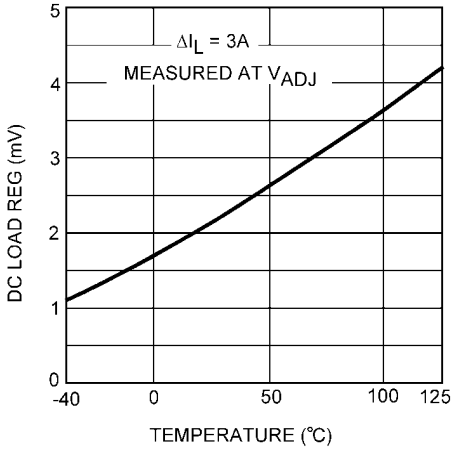
Load Regulation vs Temperature



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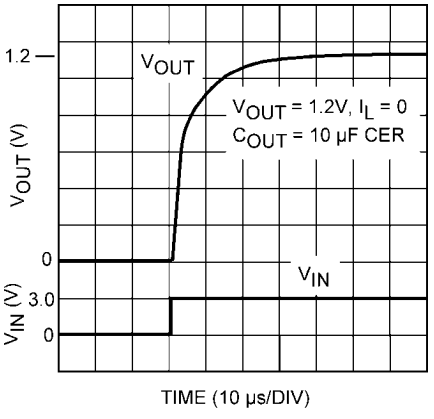
Turn-on Time



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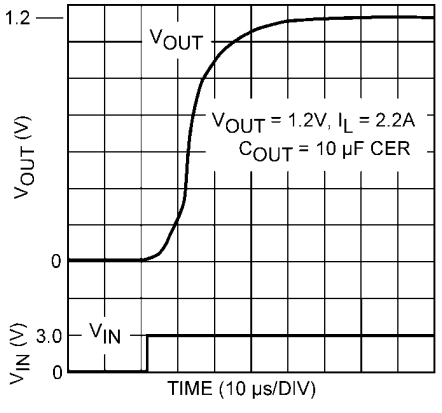
Turn-on Time



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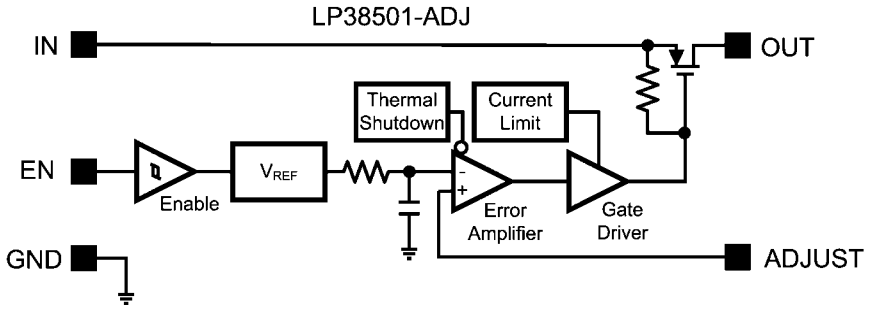
Block Diagrams

LP38501-ADJ Block Diagram



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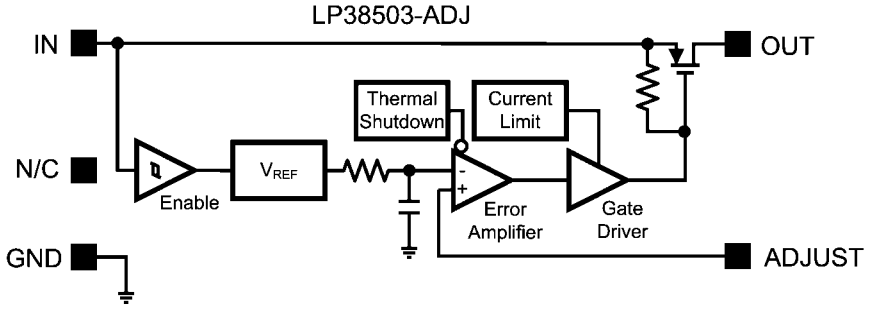
LP38503-ADJ Block Diagram



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Application Information

EXTERNAL CAPACITORS

The LP3850X requires that at least 10 µF (±20%) capacitors be used at the input and output pins located within one cm of the IC. Larger capacitors may be used without limit on size for both C_{IN} and C_{OUT}. Capacitor tolerances such as temperature variation and voltage loading effects must be considered when selecting capacitors to ensure that they will provide the minimum required amount of capacitance under all operating conditions for the application.

In general, ceramic capacitors are best for noise bypassing and transient response because of their ultra low ESR. It must be noted that if ceramics are used, only the types with X5R or X7R dielectric ratings should be used (never Z5U or Y5F). Capacitors which have the Z5U or Y5F characteristics will see a drop in capacitance of as much as 50% if their temperature increases from 25°C to 85°C. In addition, the capacitance drops significantly with applied voltage: a typical Z5U or Y5F capacitor can lose as much as 60% of it's rated capacitance if only half of the rated voltage is applied to it. For these reasons, only X5R and X7R ceramics should be used.

INPUT CAPACITOR

All linear regulators can be affected by the source impedance of the voltage which is connected to the input. If the source impedance is too high, the reactive component of the source may affect the control loop's phase margin. **To ensure proper loop operation, the ESR of the capacitor used for C_{IN} must not exceed 0.5 Ohms**. Any good quality ceramic capacitor will meet this requirement, as well as many good quality tantalums. Aluminum electrolytic capacitors may also work, but can possibly have an ESR which increases significantly at cold temperatures. If the ESR of the input capacitor may exceed 0.5 Ohms, it is recommended that a 2.2 µF ceramic capacitor be used in parallel, as this will assure stable loop operation.

OUTPUT CAPACITOR

Any type of capacitor may be used for C_{OUT}, with no limitations on minimum or maximum ESR, as long as the minimum amount of capacitance is present. The amount of capacitance can be increased without limit. Increasing the size of C_{OUT} typically will give improved load transient response.

SETTING THE OUTPUT VOLTAGE

The output voltage of the LP38501/3-ADJ can be set to any value between 0.6V and 5V using two external resistors shown as R1 and R2 in *Figure 1*.

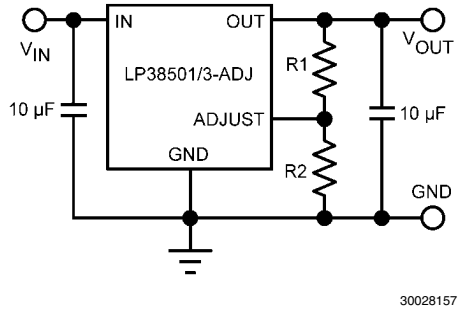


FIGURE 1.

The value of R2 should always be less than or equal to 10 kΩ for good loop compensation. R1 can be selected for a given V_{OUT} using the following formula:

$$V_{OUT} = V_{ADJ} (1 + R1/R2) + I_{ADJ} (R1)$$

Where V_{ADJ} is the adjust pin voltage and I_{ADJ} is the bias current flowing into the adjust pin.

STABILITY AND PHASE MARGIN

Any regulator which operates using a feedback loop must be compensated in such a way as to ensure adequate phase margin, which is defined as the difference between the phase shift and -180 degrees at the frequency where the loop gain crosses unity (0 dB). For most LDO regulators, the ESR of the output capacitor is required to create a zero to add enough phase lead to ensure stable operation. The LP38501 has a unique internal compensation circuit which maintains phase margin regardless of the ESR of the output capacitor, so any type of capacitor may be used.

Figure 2 shows the gain/phase plot of the LP38501-ADJ with an output of 1.2V, 10 µF ceramic output capacitor, delivering 2A of load current. It can be seen that the unity-gain crossover occurs at 300 kHz, and the phase margin is about 40° (which is very stable).

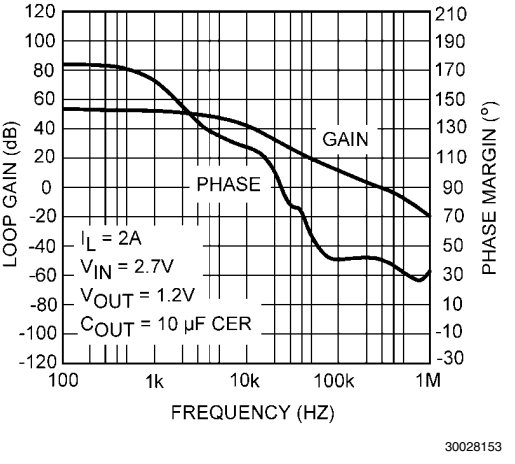


FIGURE 2. Gain-Bandwidth Plot for 2A Load

Figure 3 shows the gain and phase with no external load. In this case, the only load is provided by the gain setting resistors (about 12 kΩ total in this test). It is immediately obvious that the unity-gain frequency is significantly lower (dropping to about 500 Hz), at which point the phase margin is 125°.

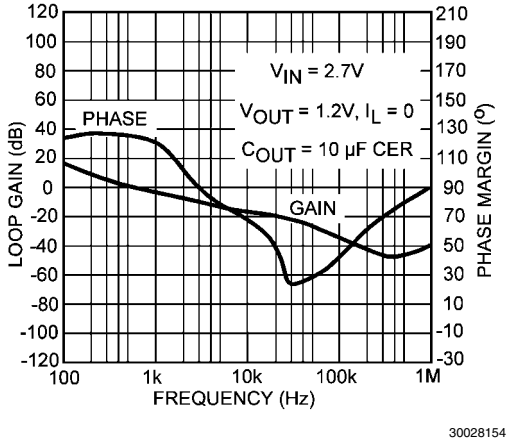


FIGURE 3. Gain-Bandwidth Plot for No Load

The reduction in unity-gain bandwidth as load current is reduced is normal for any LDO regulator using a P-FET or PNP pass transistor, because they have a pole in the loop gain function given by:

$$F_P = \frac{1}{2 \times \pi \times R_L \times C_{OUT}}$$

This illustrates how the pole goes to the highest frequency when R_L is minimum value (maximum load current). In general, LDO's have maximum bandwidth (and lowest phase margin) at full load current. In the case of the LP38501, it can be seen that it has good phase margin even when using ceramic capacitors with ESR values of only a few milli Ohms.

LOAD TRANSIENT RESPONSE

Load transient response is defined as the change in regulated output voltage which occurs as a result of a change in load current. Many applications have loads which vary, and the control loop of the voltage regulator must adjust the current in the pass FET transistor in response to load current changes. For this reason, regulators with wider bandwidths often have better transient response.

The LP38501 employs an internal feedforward design which makes the load transient response much faster than would be predicted simply by loop speed: this feedforward means any voltage changes appearing on the output are coupled through to the high-speed driver used to control the gate of the pass FET along a signal path using very fast FET devices. Because of this, the pass transistor's current can change very quickly.

Figure 4 shows the output transient response resulting from a change in load current of 0.1A – 3A, and then 3A – 0.1A with a load current slew rate of 500 mA/µs. As shown in the plots, the resulting change in output voltage is only about 40 mV (peak), which is just slightly over 2% for the 1.8V output used for this test. This is excellent performance for such a small output capacitor.

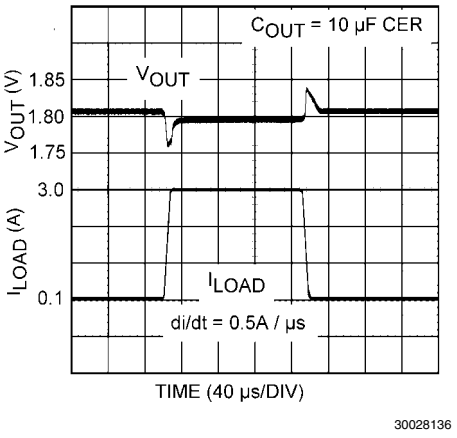


FIGURE 4. Load Transient Response: 10 µF Ceramic, 0.5A/µs di/dt

When the load current changes much more quickly, the output voltage will show more change because the loop and internal feedforward circuitry are not able to react as fast as the load changes. In such cases, it is the output capacitor which must supply load current during the transition until the loop responds and changes the pass transistor's drive to deliver the new value of load current. As an example, the slew rate of the load current will be increased to 75A/µs and the same test will be performed. In *Figure 5*, it can be seen that the peak excursion of the output voltage during the transient has now increased to about 200 mV, which is just slightly over 11% for the 1.8V output.

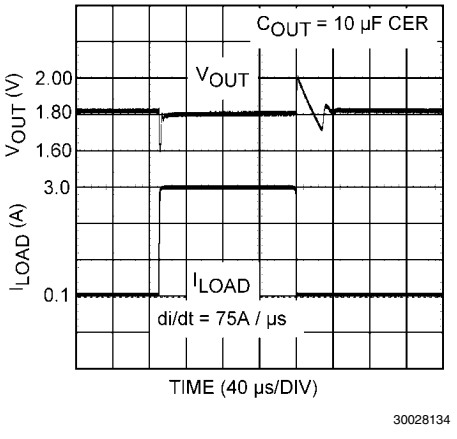


FIGURE 5. Load Transient Response: 10 µF Ceramic, 75A/µs di/dt

A better understanding of the load transient can be obtained when the load's rising edge is expanded in time scale (*Figure 6*).

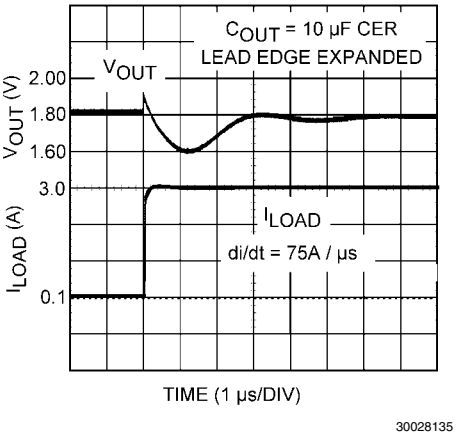


FIGURE 6. Rising Edge, 10 µF Ceramic, 75A/µs di/dt

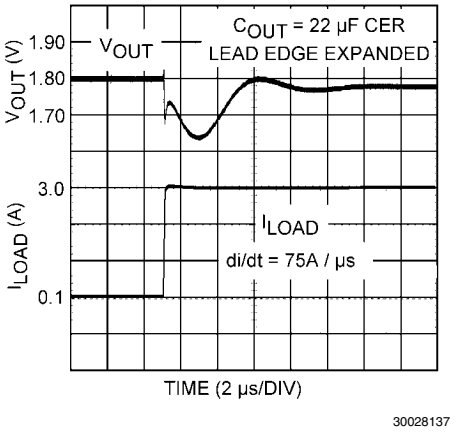


FIGURE 7. 22 µF Ceramic Output Capacitor

It can be seen from the figure that the output voltage starts "correcting" back upwards after less than a micro second, and has fully reversed direction after about 1.2 µs. This very rapid reaction is a result of the maximum loop bandwidth (full load is being delivered) and the feedforward effect kicking on the drive to the FET before feedback gets fully around the loop.

In cases where extremely fast load changes occur, and output voltage regulation better than 10% is required, the output capacitance must be increased. When selecting capacitors, it must be understood that the better performing ones usually cost the most. For fast changing loads, the internal parasitics of ESR (equivalent series resistance) and ESL (equivalent series inductance) degrade the capacitor's ability to source current quickly to the load. The best capacitor types for transient performance are (in order):

1. Multilayer Ceramic: with the lowest values of ESR and ESL, they can have ESR values in the range of a few milli Ohms. Disadvantage: capacitance values above about 22 µF significantly increase in cost.
2. Low-ESR Aluminum Electrolytics: these are aluminum types (like OSCON) with a special electrolyte which provides extremely low ESR values, and are the closest to ceramic performance while still providing large amounts of capacitance. These are cheaper (by capacitance) than ceramic.
3. Solid tantalum: can provide several hundred µF of capacitance, transient performance is slightly worse than OSCON type capacitors, cheaper than ceramic in large values.
4. General purpose aluminum electrolytics: cheap and provide a lot of capacitance, but give the worst performance.

As a first example, larger values of ceramic capacitance will be tried to show how much reduction can be obtained from the 200 mV output change (*Figure 6*) which was seen with only a 10 µF ceramic output capacitor. In *Figure 7*, the 10 µF output capacitor is increased to 22 µF. The 200 mV transient is reduced to about 160 mV, which is from about 11% of V_{OUT} down to about 9%.

In *Figure 8*, the output capacitance is increased to 47 µF ceramic. It can be seen that the output transient is further reduced down to about 120 mV, which is still about 6.6% of the output voltage. This shows that a 5X increase in ceramic capacitance from the original 10 µF only reduced the peak voltage transient amplitude by about 40%.

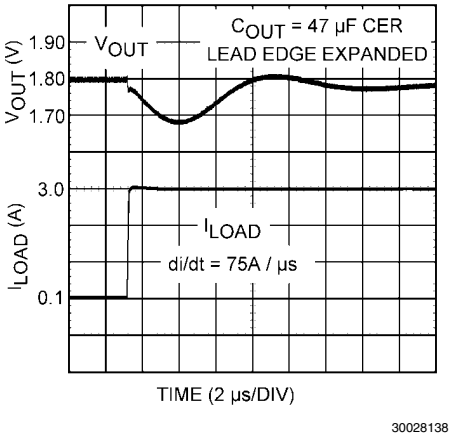


FIGURE 8. 47 µF Ceramic Output Capacitor

In general, managing load transients is done by paralleling ceramic capacitance with a larger bulk capacitance. In this way, the ceramic can source current during the rapidly changing edge and the bulk capacitor can support the load current after the first initial spike in current.

In the next test, the same 10 µF ceramic capacitor will be paralleled with a general purpose (cheap) aluminum electrolytic whose capacitance is 220 µF. As shown in *Figure 9*, there is a small improvement over the 200 mV peak seen with the 10 µF ceramic alone. By adding the 220 µF aluminum capacitor, the peak is reduced to about 160 mV (the same peak value as seen with a 22 µF ceramic capacitor alone).

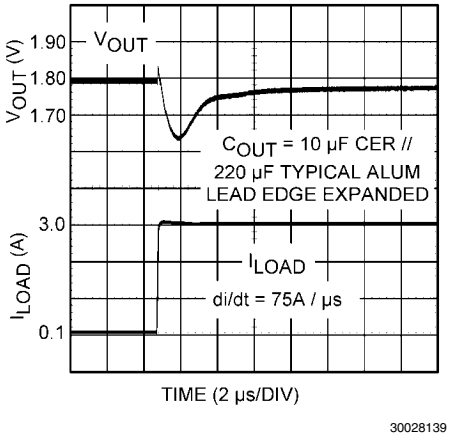


FIGURE 9. 10 µF Ceramic Paralleled By 220 µF Generic Aluminum Electrolytic

A solid Tantalum should work better, so the aluminum electrolytic is replaced by a 220 µF Tantalum (*Figure 10*). The peak amplitude of the output transient is now reduced to about 130 mV, just slightly worse than the value of the 47 µF ceramic alone.

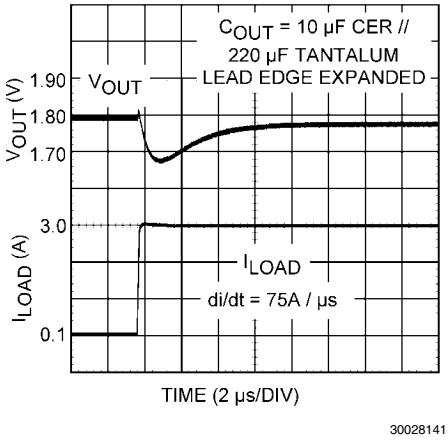


FIGURE 10. 10 µF Ceramic Paralleled By 220 µF Tantalum

The OSCON (ultra low ESR) aluminum electrolytic is the best of the electrolytics. *Figure 11* shows the output voltage transient is reduced down to about 90 mV (about 5% of V_{OUT}) when a 220 µF OSCON is added to the 10 µF ceramic. This indicates that some kind of ultra-low ESR aluminum electrolytic used in parallel with some ceramic capacitance is probably the best approach for extremely fast transients, but each application must be dialed in for it's specific load requirements.

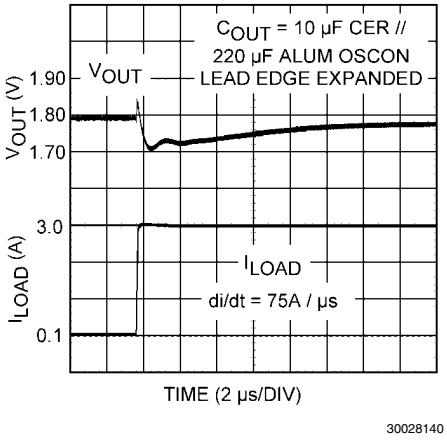


FIGURE 11. 10 µF Ceramic Paralleled By 220 µF OSCON

PRINTED CIRCUIT BOARD LAYOUT

Good layout practices will minimize voltage error and prevent instability which can result from ground loops. The input and output capacitors should be directly connected to the IC pins with short traces that have no other current flowing in them (Kelvin connect).

The best way to do this is to place the capacitors very near the IC and make connections directly to the IC pins via short traces on the top layer of the PCB. The regulator's ground pin should be connected through vias to the internal or backside ground plane so that the regulator has a single point ground.

The external resistors which set the output voltage must also be located very near the IC with all connections directly tied via short traces to the pins of the IC (Kelvin connect). Do not connect the resistive divider to the load point or DC error will be induced.

RFI/EMI SUSCEPTIBILITY

RFI (Radio Frequency Interference) and EMI (Electro-Magnetic Interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC to reduce the amount of EMI conducted into the IC.

If the LP38501/3-ADJ output is connected to a load which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 300 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 300 kHz is determined only by the output capacitor(s). Ceramic capacitors provide the best performance in this type of application.

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. In such cases, it is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load. PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry

should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane. In multi-layer PC Board applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT NOISE

Noise is specified in two ways-

Spot Noise or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Total output noise voltage or **Broadband noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies. Attention should be paid to the units of measurement.

Spot noise is measured in units μV/√Hz or nV/√Hz and total output noise is measured in μV(rms). The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current.

Noise can generally be reduced in two ways: increase the transistor area or increase the reference current. However, enlarging the transisitors will increase die size, and increasing the reference current means higher total supply current (ground pin current).

SHORT-CIRCUIT PROTECTION

The LP38501/3-ADJ contains internal current limiting which will reduce output current to a safe value if the output is overloaded or shorted. Depending upon the value of V_{IN}, thermal limiting may also become active as the average power dissipated causes the die temperature to increase to the limit value (about 170°C). The hysteresis of the thermal shutdown circuitry can result in a “cyclic” behavior on the output as the die temperature heats and cools.

ENABLE OPERATION (LP38501-ADJ Only)

The Enable pin (EN) must be actively terminated by either a 10 kΩ pull-up resistor to V_{IN}, or a driver which actively pulls high and low (such as a CMOS rail to rail comparator). If active drive is used, the pull-up resistor is not required. This pin must be tied to V_{IN} if not used (it must not be left floating).

DROPOUT VOLTAGE

The dropout voltage of a regulator is defined as the input-to-output differential required by the regulator to keep the output voltage within 2% of the nominal value. For CMOS LDOs, the dropout voltage is the product of the load current and the $R_{DS(on)}$ of the internal MOSFET pass element.

Since the output voltage is beginning to “drop out” of regulation when it drops by 2%, electrical performance of the device will be reduced compared to the values listed in the Electrical Characteristics table for some parameters (line and load regulation and PSRR would be affected).

REVERSE CURRENT PATH

The internal MOSFET pass element in the LP38501/3-ADJ has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200 mA continuous and 1A peak. The regulator output pin should not be taken below ground potential. If the LP38501/3-ADJ is used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.

POWER DISSIPATION/HEATSINKING

The maximum power dissipation ($P_{D(MAX)}$) of the LP38501/3-ADJ is limited by the maximum junction temperature of 125°C, along with the maximum ambient temperature ($T_{A(MAX)}$) of the application, and the thermal resistance (θ_{JA}) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND}) \quad (1)$$

where I_{GND} is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (2)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = \Delta T_J / P_{D(MAX)} \quad (3)$$

The LP38501/3-ADJ is available in the TO-263 package. The thermal resistance depends on the amount of copper area allocated to heat transfer.

HEATSINKING TO-263, TO-263 THIN PACKAGES

The TO-263 package and TO-263 THIN package use the copper plane on the PCB as a heatsink. The DAP of the package is soldered to the copper plane for heat sinking. *Figure 12* shows a typical curve for the θ_{JA} of the TO-263 package for different copper area sizes (the thermal performance of both the TO-263 and TO-263 THIN are the same). The tests were done using a PCB with 1 ounce copper on top side only which were square in shape.

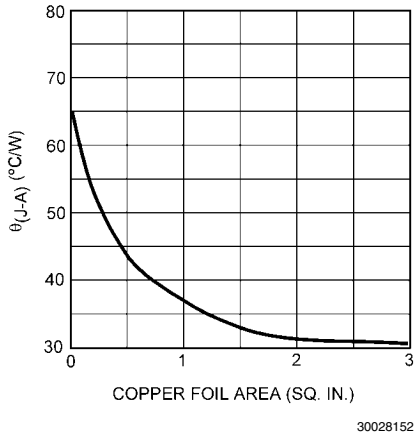
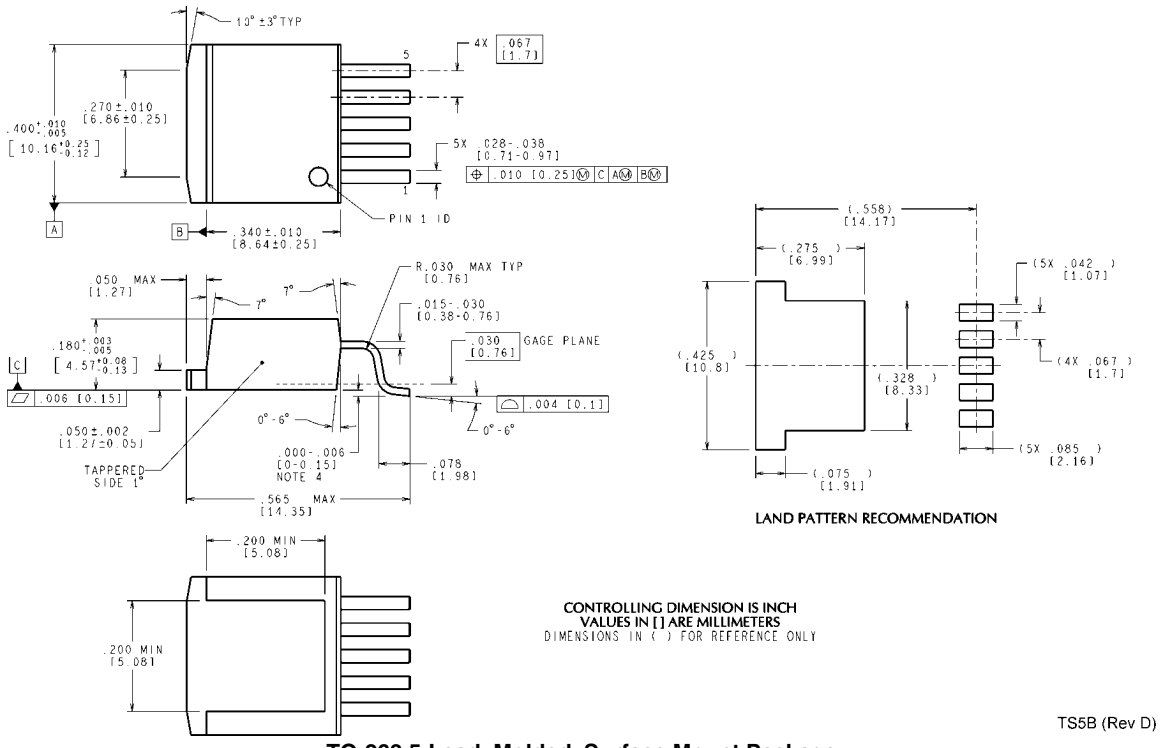


FIGURE 12. θ_{JA} vs Copper Area for TO-263 Package

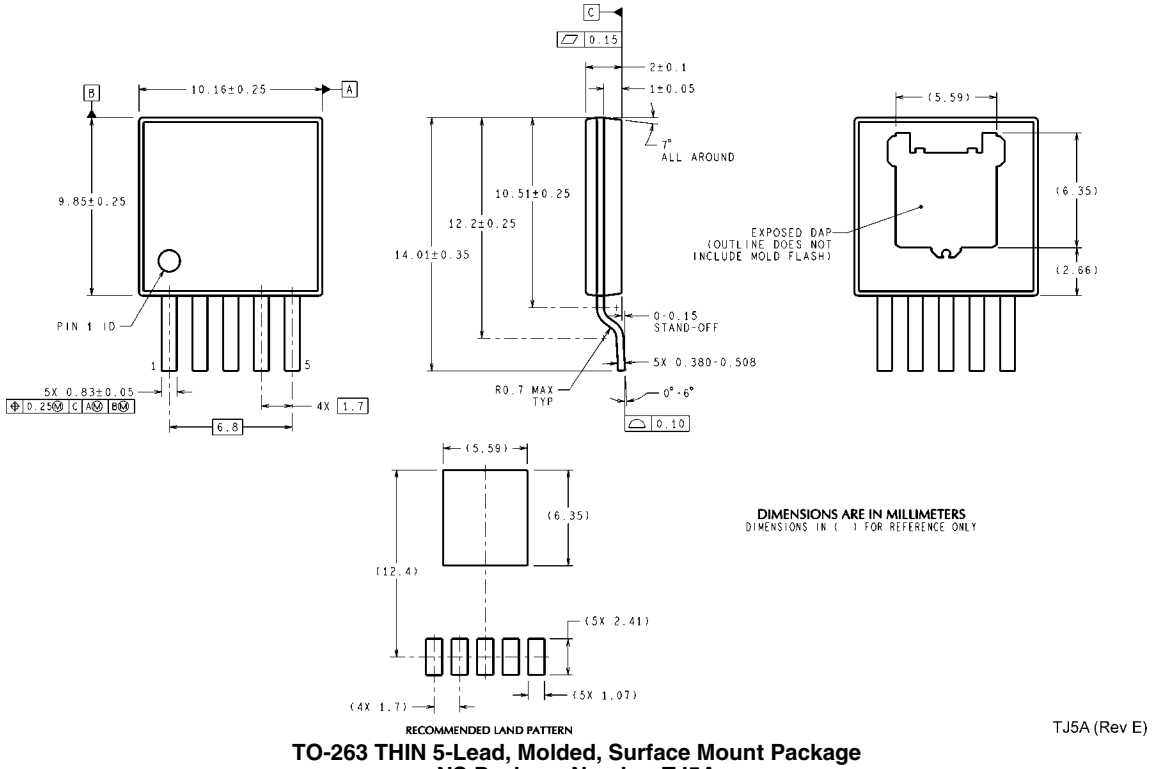
As shown in the figure, increasing the copper area beyond 1.5 square inch produces very little improvement.

Physical Dimensions inches (millimeters) unless otherwise noted



TS5B (Rev D)

TO-263 5-Lead, Molded, Surface Mount Package
NS Package Number TS5B



TJ5A (Rev E)

TO-263 THIN 5-Lead, Molded, Surface Mount Package
NS Package Number TJ5A

Notes

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