L29C520/521
4 x 8-bit Multilevel Pipeline Register

LOGIC DEVICES INCORPORATED

FEATURES

- Four 8-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, and Load Instructions
- Separate Data In and Data Out Pins
- High-Speed, Low Power CMOS Technology
- Three-State Outputs
- DECC SMD No. 5962-91762
- Replaces IDT29FCT520/IDT29FCT521 and AMD Am29520/Am29521
- Package Styles Available:
  - 24-pin Plastic DIP
  - 28-pin Plastic LCC, J-Lead
  - 24-pin Plastic SSOP

DESCRIPTION

The **L29C520** and **L29C521** are pin-for-pin compatible with the IDT29FCT520/IDT29FCT521 and AMD Am29520/Am29521, implemented in low power CMOS.

The L29C520 and L29C521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_{1-0}, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R1 and shifted sequentially through R2, R3, and R4. Also, for the L29C520, data may be loaded from the inputs into either R1 or R3 with only R2 or R4 shifting. The L29C521 differs from the L29C520 in that R2 and R4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_{1-0} may be set to prevent any register from changing.

The S_{1-0} select lines control a 4-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

TABLE 1. L29C520 INSTRUCTION TABLE

I_1	I_0	Description			
L	L	D→R1	R1→R2	R2→R3	R3→R4
L	H	HOLD	HOLD	D→R3	R3→R4
H	L	D→R1	R1→R2	HOLD	HOLD
H	H	ALL REGISTERS ON HOLD			

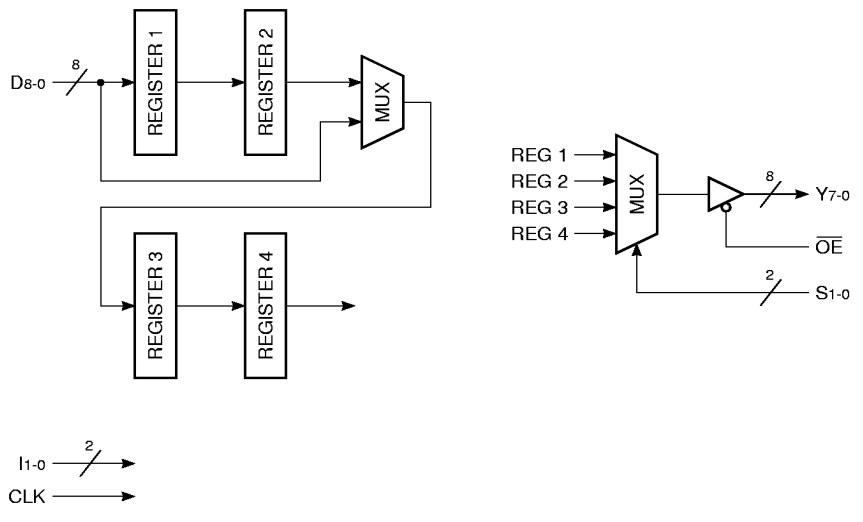
TABLE 2. L29C521 INSTRUCTION TABLE

I_1	I_0	Description			
L	L	D→R1	R1→R2	R2→R3	R3→R4
L	H	HOLD	HOLD	D→R3	HOLD
H	L	D→R1	HOLD	HOLD	HOLD
H	H	ALL REGISTERS ON HOLD			

TABLE 3. OUTPUT SELECT

S_1	S_0	Register Selected
L	L	Register 4
L	H	Register 3
H	L	Register 2
H	H	Register 1

L29C520/521 BLOCK DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –15.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

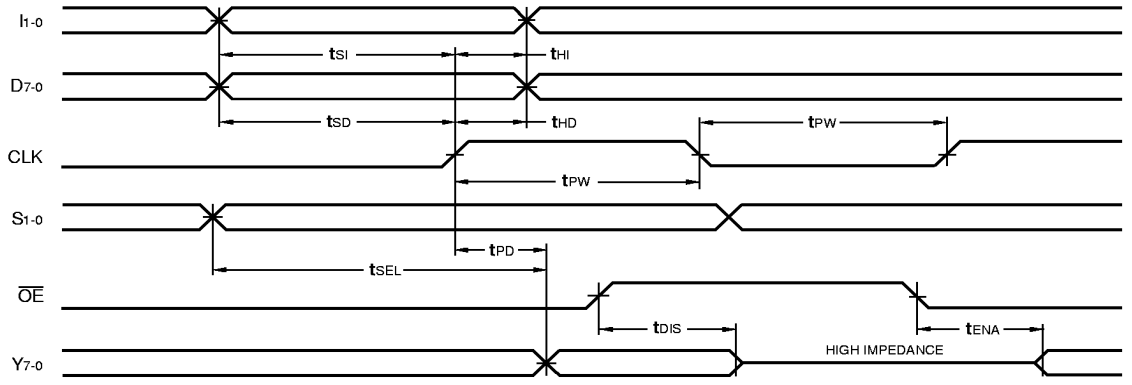
Symbol	Parameter	L29C520/521– 22 Min	22 Max	14 Min	14 Max
t_{PD}	Clock to Output Delay		22		14
t_{SEL}	Select to Output Delay		20		13
t_{PW}	Clock Pulse Width	10		7	
t_{SI}	Instruction Setup Time	10		5	
t_{HI}	Instruction Hold Time	3		1	
t_{SD}	Data Setup Time	10		5	
t_{HD}	Data Hold Time	3		1	
t_{ENA}	Three-State Output Enable Delay (Note 11)		21		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		12

*DISCONTINUED SPEED GRADE

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C520/521– 30* Min	30* Max	24* Min	24* Max	16* Min	16* Max
t_{PD}	Clock to Output Delay		30		24		16
t_{SEL}	Select to Output Delay		30		22		15
t_{PW}	Clock Pulse Width	15		10		8	
t_{SI}	Instruction Setup Time	15		10		6	
t_{HI}	Instruction Hold Time	5		3		2	
t_{SD}	Data Setup Time	15		10		6	
t_{HD}	Data Hold Time	5		3		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		22		16
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		16		13

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

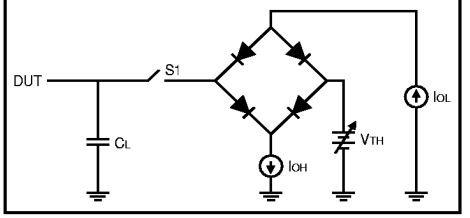
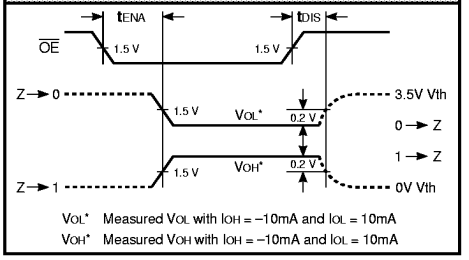
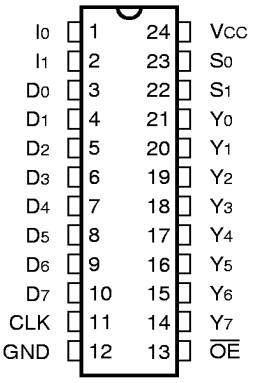


FIGURE B. THRESHOLD LEVELS

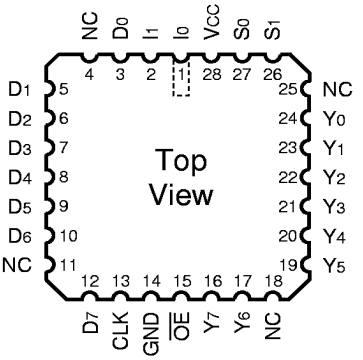


L29C520 — ORDERING INFORMATION

24-pin — 0.3" wide



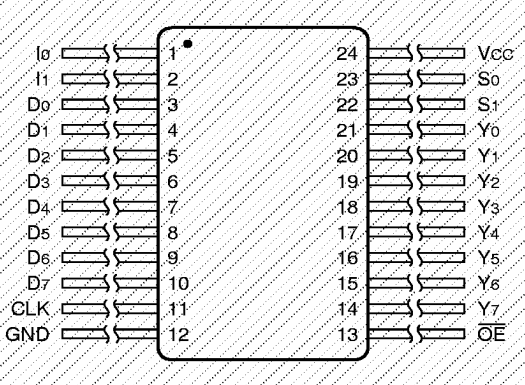
28-pin



Speed	Plastic DIP (P2)		Plastic J-Lead Chip Carrier (J4)	
	0°C to +70°C — Commercial Screening			
22 ns	L29C520PC22		L29C520JC22	
14 ns	L29C520PC14		L29C520JC14	
	–55°C to +125°C — Commercial Screening			
	–55°C to +125°C — MIL-STD-883 Compliant			

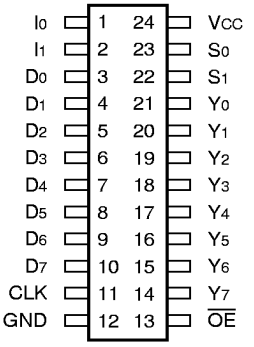
L29C520 — ORDERING INFORMATION

24-pin



Discontinued Package

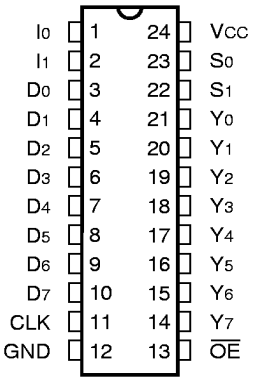
24-pin — 0.209" wide



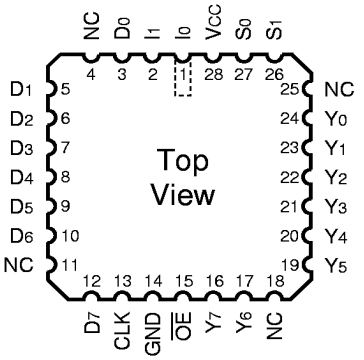
Speed	Ceramic Flatpack (M1)	Plastic SSOP (S1)
	0°C to +70°C — Commercial Screening	
22 ns 14 ns		L29C520SC22 L29C520SC14
	–55°C to +125°C — Commercial Screening	
	–55°C to +125°C — MIL-STD-883 Compliant	

L29C521 — ORDERING INFORMATION

24-pin — 0.3" wide



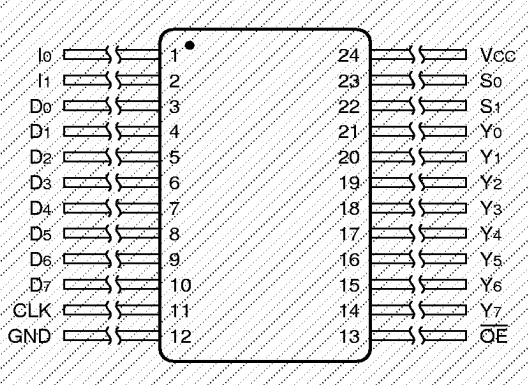
28-pin



Speed	Plastic DIP (P2)		Plastic J-Lead Chip Carrier (J4)	
	0°C to +70°C — Commercial Screening			
22 ns	L29C521PC22		L29C521JC22	
14 ns	L29C521PC14		L29C521JC14	
	–55°C to +125°C — Commercial Screening			
	–55°C to +125°C — MIL-STD-883 Compliant			

L29C521 — ORDERING INFORMATION

24-pin



Discontinued Package

Speed	Ceramic Flatpack (M1)	
	0°C to +70°C — Commercial Screening	
	–55°C to +125°C — Commercial Screening	
	–55°C to +125°C — MIL-STD-883 Compliant	