

SUBSCRIBER LINE INTERFACE CIRCUIT

PRELIMINARY DATA

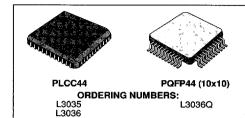
- MONOCHIP SILICON SLIC SUITABLE FOR PUBLIC/PRIVATE APPLICATIONS
- IMPLEMENTS ALL KEY FEATURES OF THE BORSCHT FUNCTION
- METERING PULSE INJECTION AND FILTER-ING WITH MINIMAL COMPONENTS COUNT (NO TRIMMING REQUIRED).
- PROTECTION RESISTOR MISMATCH COM-PENSATION
- ON HOOK TRANSMISSION

BLOCK DIAGRAM

- LOOP START/GROUND START FEATURE
- IND TEMP. RANGE (-40°C to +85°C)
- LOW POWER DISSIPATION IN ALL OPER-ATING MODES
- INTEGRATED ZERO CROSSING RELAY DRIVER
- INTEGRATED (NOISE-LESS) RING TRIP DE-TECTION
- VERY LOW NO. of STD TOLERANCE EX-TERNAL COMPONENTS
- OPTIMIZED FOR U.S. APPLICATIONS (63dB TYP, LONG, BALANCE WITH L3035).
- SURFACE MOUNT PACKAGE (PLCC44 or PQFP44)

ACED RS

CAC RTTX



■ INTEGRATED THERMAL PROTECTION

DESCRIPTION

The L3035/6 subscriber line interface circuit is a bipolar device in 70V technology developed for central office / loop carrier and private applications.

The only difference between L3035 and L3036 is that the L3035 has a better longitudinal balance performance allowing it to meet the United States BELLCORE requirements for central office/loop carrier and private applications

The SLIC integrates loop start, ground start, ground key on/off-hook, automatic ring-trip as well as zero crossing ring relay driver.

GREL REL CRT RGIN UCK STIP LINE ODE T LDGIC ILT STATUS TIP DØ INTERFACE ITNE SUPERUISION ILL D1 INTERFACE RING GST DECODER SPINE LIM COMMANDS AC+DC BGND AC UDFE ILTF BIAS TIXIN DC צמ REFERENCE ZAC AC. £. nr PPACESSAR RTAS PROCESSOR ZΒ SUITCHING TX

USS AGND

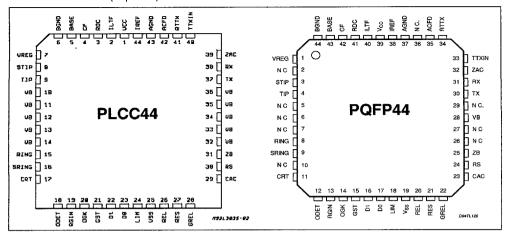
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IREF VCC

PIN CONNECTIONs (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{bat}	Battery Voltage	-64 to V _{SS} +0.5	٧
Vcc	Positive Supply Voltage (0 to 1 ms) (continuous)	-0.4 to +7 -0.4 to +5.5	V V
V _{SS}	Negative Supply Voltage (0 to 1ms) (continuous)	-7 to +0.4 -5.5 to +0.4	V
V _{agnd} - V _{bgnd}	Agnd Respect Bgnd (continuous)	-2 to +2	٧
V _{REL}	Ring Relay Supply Voltage	14	V
V _{dig}	Digital I/O D0, D1, GST, LIM, ODET, OGK	-0.4 to +5.5	V
l _{dig}	Digital I/O Do, D1, GST, LIM, ODET, OGK	-3 to +3	mA
T ₁	Maximum Junction Temperature	+150	°C
T _{stg}	Storage Temperature	-55 to +150	°C
Hu	Humidity	5 to 95	%

Note: In case of power on, power failure or hot insertion with V_{DD}, V_{SS} present and V_{bat} floating the Absolute Maximum Ratings can be exceeded with Vbat > V_{SS} +0.5V. In this case the power consumption of the device increases and the logic output state including relay driver are not controlled. This effect can be prevented ensuring that Vbat is always present before V_{DD} and V_{SS} or connecting one shottky diode (e.g. BAT49X or equivalent) between Vbat and V_{SS} One diode can be shared between all the SLICs of the same line card.

OPERATING RANGE

Top	Operating Temperature Range	-40 to +85	°C
V _{agnd} - V _{bgnd}	Difference between Agnd and Bgnd	-2 to +2	V
Vçç	Positive Supply voltage	+4.5 to +5.5	V
Vss	Negative Supply Voltage	-5.5 to -4.5	V
V _{bat}	Battery Voltage	-62 to -24	V
V _{REL}	Ring Relay Supply Voltage	4 to 13	V

THERMAL DATA

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Symbol	Parameter		PLCC44	Unit
R _{th J-amb}	Thermal Resistance Junction-ambient Max.	75	45	°C/W

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PIN DESCRIPTION

Unless otherwise specified all the diagrams in this datasheet refers to the PLCC44 Pin Connection.

PQFP44 No.	PLCC44 No.	Pin	Description
39	1	Vcc	Positive Power Supply (+5V)
40	2	ILTF	Transversal Line Current Image ((I _A + I _B) / 200)
41	3	RDC	DC feedback input (the RDC resistor is connected from this node to I _{LTF})
42	4	CF	Battery voltage ripple rejection (C _{SVR} capacitor is connected from this node to BGND).
43	5	BASE	Driver for external transistor base
44	6	BGND	Battery ground
1	7	VREG	Regulated Voltage. Provides negative power supply for the power amplifier. (connected to emitter of the external transistor.)
3	8	STIP	Input of A power amplifier (when no compensation of ext. ptc resistor mismatch is requested it must be shorted to the TIP lead).
4	9	TIP	A line termination output (I _A is the current sourced from this pin).
28	10 to 14 32 to 36	VB	Battery Supply (All pins are internally connected together)
8	15	RING	B line termination output (l_B is the current sunk into this pin).
9	16	SRING	Input of B power amplifier (when no compensation of ext. ptc resistor mismatch is requested it must be shorted to the RING lead).
11	17	CRT	Ring trip and ground key capacitor
12	18	ODET	ON/OFF hook and RING TRIP output (when disable is internally pulled up)
13	19	RGIN	Ring input signal. (when open is internally pulled to GND)
14	20	OGK	Ground key output (when disable is internally pulled up)
15	21	GST	A open command (when open is internally pulled down)
16	22	D1	Bit 1
17	23	D0	Bit 0
18	24	LIM	Current Limitation Program. (when open is internally forced to 44mA current limitation)
19	25	Vss	Negative Power Supply (-5V)
20	26	REL	Ring relay driver output
21	27	RES	Reserved should be connected to AGND.
22	28	GREL	Ground reference for ring relay driver
23	29	CAC	AC feedback input (ACDC split capacitor is connected from this node to ILTF)
24	30	Rs	Protection resistors image (the image resistor is connected from this node to ACFD)
25	31	Z _B	Balance network for 2 to 4 wire conversion (the balance impedance Z_B is connecetd from this node to AGND. The Z_A impedance is connected from this node to Z_{AC})
30	37	Tx	4 wire output port (Tx output)
31	38	Rx	4 wire receiving port. (Rx input)
32	39	Z _{AC}	Rx buffer output (the AC impedance is connected from this node to ACFD)
33	40	TTXIN	Metering input port/V _{drop} programming. If not used should be connected to AGND.
34	41	RTTX	Metering cancellation network. If not used should be left open.
35	42	ACFD	AC impedance synthesis
37	43	AGND	DC and AC signal ground
38	44	IREF	Voltage Reference Output
2,5 to 7, 10,26, 27, 29,36	-	N.C.	Not connected

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DESCRIPTION (continued)

L3036 is available in two different package options: PLCC44 and PQFP44(10 x 10).

Two to four wire conversion is implemented by the SLIC for applications with first generation COMBO. In case of application with second generation (programmable) COMBO this function can be implemented outside saving external components.

The L3035/6 offers programmable current limitation (3 ranges), on hook transmission and low power in all operating modes, power management is controlled by a simple external low cost transistor.

Metering pulses are injected on the line via a summing node through TTXIN pin.

Metering pulse filtering is performed by means of a simple RC network with standard tolerance components. When TTX function is not used this pin must be connected to AGND. It is also possible to use this pin to modify the DC voltage drop between TIP/RING terminals and battery voltage for appications where it is important to optimize the battery voltage supply versus the signal swing.

Effects of protection resistor mismatch are compensated by a feedback loop on the final stage, allowing good longitudinal balance performance even with large tolerance protection resistors (ex: PTC).

This function allows L3035 to fully conform to BELLCORE power cross and surge tests and also meet the Longitudinal Balance Specification without using matched PTC resistors.

An integrated thermal protection circuit forces the L3035/6 into POWER DOWN (PD) mode when the junction temperature exceeds 150°C Typ.

L3035/6 is specified over a -40°C to +85°C ambient temperature range.

L3035/6 package is a surface mount 44PLCC.

FUNCTIONAL DESCRIPTION

L3035/36 is designed in 70V bipolar technology and performs the telephone line interface functions required in both C.O. and PABX environments. The full range of signal transmission, battery feed, loop supervision are performed.

Signal transmission performance is compatible with European and North American Standards and with CCITT recommendations.

Ringing, overvoltage and power cross protection are performed by means of external networks.

The signal transmission function includes both 2 to 4 wire and 4 to 2 wire conversion. The 2W termination impedance is set by means of an external impedance which may be complex. The 2 to 4 wire conversion is provided by means of an external network.

Such a network can be avoided in case of applications with COMBOII, in this case the 2 to 4 wire conversion is implemented inside the COMBOII by means of the programmable Hybal filter.

An additional input allows a metering pulse signal to be added on the line.

The DC feed resistance is programmable with one external resistor. Three different values of current limitation (25, 43, 56mA)can be selected by software through the parallel digital interface.

One external transistor reduces the power dissipation inside the L3035/6 in the presence of a short loop (limiting current region).

An additional supervisory function sets the TIP lead into high impedance state in order to allow application in ground start configurations.

The different L3035/6 operating modes are controlled by a 4bit logic interface, two additional detector outputs provide ground key detection and either hook state or ring trip detection.

SLIC OPERATING MODES

Through the L3035/6 digital interface it is possible to select 5 different SLIC operating modes:

- 1) Active Mode (ACT)
- Standby Mode (SBY)
- Tip Open Mode (TO)
- 4) Power Down Mode (PD)
- 5) Ringing Mode (RNG)

ACTIVE MODE (ACT)

This operating mode is set by the card controller when the Off-Hook condition has been recognized.

When this operating mode is selected the two output buffers (TIP/RING) can sink or source up to 100mA each. In case of Ground key or line terminals to GND the output current is limited to 15mA for the Tip wire and 30mA for the Ring wire.

As far as the DC characteristic is concerned three different feeding conditions are present:

a) Current limiting region: the DC impedance of the SLIC is very high (20Kohm) and therefore the system works like a current source. Using the L3035/6 digital interface it is possible to select the value of the limiting current:

25mA, 43mA, or 56mA.

When the device is in limiting current region the negative supply for the output buffer is fixed by the ext. transistor to a proper value higher than the real negative battery in order to reduce the power dissipated by the L3035/6 itself.

- b) Resistive feed region: the characteristic is equal to a battery voltage (Vbat) in series with a resistor (typ 400ohm or 800ohm) whose value is set by one ext. resistor (see ext. components list).
- c) Constant voltage region: the characteristic is equal to the battery voltage 12V in series with the ext. protection resistors (typ 80ohm).

This voltage drop between battery and line termi-

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nals for II=0 allows on-hook transmission.

Fig. 1 shows the DC characteristic in active mode. Fig. 2 shows the line current versus loop resistance

Figure 1: DC Characteristic in active mode

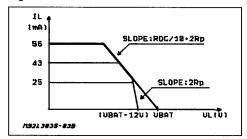
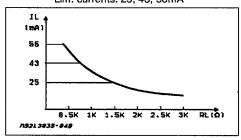


Figure 2: Current vs. Loop Resistance. Rfeed = 2 x 2000hm, Lim. currents: 25, 43, 56mA



In active mode the AC impedance at the line terminals is sinthetized by the external components ZAC and Rp according to the following formula:

$$Zs = ZAC/50 + 2*Rp$$

Depending on the characteristic of the ZAC network, Zs can be either a pure resistance or a complex impedance. This allows L3035/6 to meet different standards as far as return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two to four wire conversion is achieved by means of a circuit that can be represented as a Wheastone bridge, the branches of which are:

The line impedance (Zline)

CONTROL INTERFACE

	INP	UTS		OPERATING MODE OUTPUTS	PUTS	
D0	D1	GST	LIM			OGK
0	0	0	х	POWER DOWN	DISABLE	DISABLE
1	1	0	X	STANDBY	OFF/HK	GDKEY
1	0	0	0	ACTIVE (25mA)	OFF/HK	i GDKEY
1	0	0	HI	ACTIVE (43mA)	OFF/HK	GDKEY
1 1	0	0	1	ACTIVE (56mA)	OFF/HK	GDKEY
0	1	0	X	RING	RING-TRIP	DISABLE
0	0	1	X	A OPEN	OFF/HK	GDKEY

- 2) The SLIC impedance at line terminals (Zs)
- 3) The balancing network ZA+RA connected between pin ZAC and ZB of L3035/6.
- 4) The network ZB between pin ZB and GND that shall copy the line impedance.

When L3035/6 is used with a second generation combo (eg TS5070FN) which is able to perform the two to four wire conversion, the two impedances ZA and ZB can be removed and the ZB pin concected to GND. The -6dB TX gain of the L3035/6 allows the echo signal to remain always within the COMBOII Hybrid balance filter dynamic range.

The injection of high frequency metering pulses is carried out through the SLIC. An unbalanced 12 or 16KHz sinusoidal signal with shaping is, when necessary, applied at the TTXIN input of the SLIC.

A fixed transfer gain is provided for the metering signal. To avoid saturation in the 4-wire side a cancellation is provided in the 4-wire transmission path.

Cancellation is obtained via an external RC network without the need for trimmed components.

When the TTX function is not used TTXIN input should be connected to GND. Since this pin is directly connected to a summing node inside the SLIC any signal applied to the TTXIN is transferred to the line with a fixed transfer gain.

In special applications, this pin can be used to modify the voltage drop (constant voltage region of DC characteristic) simply by applying a proper DC level on the TTXIN pin, allowing optimization of the battery voltage versus the maximum needed AC signal swing.

In active mode, with a -48V battery voltage, the L3035/6 dissipates 150mW for its own operation (including the power dissipation from +5/-5 supply), the dissipation related to the current supplied to the line should be added in order to get the total dissipation.

STAND-BY MODE (SBY)

In this mode the bias current of the L3035/6 is reduced and only some part of the circuit are completely active. The transversal current supplied to the line is limited at 12mA. Common mode current rejection is performed and the total current capability of the output stages (TIP and RING) is limited to 30mA. The open circuit voltage is |Vbat|-7V.

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Both Off/Hook and Ground key detectors are active. Signal transmission is not operating.

In stand-by mode, with a -48V battery voltage, the L3035/6 dissipates 90mW typ. (including the power dissipation from a +5/-5V supply).

Stand-by mode is usually selected when the telephone is in on-hook condition. It allows a proper off-hook detection, even in the presence of high common mode currents, or with telephone sets sinking a few milliamperes of line current in on-hook condition.

TIP OPEN MODE (TO)

This mode is selected when the SLIC is adopted in a system using the Ground start feature. In this mode the TIP termination is set in High Impedance (100Kohm) while the RING termination is active and fixed at Vbat + 4.5V. In the case of connection of RING termination to GND the sinked current is limited to 30mA. When RING is connected to GND both off-hook and ground-key detectors become active.

Power dissipation in this mode with a -48V battery voltage is 100mW (including the power dissipation from +5/-5V supply).

POWER DOWN MODE (PD)

In this mode, both TIP and RING terminations are open and no current is fed into the line.

The power dissipation is very low.

This mode is usually selected in emergency conditions or when the connected line is disabled.

This is also the mode into which the SLIC is automatically forced, in the case of thermal overload $T_i > 150^{\circ}\text{C}$ typ.

RINGING MODE (RNG)

When this mode is selected the ringing signal is injected on the line via the ext relay activated by the L3035/6 relay driver.

When the ringing signal phase is provided at the RGIN pin, the relay command is also synchronized with the ringing signal zero crossing.

The TIP and RING termination of the L3035/6

also senses the line current which is then integrated on the CRT capacitor.

TIP pin voltage is fixed at – 2.5V, RING pin voltage is fixed at V_{BAT} + 4.5V, TIP, RING buffer current capability is limited to 100mA.

When off-hook occurs during ringing burst the voltage on CRT increase above a proper threshold and ring trip is detected.

Once ring trip is detected the ringing signal is automatically disconnected at the first zero crossing. When the ringing signal phase is not provided at the RGIN pin the ringing signal is disconnected immediately after ring trip detection.

EXTERNAL COMPONENTS LIST

To set the SLIC into operation the following parameters have to be defined:

- The DC feeding resistance "Rfeed" defined as the resistance of the traditional feeding system (most common Rfeed values are: 400, 800, 1000 ohm).
- The AC SLIC impedance at line terminals "Zs" to which the return loss measurements is referred. It can be real (typ. 600ohm) or complex.
- The equivalent AC impedance of the line "ZI" used for evaluation of the trans-hybrid loss performance (2/4wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.
- The line impedance at the TTX freq. Zlttx.

Once, the above parameters are defined, it is possible to calculate all the external components using the following table.

The typical values has been obtained supposing:

- Rfeed = 400Ω
- $-Zs = 600\Omega$
- $-ZI = 600\Omega$
- $Rp = 40\Omega$
- $ZIttx = 216\Omega + 120nF @ 12KHz$
- $Re[Zlttx] = 216\Omega$
- $\text{Im}[Z|\text{Ittx}] = -110\Omega @ 12KHz$

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EXTERNAL COMPONENTS

Name	Function	Formula	Typ. Value
CVB	Battery Filter		330nF 20% 63VI
CVDD	Positive Supply Filter		100nF 20%
CVSS	Negative Supply Filter		100nF 20%
RREF	Internal Current Reference		23.7K 1%
CSVR	Battery Ripple Rejection	CSVR = 1/(6.28 * fp * 150K) @ fp = 1.6Hz	680nF 20% 60VI
CRT	Ring Trip & Ground-key Capacitor	CRT = (25/f _{RING}) · 390nF	390nF 20% 6VI
RDC	DC Feeding Resistance	RDC = 10 * (Rfeed - 2Rp)	3.2K 1%
CAC	AC/DC Splitter	CAC = 1 / (6.28 * fsp * RDC) @ fsp = 10Hz	4.7μF 20% 15VI
RS	Protection Resistor Image	RS = 50 * 2RP	4K 1%
ZAC	2 Wire AC Impedance	ZAC = 50 * (Zs-2Rp)	26K 1%
ZA (1)	SLIC Impedance Balancing Network	ZA = 50 * (Zs-2Rp)	26K 1%
RA (1)	SLIC Impedance Balancing Network	RA = 50 * 2Rp	4K 1%
ZB (1)	Line Impedance Balancing Network	ZB = 50 * ZI	30K 1%
CCOMP	AC Feedback Compensation	ССОМР = 1 / [2Пfo (100 Rp)] @ fo = 250KHz	220pF 20%
CH (1)	Trans-hybrid Loss Frequency Compensation	CH = CCOMP	220pF 20%
RF	Feeding Resistance for Ring Inj.	≥ 200Ω (7)	200Ω 2W
RT	Feeding Resistance for Ring Inj.	≥ 200Ω (7)	200Ω 2W
RRG	Ring Input Resistor	RRG = (V _{RING} /25μA)cos[-2·f _{RING} · T · 180] (4)	4ΜΩ 5%
CRG	Ring Input Capacitor	CRG = 25μ A/(V _{RING} · sin[2 · f _{RING} ·T · 180] · 2∏f _{RING}) (4)	3.9nF 20% 100V
PTC (2)	Positive Temp. Coeff. Resistor	< 15Ω	10Ω
RST (2)	Tip Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (6)
RSR (2)	Ring Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (6)
QEXT	External Transistor (3)		(*)
Rp	Protection Resistor	30 to 80Ω (8)	40Ω
RTTX	Teletax Cancellation Resistor	RTTX = 21.5 · [Re (Zlttx) +2Rp] (5)	6.34K 1%
СТТХ	Teletax Cancellation Capacitor	CTTX = $1/(21.5 \cdot [-lm(Zlttx) \ fttx \cdot 6.28])$ (5)	5.6nF 20%
D1	Relay Kickback Clamp Diode		1N4148

Notes:

- (1) These components can be removed and ZB pin shorted to GND when 2/4wire conversion is implemented with 2nd generation COMBO (EG. TS5070FN)
- (2) In case there is no necessity to recover the unbalance introduced by PTC tolerance pins TIP and STIP can be shorted togheter as pins RING and SRING. In this case also the R_F Resistor should be splitted in two parts keeping at least 20Ω between TIP/RING terminals and protection connection. In this case PTC or fuse resistor (if used) can be placed in series to R_D.
- (3) Transistor characteristic: Pbss = 1W (typ. depending on application) h_{FE} ≥ 25; l_C ≥ 100mA; V_{CEO} ≥ 60V; f_T ≥ 15MHz.
- (4) VRING: Max Ring Generator Voltage, fring: Ring Frequency, T: relay response time Typical value obtained for VRING = 100Vrms, fring = 25Hz; T = 2.5ms.
- (5) Defining RTTX + CTTX = ZTTX, RTTX and CTTX can also be calculated from the following formula: Z_{FTTX} = 21.5 [Zittx + 2Rp].
- (6) RST and RSR wattage should be calculated according to the power cross test specification. (When PTC become open circuit the entire power cross voltage will appear across RSR and RST).
- (7) In order to optimize the component count it is also possible to use only one resistor in series to the ringing generator. In this case RT = 0Ω; RF≥ 400Ω (RF typ. value = 400Ω).
- (8) Suggested Rp type are 2W wire wound resistors or thick film resistors on ceramic substrate. Fuse function should be included if PTC are not used.
- (*) ex⁻ BD140; MJE172;MJE350. (SOT32 or SOT32 package available also for surface mount). For low power application (reduced battery voltage) BCP53 (SOT223 surface mount package) can be used.

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Figure 3: Typical Application Circuit including all features.

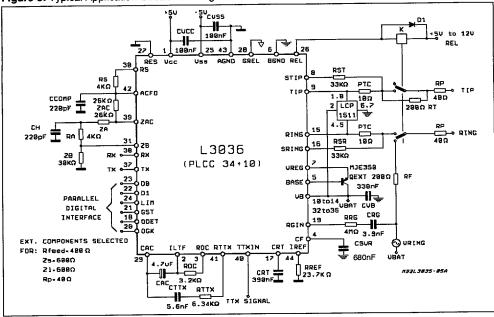
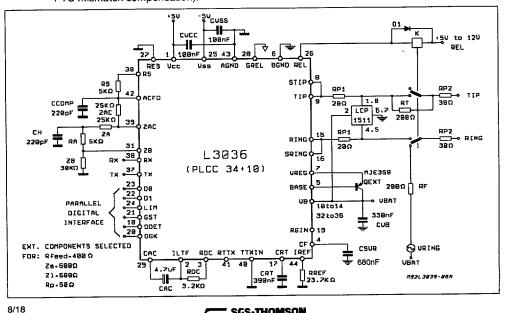


Figure 4: Typical Application circuit with minimum components count (NoTTX/No zero crossing sync/no PTC mismatch compensation).



In case of U.S. application based on L3035 the external components can be calculated supposing:

- Rfeed = 400Ω

 $-Zs = 900\Omega + 2.12\mu F$

 $-ZI = 1650\Omega// (100\Omega + 5nF)$ Loaded Line

- ZI = 800Ω // (100Ω + 50nF) Not Loaded Line

 $-Rp = 62\Omega$

EXTERNAL COMPONENTS (for US. Application)

Name	Function	Formula	Typ. Value
CVB	Battery Filter		330nF 20% 63VI
CVDD	Positive Supply Filter		100nF 20%
CVSS	Negative Supply Filter		100nF 20%
RREF	Internal Current Reference		23.7K 1%
CSVR	Battery Ripple Rejection	CSVR = 1/(6.28 * fp * 150K) @ fp = 1.6Hz	680nF 20% 60VI
CRT	Ring Trip & Ground-key Capacitor	CRT = (25/f _{RING}) · 390nF	390nF 20% 6VI
RDC	DC Feeding Resistance	RDC = 10 * (Rfeed - 2Rp)	2.76K 1%
CAC	AC/DC Splitter	CAC = 1 / (6.28 * fsp * RDC) @ fsp = 10Hz	4.7μF 20% 15VI
RS	Protection Resistor Image	RS = 50 * 2RP	6.2K 1%
ZAC	2 Wire AC Impedance	ZAC = 50 * (Zs-2Rp) (7)	39K + (180K//55nF)
ZA (1)	SLIC Impedance Balancing Network	ZA = 50 * (Zs-2Rp) (7)	39K + (180K//55nF)
RA (1)	SLIC Impedance Balancing Network	RA = 50 * 2Rp	6.2K 1%
ZB (1)	Line Impedance Balancing Network	ZB = 50 * ZI	82.5K + (5K + 100pF) (3) 40K + (5K + 1nF) (4)
CCOMP	AC Feedback Compensation	ССОМР = 1 / [2Пfo (100 Rp)] @ fo = 250KHz	100pF 20%
CH (1)	Trans-hybrid Loss Frequency Compensation	CH = CCOMP	100pF 20%
RF	Feeding Resistance for Ring Inj.	≤ 200Ω (9)	200Ω 2W
RT	Feeding Resistance for Ring Inj.	≤ 200Ω (9)	200Ω 2W
RRG	Ring Input Resistor	RRG = (V _{RING} /25μA)cos[-2·f _{RING} · T · 180] (6)	4MΩ 5%
CRG	Ring Input Capacitor	CRG = 25μΑ/(V _{RING} · sin[2 · f _{RING} ·T · 180] · 2Πf _{RING} (6)	3.9nF 20% 100V
PTC (2)	Positive Temp. Coeff. Resistor	< 15Ω	10Ω
RST (2)	Tip Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (8)
RSR (2)	Ring Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (8)
QEXT	External Transistor (5)		(*)
Rp	Protection Resistor	30 to 80Ω (10)	62Ω
D1	Relay Kickback Clamp Diode		1N4148

Notes:

- (1) These components can be removed and ZB pin shorted to GND when 2/4wire conversion is implemented with 2nd generation COMBO (EG. TS5070FN)
- (2) In case there is no necessity to recover the unbalance introduced by PTC tolerance pins TIP and STIP can be shorted togheter as pins RING and SRING. In this case also the R_P Resistor should be splitted in two parts keeping at least 20Ω between TIP/RING terminals and protection connection. In this case PTC or fuse resistor (if used) can be placed in series to Rp.
- (3) Loaded Line.
- (4) Not Loaded Line.
- (5) Transistor characteristic: P_{DISS} = 1W (typ. depending on application); h_{FE} ≥ 25; l_C ≥ 100mA; V_{CEO} ≥ 60V; f_T ≥ 15MHz.
- (6) VRING: Max Ring Generator Voltage, fRING: Ring Frequency, T: relay response time. Typical value obtained for VRING = 100Vrms, fRING = 25Hz; T = 2.5ms.
- (7) For details see AN496.
- (8) RST and RSR wattage should be calculated according to the power cross test specification. (When PTC become open circuit the entire power cross voltage will appear across RSR and RST).
- (9) In order to optimize the component count it is also possible to use only one resistor in series to the ringing generator. In this case RT = 0Ω; RF≥ 400Ω (RF typ. value = 400Ω).
- (10) Suggested Rp type are 2W wire wound resistors or thick film resistors on ceramic substrate. Fuse function should be included if PTC are not used.
- (*) ex: BD140; MJE172;MJE350....(SOT32 or SOT82 package available also for surface mount).

 For low power application (reduced battery voltage) BCP53 (SOT223 surface mount package) can be used.

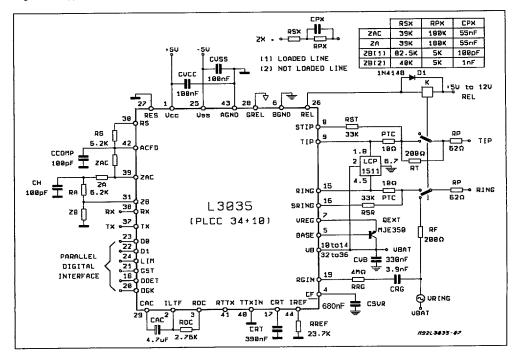
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Figure 5: Typical Application Circuit for U.S. Application.



ELECTRICAL CHARACTERISTICS TEST CONDITION, unless otherwise specified: $V_{CC} = 5V$; $V_{SS} = -5V$; $V_{BAT} = -48V$; AGND = BGND; $T_A = 25^{\circ}C$.

Note: Testing of all parameter is performed at 25°C. Characterization as well as the design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the range 0°C to +70°C. Additional selection (on request ordering part #: L3035/6T) can be performed so that the functionality between -40°C and 85°C is verified.

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
NTERFAC	E REQUIREMENTS 2 WIRE P	ORT				
V _{ab}	Overload Level Voice Signal	Rp +PTC = 50Ω 300Hz to 3.4KHz (*)	4.1			Vpk
Zμ	Long Input Impedance	at SLIC terminals per wire			10	Ω
l _{II}	Long Current Capab. ac	standby per wire (on HOOK)	17			mApk
	1	active per wire (on HOOK)	17			mApk
lη	Longitudinal Current Capability	active per wire off HOOK (IT = Transversal current)	75-I _⊤			mApk
WIRE TRA	ANS PORT					
V _{tx}	Overload Level		1.8			Vpk
V _{toff}	Output Offset Voltage		-350		350	mV
Z _{tx}	Output Impedance				10	Ω

^(*) At TIP/RING line connection with Z_{LINE} (AC) = 600Ω. For any DC Loop current from 0mA to I_{LIM}

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L3035 Longitudinal balance (IEEE Std 455-1976)

Longitudinal to Transversal

Longitudinal Signal Rejection

 $\mathbf{L} - \mathbf{T}$

L-4

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
4 WIRE REC	CEIVE PORT				4	L
Z _{RX}	Input Impedance		100			ΚΩ
V _{RX}	Overload Level		3.2			Vpk
METERING	INPUT PORT				•	
Z _{MIN}	Input Impedance		100			ΚΩ
LOGIC CON INPUT D0, [ITROL PORT 01, GST					
V_{th}	Input High Voltage		2			٧
V _t	Input Low Voltage				0.8	٧
l _{ih}	Input High Current		-10		90	μA
l _{tt}	Input Low Current		-10		10	μА
C _{in}	Input Capacitance				10	pF
INPUT LIM						
V _{th}	Input High Voltage		2.4			٧
Vil	Input Low Voltage				0.4	V
l _{ih}	Input high Current		-10		30	μА
l _{il}	Input Low Current		-30		10	μA
C _{in}	Input Capacitance				10	pF
OUTPUT DE	T					
Vol	Output Low Voltage	l _o = 1.5mA			0.4	٧
V _{oh}	Output High Voltage	I _o = 30μA I _o ≤10μA	2.4 3.8			>>
Cld	Load Capacitance				150	ρF
RINGING IN	PUT PORT					
****	Overload Level		-0.5		0.5	٧
	Input Impedance		50		90	ΚΩ
	Offset Voltage Allowed		-15		15	mV
RANSMIS	SION PERFORMANCE					
Arl	Return Loss (2-wire)	300Hz to 3.4KHz	22			dB
Thl	Transhibrid Loss	300Hz to 3.4KHz	30			dB
		$20log_{10} \mid \frac{V_{RX}}{V_{TX}} \mid$				
Longitudinal	balance (CCITT Rec.0.121)				J	
L-T	Longit to Transversal	300Hz to 3.4KHz	52			dB
L-4	Long Sign Rejection	$Zs = 600\Omega$	58			dB
T-L	Transvers to Longit	= Rp = 40Ω, 1% tolerance	49			dB
4-L	Long Sign Generation		49			dB

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300Hz to 3.4KHz

 $Z_S = 900\Omega + 2.12\mu F$

 $R_P = 62\Omega$, 1% match

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63

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dΒ

dΒ

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
INSERTION	LOSS					
Gt	Transmit V Gain	0dBm, 1KHz	-6.25		-5.79	dB
Gr	Receive V Gain		-0.2		0.2	ďВ
INSERTION	LOSS vs. FREQUENCY (rel 1KHz /	0dBm)				
Gt	Transmit V Gain	0.3 to 3.4KHz	-0.1		0.1	₫B
Gr	Receive V Gain		-0.1		0.1	dB
METERING	NJECTION					
GTTX	Transfer Gain	$V_{TTXIN} = 0.66V \text{rms } Z_L = 200\Omega;$	3.18		3.51	
THD	Harmonic Distortion	$2 \cdot R_P = 80\Omega$; $V_{moff} = 0$			3	%
GAIN LINEA	RITY (rel 1KHz, -4dBm)					
Gt	Transmit V Gain	-55dBm to 7dBm (1)	-0.1		0.1	d₽
Gr	Receive V Gain		-0.1		0.1	dB
GROUP DEL	AY (2-4, 4-2) 0DbM					
TgABS	Absolute	3KHz		5		μs
T _{gDIS}	4 to 2-wire	0.5 to 3,4KHz	<u> </u>	5	<u> </u>	μs
TOT HARMO	ONIC DISTORTION					
Thd4	2 to 4-wire	7dBm, 0.3 to 3.4KHz			-46	dB
Thd2	4 to 2-wire				-46	dB
IDLE CHAN	NEL NOISE					
Vabp	2-wire port	psophometric		-78	-72	dBmP
Vtxp	4-wire transmit	psophometric		-82	-76	dBmP
Vabc	2-wire port	c message		12	18	dBrnC
Vtxc	4-wire transmit	c message		8	14	dBrnC

RINGING FUNCTION

0 cross	Zero Crossing Threshold Level	f _{RING} = 16 to 66Hz R _{GIN} = 3Vrms	-70		70	mV
I _{BT}	Ring Trip Threshold			7.5		mA DC
T _{RTD}	Ring Trip Detection Time	R _L = 1.8k, f _{RING} = 25Hz			150	ms

BATTERY FEED CHARACTERISTIC

POWER DO	OWN STATE					
ILGND	Loop Current	TIP or RING to BGND			0.5	mA
LBAT	Loop Current	TIP or RING to V _{bat}			0.5	mA
lι	Loop Current	R _L = 0			1	mA
STAND BY	STATE					
lı	Iloop Accuracy	constant region	11		15	mA
V _{LOS}	Line Voltage	@ I _L = 0	40		42	V
ACTIVE ST	ATE					
V _{LO}	Line Voltage	@ I _L = 0	34.5		37.5	V
R _{feed}	Feeding Resistance Accuracy		-10		10	%
l _{lim}	Loop Current Limit Accuracy	I _{lim} = 25mA, 43mA, 56mA	-8	l _{lim}	8	%
GROUND S	START STATE					
Z _{TIP}	Tip Lead Impedance		100			ΚΩ
Igs	Ring Lead Current	RING to GND		30		mA

^{(1):} For level lower than -40dBm guaranteed by correlation.

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Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
DETECTOR	RS					
OFF HOOK	DETECTOR					
l _{det}	Off-hook Current Threshold	stand by state	9		12	mA
l _{det}	Off-hook Current Threshold	active state	9		12	mA
Hys	Off-hook / On-hook Hysteresys	Both stand by and active state	1		1.6	mA
Td	Dialling Distortion	active state	-1		1	ms
GROUND K	EY DETECTOR					
luu	Ground Key Current Threshold I _{LL} = (I _B - I _A) / 2	TIP to RING to GND or RING to GND		4		mA
POWER DI	SSIPATION ON L3035/36 at V	BAT = 48V				
Pd	Power Down	any line lenght			38	mW
Pd	Stand-by	2-wire open		95	136	mW

Pd	Power Down	any line lenght		38	mW
Pd	Stand-by	2-wire open R _L = 0 to 2K	95	136 220	mW mW
Pd	Active, $R_{feed} = 800\Omega$ $I_{LIM} = 25 \text{mA}$ $I_{LIM} = 43 \text{mA}$ $I_{LIM} = 56 \text{mA}$	2-wire open R _L = 0 to 2K	155	224 710 1690 2710	mW mW mW mW
P _d	Active, Rfeed = 400Ω I _{LM} = 25mA I _{LM} = 43mA I _{LM} = 56mA	2-wire open R _L = 0 to 2K R _L = 0 to 2K R _L = 0 to 2K	155	224 510 850 1300	mW mW mW
Pd	Active	Ground Key	1500		mW

POWER DISSIPATION ON QEXT AT Vbat = 48V

Pdq	Active, R _{feed} = 800Ω I _{LM} = 25mA I _{LM} = 43mA I _{LM} = 56mA	R _L = 0 to 2K R _L = 0 to 2K R _L = 0 to 2K	880 790 430	mW mW mW
P _{dq}	Active, Rfeed = 400Ω I _{LIM} = 25mA I _{LIM} = 43mA I _{LIM} = 56mA	$R_L = 0$ to 2K $R_L = 0$ to 2K $R_L = 0$ to 2K	1080 1580 1700	mW mW mW

SUPPLY CURRENTS

ANALOG S	SI IDDI V				
lcc	Vcc	Power Down	1.5	2.2	mA
Iss	Vss	Power Down	0.1	0.5	mA
lcc	Vcc	Stand-by/ A open	4	5	mA
Iss	Vss	Stand-by/ A open	1.5	3	mA
lcc	Vcc	Active	6	10	mA
Iss	V _{SS}	Active	3	6	mA
BATTERY	SUPPLY				
l _{bat}	Power down	a or b to BGND	120	500	μА
l _{bat}	Stand-by/ A open	2-wire open	1.4	2	mA
l _{bat}	Active	2-wire open 2-wire $R_L = 400\Omega$	2.3	3 I _{I+} 5	mA mA

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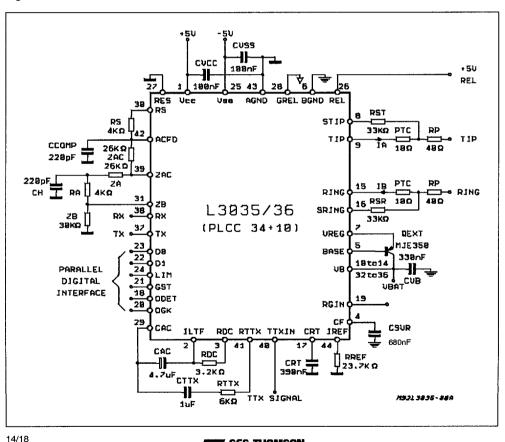
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Symbol	Parameter	lest Condition	Min.	Typ.	мах.	Unit	
POWER SUPPLY REJECTION (VRIPPLE = 100mVrms)							
LINE TERM	INALS						
PSRR	V _{CC} ref to AGND	50Hz to 3.4KHz	20			dB	
PSRR	V _{SS} ref to AGND		20			dB	
PSRR	V _{bat} ref to AGND		30			dB	
PSRR	BGND ref to AGND		20			dΒ	

RELE DRIVER

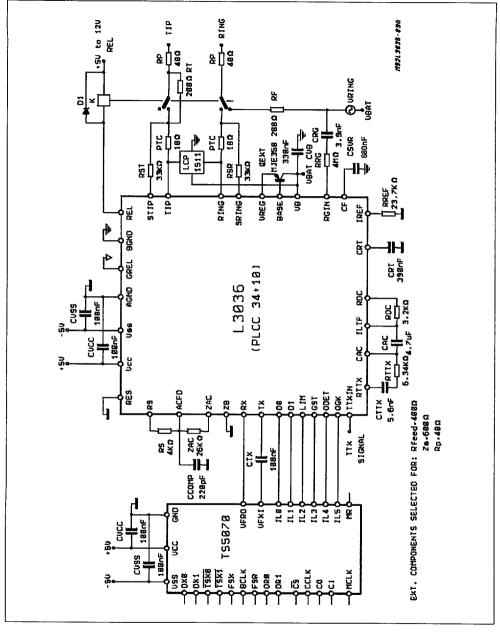
i _{RD}	Current Capability		40		mA
V	Voltage Drop	@I _{RD} = 40mA		1.25	V
İLK	Off Leakage Current			100	μА

Figure 6: Test Circuit



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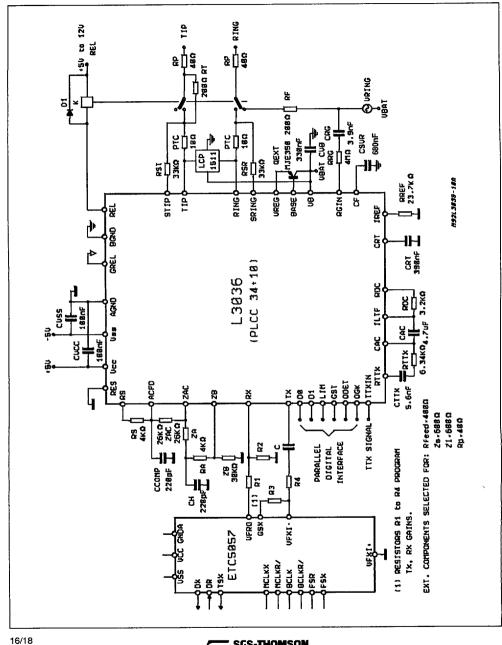
Figure 7: Typical Application with 2nd Generation COMBO (600Ω Application)



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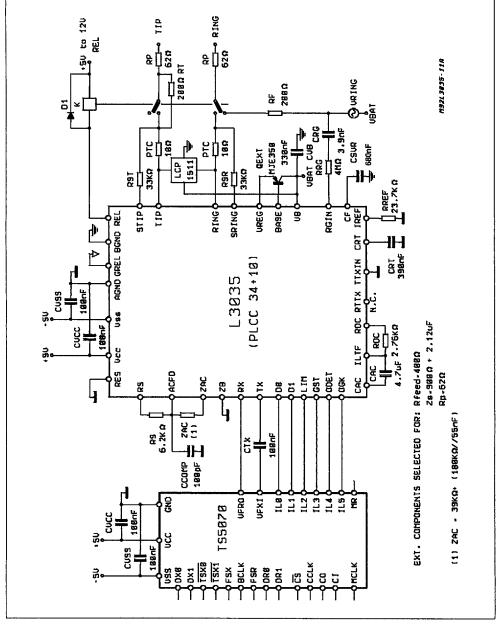
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Figure 8: Typical Application with 1st Generation COMBO (600Ω Application)



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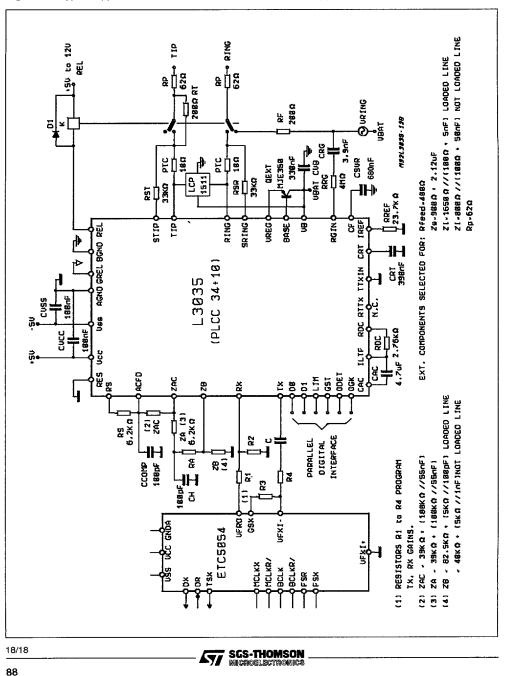
Figure 9: Typical Application with 2nd Generation COMBO (U.S. Application)



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Figure 10: Typical application with 1st Generation COMBO (U.S. Application)



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