

74VCX162374

Low Voltage 16-Bit D-Type Flip-Flop with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in Outputs

General Description

The VCX162374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and output enable ($\overline{OE}$) are common to each byte and can be shorted together for full 16-bit operation.

The VCX162374 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceivers/transmitters.

The 74VCX162374 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX162374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- t_{PD} (CLK to O_n)
 - 3.4 ns max for 3.0V to 3.6V V_{CC}
 - 4.8 ns max for 2.3V to 2.7V V_{CC}
 - 9.6 ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
 - ±12 mA @ 3.0V V_{CC}
 - ±8 mA @ 2.3V V_{CC}
 - ±3 mA @ 1.65V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

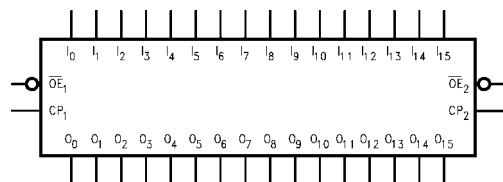
Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Descriptions
74VCX162374MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

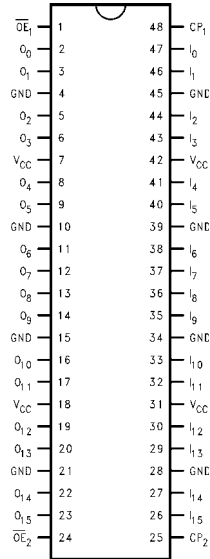
Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
CP_n	Clock Pulse Input
I_0 – I_{15}	Inputs
O_0 – O_{15}	Outputs

Connection Diagram



Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	–0.5V to +4.6V
DC Input Voltage (V_I)	–0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	–0.5V to +4.6V
Outputs Active (Note 3)	–0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
$V_I < 0V$	–50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	–50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	–0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in "OFF" State	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	±12 mA
$V_{CC} = 2.3V$ to 2.7V	±8 mA
$V_{CC} = 1.65V$ to 2.3V	±3 mA
Free Air Operating Temperature (T_A)	–40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < V_{CC} ≤ 3.6V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 – 3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7 – 3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 – 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -6 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -8 \text{ mA}$	3.0	2.4		V
		$I_{OH} = -12 \text{ mA}$	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7 – 3.6		0.2	V
		$I_{OL} = 6 \text{ mA}$	2.7		0.4	V
		$I_{OL} = 8 \text{ mA}$	3.0		0.55	V
		$I_{OL} = 12 \text{ mA}$	3.0		0.8	V
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.7 – 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	2.7 – 3.6		±10	μA
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7 – 3.6		20	μA
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 5)	2.7 – 3.6		±20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 – 3.6		750	μA

Note 5: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($2.3V \leq V_{CC} \leq 2.7V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.6		V
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 – 2.7	$V_{CC} - 0.2$		V
		$I_{OH} = -4 \text{ mA}$	2.3	2.0		V
		$I_{OH} = -6 \text{ mA}$	2.3	1.8		V
		$I_{OH} = -8 \text{ mA}$	2.3	1.7		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 – 2.7		0.2	V
		$I_{OL} = 6 \text{ mA}$	2.3		0.4	V
		$I_{OL} = 8 \text{ mA}$	2.3		0.6	V
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.3 – 2.7		± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH} \text{ or } V_{IL}$	2.3 – 2.7		± 10	μA
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC} \text{ or GND}$	2.3 – 2.7		20	μA
		$V_{CC} \leq (V_I, V_O) \leq 3.6V \text{ (Note 6)}$	2.3 – 2.7		± 20	μA

Note 6: Outputs disabled or 3-STATE only.

DC Electrical Characteristics ($1.65V \leq V_{CC} < 2.3V$)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 2.3	$0.65 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage		1.65 - 2.3		$0.35 \times V_{CC}$	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 2.3	$V_{CC} - 0.2$		V
		$I_{OH} = -3 \text{ mA}$	1.65	1.25		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 2.3		0.2	V
		$I_{OL} = 3 \text{ mA}$	1.65		0.3	V
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.65 - 2.3		± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH} \text{ or } V_{IL}$	1.65 - 2.3		± 10	μA
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC} \text{ or GND}$	1.65 - 2.3		20	μA
		$V_{CC} \leq (V_I, V_O) \leq 3.6V \text{ (Note 7)}$	1.65 - 2.3		± 20	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

(Note 8)

Symbol	Parameter	T _A = −40°C to +85°C, C _L = 30 pF, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	250		200		100		MHz
t _{PHL} , t _{PLH}	Prop Delay CP to O _n	0.8	3.4	1.0	4.8	1.5	9.6	ns
t _{PZL} , t _{PZH}	Output Enable Time	0.8	3.9	1.0	5.4	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	0.8	4.0	1.0	4.4	1.5	7.9	ns
t _S	Setup Time	1.5		1.5		2.5		ns
t _H	Hold Time	1.0		1.0		1.0		ns
t _W	Pulse Width	1.5		1.5		4.0		ns
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 9)		0.5		0.5		0.75	ns

Note 8: For C_L = 50pF, add approximately 300 ps to the AC maximum specification.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

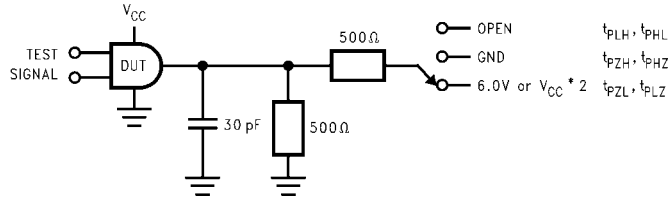
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	0.15 0.25 0.35	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	−0.15 −0.25 −0.35	V
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	1.55 2.05 2.65	V

Capacitance

Symbol	Parameter	Conditions	T _A = +25°C	Units
			Typical	
C _{IN}	Input Capacitance	V _{CC} = 1.8V, 2.5V or 3.3V, V _I = 0V or V _{CC}	6	pF
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V	20	pF

AC Loading and Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$; $1.8V \pm 0.15V$
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

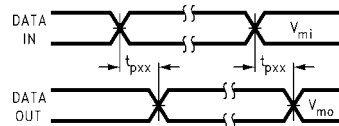


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

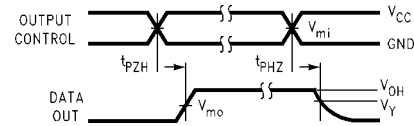


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

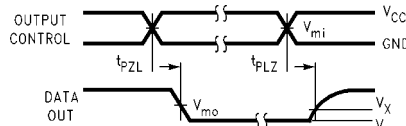


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

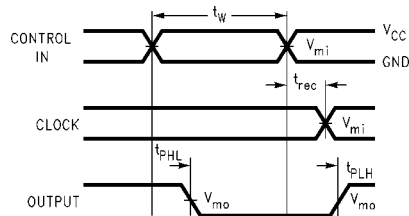


FIGURE 5. Propagation Delay, Pulse Width and t_{REC} Waveforms

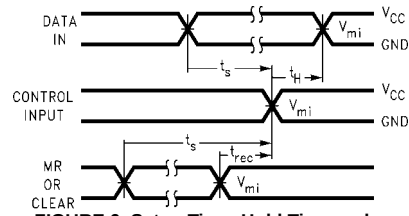
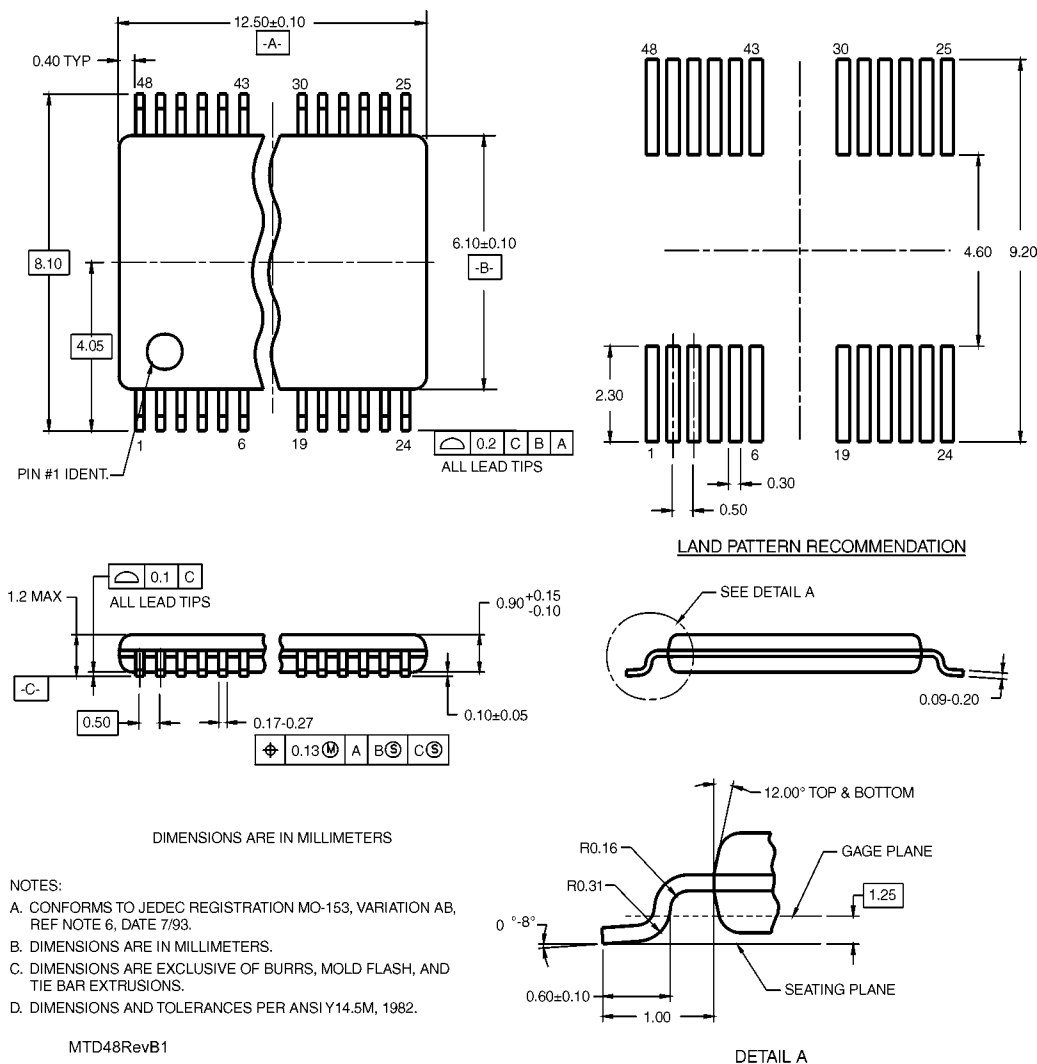


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Body Width
Package Number MTD48**

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