

FEATURES

- High-Speed (15ns), Low Power 16-bit Cascadable ALU
- Implements Add, Subtract, Accumulate, Two's Complement, Pass, and Logic Operations
- All Registers Have a Bypass Path for Complete Flexibility
- DECC SMD No. 5962-89959
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
 - 68-pin Plastic LCC, J-Lead
 - 68-pin Ceramic LCC
 - 68-pin Ceramic PGA

DESCRIPTION

The **L4C381** is a flexible, high speed, cascadable 16-bit Arithmetic and Logic Unit. It combines four 381-type 4-bit ALUs, a look-ahead carry generator, and miscellaneous interface logic — all in a single 68-pin package. While containing new features to support high speed pipelined architectures and single 16-bit bus configurations, the L4C381 retains full performance and functional compatibility with the bipolar '381 designs.

The L4C381 can be cascaded to perform 32-bit or greater operations. See "Cascading the L4C381" toward

the end of this data sheet for more information.

ARCHITECTURE

The L4C381 operates on two 16-bit operands (A and B) and produces a 16-bit result (F). Three select lines control the ALU and provide 3 arithmetic, 3 logical, and 2 initialization functions. Full ALU status is provided to support cascading to longer word lengths. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one of the ALU inputs, accommodating chain operations and accumulation. Furthermore, the A or B input can be forced to Zero allowing unary functions on either operand.

ALU OPERATIONS

The S₂-S₀ lines specify the operation to be performed. The ALU functions and their select codes are shown in Table 1.

The two functions, B minus A and A minus B, can be achieved by setting the carry input of the least significant slice and selecting codes 001 and 010 respectively.

L4C381 BLOCK DIAGRAM

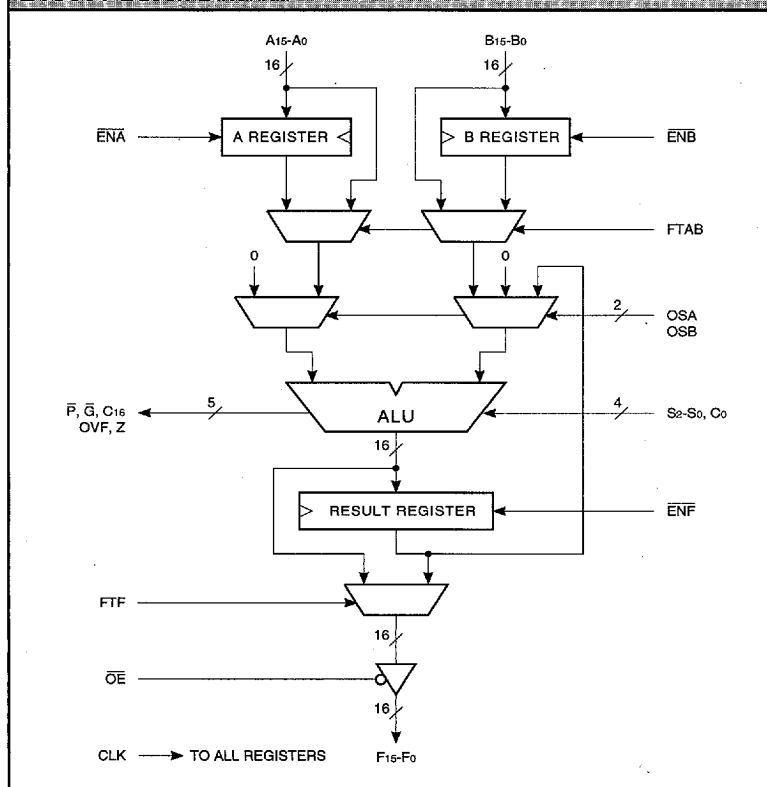


TABLE 1. ALU FUNCTIONS

S ₂ -S ₀	FUNCTION
000	CLEAR (F = 00 ... 00)
001	NOT(A) + B
010	A + NOT(B)
011	A + B
100	A XOR B
101	A OR B
110	A AND B
111	PRESET (F = 11 ... 11)

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Arithmetic Logic Units

ALU STATUS

The ALU provides Overflow and Zero status bits. Carry, Propagate, and Generate outputs are also provided for cascading. These outputs are defined for the three arithmetic functions only. The ALU sets the Zero output when all 16 output bits are zero. The Generate, Propagate, C16, and OVF flags for the A + B operation are defined in Table 2. The status flags produced for NOT(A) + B and A + NOT(B) can be found by complementing Ai and Bi respectively in Table 2.

OPERAND REGISTERS

The L4C381 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. The A register is enabled for input by setting the $\overline{\text{ENA}}$ control LOW, and the B register is enabled for input by setting the $\overline{\text{ENB}}$ control LOW. When either the $\overline{\text{ENA}}$ control or $\overline{\text{ENB}}$ control is HIGH, the data in the corresponding input register will not change.

This architecture allows the L4C381 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be bypassed with the FTAB control line. When the FTAB control is asserted (FTAB = HIGH), data is routed around the A and B input registers; however, they continue to function normally via the $\overline{\text{ENA}}$ and $\overline{\text{ENB}}$ controls. The contents of the input registers will again be available to the ALU if the FTAB control is released.

OUTPUT REGISTER

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. When the $\overline{\text{ENF}}$ control is LOW, data from the ALU will be clocked into the

TABLE 2. ALU STATUS FLAGS

Bit Carry Generate	= $g_i = A_i B_i$	for $i = 0 \dots 15$
Bit Carry Propagate	= $p_i = A_i + B_i$	for $i = 0 \dots 15$
P_0	= p_0	
P_i	= $p_i (P_{i-1})$	for $i = 1 \dots 15$
and		
G_0	= g_0	
G_i	= $g_i + p_i (G_{i-1})$	for $i = 1 \dots 15$
C_i	= $G_{i-1} + P_{i-1} (C_0)$	for $i = 1 \dots 15$
then		
\overline{G}	= NOT(G_{15})	
\overline{P}	= NOT(P_{15})	
C_{16}	= $G_{15} + P_{15} C_0$	
OVF	= $C_{15} \text{ XOR } C_{16}$	

output register. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the $\overline{\text{OE}}$ input allow the L4C381 to be configured in a single bidirectional bus system.

The output register can be bypassed by asserting the FTF control signal (FTF = HIGH). When the FTF control is asserted, output data is routed around the output register, however, it continues to function normally via the $\overline{\text{ENF}}$ control. The contents of the output register will again be available on the output pins if FTF is released. With both FTAB and FTF true (HIGH) the L4C381 is functionally identical to four cascaded 54S381-type devices.

OPERAND SELECTION

The two operand select lines, OSA and OSB, control multiplexers that precede the ALU inputs. These multiplexers provide an operand force-to-zero function as well as F register feedback to the B input. Table 3 shows the inputs to the ALU as a function of the operand select inputs. Either the A or B operands may be forced to zero.

TABLE 3. OPERAND SELECTION

OSB	OSA	OPERAND B	OPERAND A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

When both operand select lines are low, the L4C381 is configured as a chain calculation ALU. The registered ALU output is passed back to the B input to the ALU. This allows accumulation operations to be performed by providing new operands via the A input port. The accumulator can be preloaded from the A input by setting OSA true. By forcing the function select lines to the CLEAR state (000), the accumulator may be cleared. Note that this feedback operation is not affected by the state of the FTF control. That is, the F outputs of the L4C381 may be driven directly by the ALU. The output register continues to function, however, and provides the ALU B operand source.

MAXIMUM RATINGS Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V _{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V _{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V _{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS Over Operating Conditions (Note 4)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = –2.0 mA	2.4			V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 8.0 mA			0.5	V
V _{IH}	Input High Voltage		2.0		V _{CC}	V
V _{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I _{IX}	Input Current	Ground ≤ V _{IN} ≤ V _{CC} (Note 12)			±20	µA
I _{OZ}	Output Leakage Current	Ground ≤ V _{OUT} ≤ V _{CC} (Note 12)			±20	µA
I _{CC1}	V _{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I _{CC2}	V _{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS <i>Notes 9, 10 (ns)</i>												
To Output From Input	L4C381-55				L4C381-40				L4C381-26			
	F15-F0	P, G	OVF, Z	C16	F15-F0	P, G	OVF, Z	C16	F15-F0	P, G	OVF, Z	C16
FTAB = 0, FTF = 0												
Clock	32	38	53	36	26	30	44	32	22	22	26	22
C0	—	—	34	22	—	—	28	20	—	—	18	18
S2-S0, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 0, FTF = 1												
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C0	37	—	34	22	30	—	28	20	22	—	18	18
S2-S0, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22
FTAB = 1, FTF = 0												
A15-A0, B15-B0	—	36	46	37	—	30	40	32	—	22	22	22
Clock	32	—	—	—	26	—	—	—	22	—	—	—
C0	—	—	34	22	—	—	28	20	—	—	18	18
S2-S0, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 1, FTF = 1												
A15-A0, B15-B0	55	36	46	37	40	30	40	32	26	22	22	22
Clock (OSA, OSB = 0)	56	38	53	36	46	30	44	32	28	22	26	22
C0	37	—	34	22	30	—	28	20	22	—	18	18
S2-S0, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE <i>Notes 9, 10 (ns)</i>												
Input	L4C381-55				L4C381-40				L4C381-26			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A15-A0, B15-B0	8	2	35	2	8	2	28	2	8	2	16	2
C0	21	0	21	0	16	0	16	0	8	0	8	0
S2-S0, OSA, OSB	44	0	44	0	32	0	32	0	18	0	18	0
ENA, ENB, ENF	10	2	10	2	10	2	10	2	8	2	8	2

TRI-STATE ENABLE/DISABLE TIMES <i>Notes 9, 10, 11 (ns)</i>			
	L4C381-55	L4C381-40	L4C381-26
t _{ENA}	20	18	16
t _{DIS}	20	18	16

CLOCK CYCLE TIME AND PULSE WIDTH <i>Notes 9, 10 (ns)</i>			
	L4C381-55	L4C381-40	L4C381-26
Minimum Cycle Time	43	34	20
Highgoing Pulse	15	10	10
Lowgoing Pulse	15	10	10

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Arithmetic Logic Units

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)
GUARANTEED MAXIMUM COMBINATIONAL DELAYS Notes 9, 10 (ns)

To Output From Input	L4C381-20				L4C381-15				
	F15-F0	P, G	OVF, Z	C16	F15-F0	P, G	OVF, Z	C16	
FTAB = 0, FTF = 0									
Clock	11	20	20	20	11	15	15	15	
Co	—	—	14	14	—	—	13	13	
S2-S0, OSA, OSB	—	18	20	18	—	14	15	14	
FTAB = 0, FTF = 1									
Clock	20	20	20	20	15	15	15	15	
Co	18	—	14	14	14	—	13	13	
S2-S0, OSA, OSB	20	18	20	18	15	14	15	14	
FTAB = 1, FTF = 0									
A15-A0, B15-B0	—	16	20	17	—	14	15	14	
Clock	11	—	—	—	11	—	—	—	
Co	—	—	14	14	—	—	13	13	
S2-S0, OSA, OSB	—	18	20	18	—	14	15	14	
FTAB = 1, FTF = 1									
A15-A0, B15-B0	20	16	20	17	15	14	15	14	
Clock (OSA, OSB = 0)	20	20	20	20	15	15	15	15	
Co	18	—	14	14	14	—	13	13	
S2-S0, OSA, OSB	20	18	20	18	15	14	15	14	

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE Notes 9, 10 (ns)

Input	L4C381-20				L4C381-15					
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1			
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold		
A15-A0, B15-B0	5	0	14	0	5	0	12	0		
Co	12	0	12	0	10	0	10	0		
S2-S0, OSA, OSB	15	0	15	0	12	0	12	0		
EN \bar{A} , EN \bar{B} , EN \bar{F}	5	0	5	0	5	0	5	0		

TRI-STATE ENABLE/DISABLE TIMES Notes 9, 10, 11 (ns)

	L4C381-20	L4C381-15	
t _{ENA}	8	6	
t _{DIS}	8	6	

CLOCK CYCLE TIME AND PULSE WIDTH Notes 9, 10 (ns)

	L4C381-20	L4C381-15	
Minimum Cycle Time	18	14	
Highgoing Pulse	5	4	
Lowgoing Pulse	5	4	

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Arithmetic Logic Units

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS <i>Notes 9, 10 (ns)</i>												
To Output From Input	L4C381-65				L4C381-45				L4C381-30			
	F15-F0	P, \bar{G}	OVF, Z	C16	F15-F0	P, \bar{G}	OVF, Z	C16	F15-F0	P, \bar{G}	OVF, Z	C16
FTAB = 0, FTF = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C ₀	—	—	42	25	—	—	32	23	—	—	22	22
S2-S ₀ , OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 0, FTF = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C ₀	42	—	42	25	32	—	32	23	26	—	22	22
S2-S ₀ , OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28
FTAB = 1, FTF = 0												
A15-A ₀ , B15-B ₀	—	44	56	44	—	32	46	36	—	28	28	28
Clock	37	—	—	—	28	—	—	—	26	—	—	—
C ₀	—	—	42	25	—	—	32	23	—	—	22	22
S2-S ₀ , OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 1, FTF = 1												
A15-A ₀ , B15-B ₀	65	44	56	44	45	32	46	36	30	28	28	28
Clock (OSA, OSB = 0)	68	44	63	45	56	34	50	34	34	28	34	28
C ₀	42	—	42	25	32	—	32	23	26	—	22	22
S2-S ₀ , OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C381-65				L4C381-45				L4C381-30			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A15-A ₀ , B15-B ₀	10	3	43	3	8	3	33	3	8	3	20	3
C ₀	25	0	25	0	20	0	20	0	12	0	12	0
S2-S ₀ , OSA, OSB	50	0	50	0	36	0	36	0	20	0	20	0
EN _A , EN _B , EN _F	12	2	12	2	10	2	10	2	10	2	10	2

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-65	L4C381-45	L4C381-30
t _{ENA}	22	20	18
t _{DIS}	22	20	18

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-65	L4C381-45	L4C381-30
Minimum Cycle Time	52	38	26
Highgoing Pulse	20	15	12
Lowgoing Pulse	20	15	12

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS Notes 9, 10 (ns)

To Output From Input	L4C381-25				L4C381-20				
	F15-F0	P, G	OVF, Z	C16	F15-F0	P, G	OVF, Z	C16	
FTAB = 0, FTF = 0									
Clock	14	24	24	24	14	20	20	20	
C0	—	—	18	18	—	—	16	16	
S2-S0, OSA, OSB	—	22	24	22	—	18	20	18	
FTAB = 0, FTF = 1									
Clock	25	24	24	24	20	20	20	20	
C0	21	—	18	18	17	—	16	16	
S2-S0, OSA, OSB	25	22	24	22	20	18	20	18	
FTAB = 1, FTF = 0									
A15-A0, B15-B0	—	20	25	22	—	17	20	17	
Clock	14	—	—	—	14	—	—	—	
C0	—	—	18	18	—	—	16	16	
S2-S0, OSA, OSB	—	22	24	22	—	18	20	18	
FTAB = 1, FTF = 1									
A15-A0, B15-B0	25	20	25	22	20	17	20	17	
Clock (OSA, OSB = 0)	25	24	24	24	20	20	20	20	
C0	21	—	18	18	17	—	16	16	
S2-S0, OSA, OSB	25	22	24	22	20	18	20	18	

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE Notes 9, 10 (ns)

Input	L4C381-25				L4C381-20					
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1			
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold		
A15-A0, B15-B0	7	2	14	2	6	2	12	2		
C0	14	0	14	0	12	0	12	0		
S2-S0, OSA, OSB	19	0	19	0	16	0	16	0		
ENA, ENB, ENF	7	0	7	0	6	0	6	0		

TRI-STATE ENABLE/DISABLE TIMES Notes 9, 10, 11 (ns)

	L4C381-25	L4C381-20	
tENA	14	10	
tDIS	14	10	

CLOCK CYCLE TIME AND PULSE WIDTH Notes 9, 10 (ns)

	L4C381-25	L4C381-20	
Minimum Cycle Time	20	18	
Highgoing Pulse	8	6	
Lowgoing Pulse	8	6	

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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

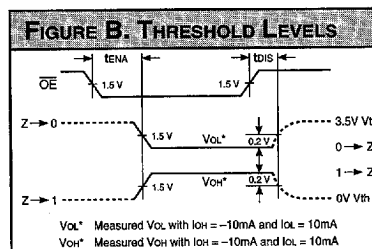
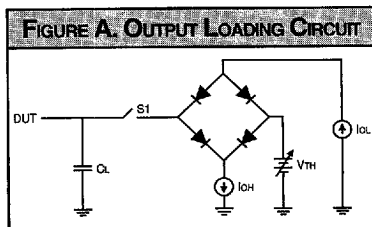
b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the tENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the tDIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.



CASCADING THE L4C381

Cascading the L4C381 to 32 bits is accomplished simply by connecting the C16 output of the least significant slice to the C0 input of the most significant slice. The S2-S0, OSA, OSB, $\overline{\text{ENA}}$, $\overline{\text{ENB}}$, and $\overline{\text{ENF}}$ lines are common to both devices. The Zero output flags should be logically ANDed to produce the Zero flag for the 32-bit result. The OVF and C16 outputs of the most significant slice are valid for the 32-bit result.

Propagation delay calculations for this configuration require two steps: First determine the propagation delay from the input of interest to the C16 output of the lower slice. Add this number to the delay from the C0 input of the upper slice to the output of interest

(of the C0 setup time, if the F register is used). The sum gives the overall input-to-output delay (or setup time) for the 32-bit configuration. This method gives a conservative result, since the C16 output is very lightly loaded. Formulas for calculation of all critical delays for a 32-bit system are shown in Figures 4A through 4D.

Cascading to greater than 32 bits can be accomplished in two ways: The simplest (but slowest) method is to simply connect the C16 output of each slice to the C0 input of the next more significant slice. Propagation delays are calculated as for the 32-bit case, except that the C0 to C16 delays for all intermediate slices must be added to the overall delay for each path. A

faster method is to use an external carry-lookahead generator. The $\overline{\text{P}}$ and $\overline{\text{G}}$ outputs of each slice are connected as inputs to the CLA generator, which in turn produces the C0 inputs for each slice except the least significant. The C16 outputs are not used in this case, except for the most significant one, which is the carry out of the overall system. The carry in to the system is connected to the C0 input of the least significant slice, and also to the carry lookahead generator. Propagation delays for this configuration are the sum of the time to $\overline{\text{P}}$, $\overline{\text{G}}$, for the least significant slice, the propagation delay of the carry lookahead generator, and the C0 to output time of the most significant slice.

16-bit Cascadable ALU

FIGURE 4A. FTAB = 0, FTF = 0

From	To	Calculated Specification Limit
Clock	→ F	= Same as 16-bit case
Clock	→ Other	= (Clock → C16) + (C0 → Out)
Co	→ Other	= (Co → C16) + (C0 → Out)
S2-S0, OSA, OSB	→ Other	= (S2-S0, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	= Same as 16-bit case
Co	Setup time	= (Co → C16) + (Co Setup time)
S2-S0, OSA, OSB	Setup time	= (S2-S0, OSA, OSB → C16) + (C0 Setup time)
ENA, ENB, ENF	Setup time	= Same as 16-bit case
Minimum cycle time		= (Clock → C16) + (C0 Setup time)

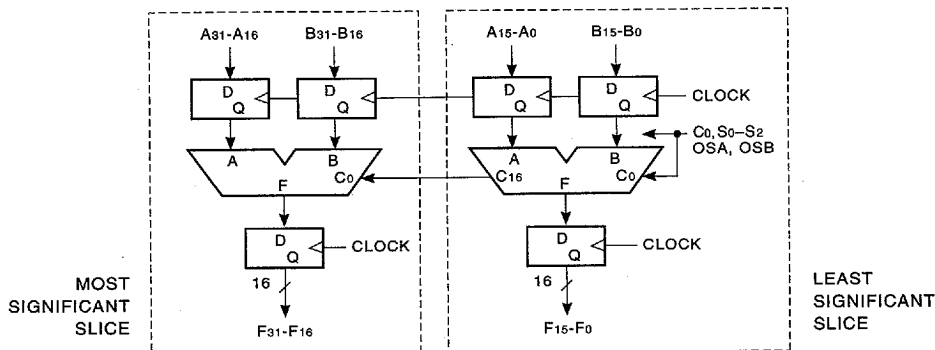


FIGURE 4B. FTAB = 0, FTF = 1

From	To	Calculated Specification Limit
Clock	→ F	$(\text{Clock} \rightarrow C_{16}) + (C_0 \rightarrow F)$
Clock	→ Other	$(\text{Clock} \rightarrow C_{16}) + (C_0 \rightarrow \text{Out})$
C ₀	→ F	$(C_0 \rightarrow C_{16}) + (C_0 \rightarrow F)$
C ₀	→ Other	$(C_0 \rightarrow C_{16}) + (C_0 \rightarrow \text{Out})$
S ₂ -S ₀ , OSA, OSB	→ F	$(S_2-S_0, \text{OSA}, \text{OSB} \rightarrow C_{16}) + (C_0 \rightarrow F)$
S ₂ -S ₀ , OSA, OSB	→ Other	$(S_2-S_0, \text{OSA}, \text{OSB} \rightarrow C_{16}) + (C_0 \rightarrow \text{Out})$
A, B	Setup time	= Same as 16-bit case
C ₀	Setup time	$(C_0 \rightarrow C_{16}) + (C_0 \text{ Setup time})$
S ₂ -S ₀ , OSA, OSB	Setup time	$(S_2-S_0, \text{OSA}, \text{OSB} \rightarrow C_{16}) + (C_0 \text{ Setup time})$
EN _A , EN _B , EN _F	Setup time	= Same as 16-bit case
Minimum cycle time		$(\text{Clock} \rightarrow C_{16}) + (C_0 \text{ Setup time})$

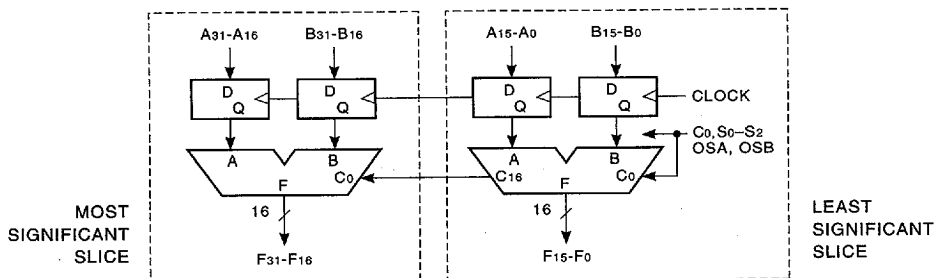
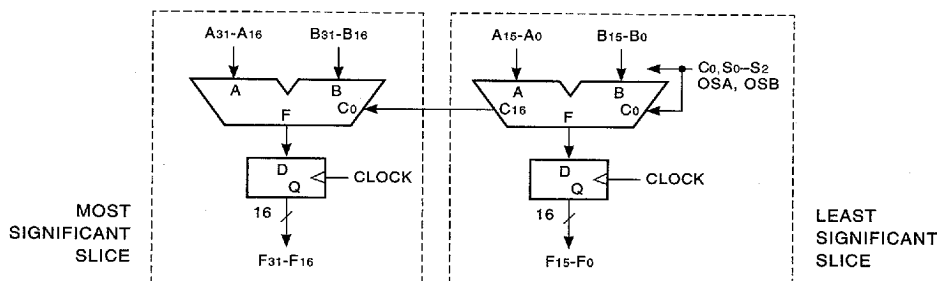


FIGURE 4C. FTAB = 1, FTF = 0

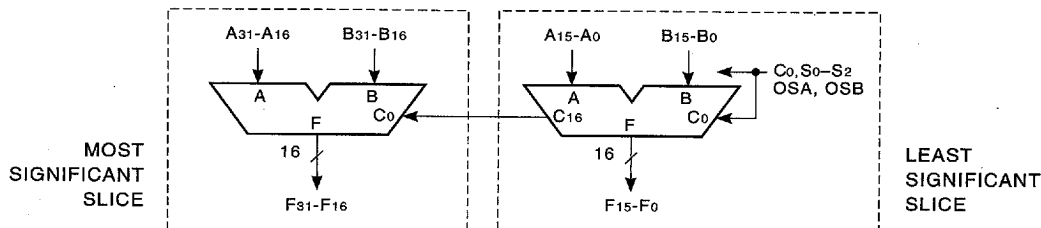
From	To	Calculated Specification Limit
Clock	→ F	= Same as 16-bit case
A, B	→ Other	= (A, B → C ₁₆) + (C ₀ → Out)
C ₀	→ Other	= (C ₀ → C ₁₆) + (C ₀ → Out)
S ₂ -S ₀ , OSA, OSB	→ Other	= (S ₂ -S ₀ , OSA, OSB → C ₁₆) + (C ₀ → Out)
A, B	Setup time	= (A, B → C ₁₆) + (C ₀ Setup time)
C ₀	Setup time	= (C ₀ → C ₁₆) + (C ₀ Setup time)
S ₂ -S ₀ , OSA, OSB	Setup time	= (S ₂ -S ₀ , OSA, OSB → C ₁₆) + (C ₀ Setup time)
ENA, ENB, ENF	Setup time	= Same as 16-bit case
Minimum cycle time (F register accumulate loop)	Setup time	= (Clock → C ₁₆) + (C ₀ Setup time)



3

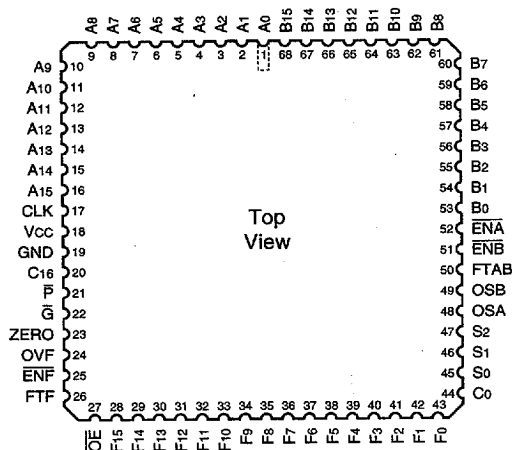
FIGURE 4D. FTAB = 1, FTF = 1

From	To	Calculated Specification Limit
A, B	→ F	= (A, B → C ₁₆) + (C ₀ → F)
A, B	→ Other	= (A, B → C ₁₆) + (C ₀ → Out)
C ₀	→ F	= (C ₀ → C ₁₆) + (C ₀ → F)
C ₀	→ Other	= (C ₀ → C ₁₆) + (C ₀ → Out)
S ₂ -S ₀ , OSA, OSB	→ F	= (S ₂ -S ₀ , OSA, OSB → C ₁₆) + (C ₀ → F)
S ₂ -S ₀ , OSA, OSB	→ Other	= (S ₂ -S ₀ , OSA, OSB → C ₁₆) + (C ₀ → Out)
A, B	Setup time	= (A, B → C ₁₆) + (C ₀ Setup time)
C ₀	Setup time	= (C ₀ → C ₁₆) + (C ₀ Setup time)
S ₂ -S ₀ , OSA, OSB	Setup time	= (S ₂ -S ₀ , OSA, OSB → C ₁₆) + (C ₀ Setup time)
ENA, ENB, ENF	Setup time	= Same as 16-bit case
Minimum cycle time (F register accumulate loop)	Setup time	= (Clock → C ₁₆) + (C ₀ Setup time)

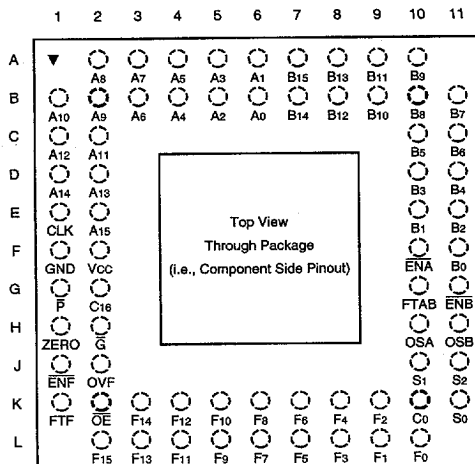


ORDERING INFORMATION

68-pin



68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Ceramic Pin Grid Array (G1)
0°C to +70°C — COMMERCIAL SCREENING			
55 ns	L4C381JC55	L4C381KC55	L4C381GC55
40 ns	L4C381JC40	L4C381KC40	L4C381GC40
26 ns	L4C381JC26	L4C381KC26	L4C381GC26
20 ns	L4C381JC20	L4C381KC20	L4C381GC20
15 ns	L4C381JC15	L4C381KC15	L4C381GC15
-55°C to +125°C — COMMERCIAL SCREENING			
65 ns		L4C381KM65	L4C381GM65
45 ns		L4C381KM45	L4C381GM45
30 ns		L4C381KM30	L4C381GM30
25 ns		L4C381KM25	L4C381GM25
20 ns		L4C381KM20	L4C381GM20
-55°C to +125°C — MIL-STD-883 COMPLIANT			
65 ns		L4C381KMB65	L4C381GMB65
45 ns		L4C381KMB45	L4C381GMB45
30 ns		L4C381KMB30	L4C381GMB30
25 ns		L4C381KMB25	L4C381GMB25
20 ns		L4C381KMB20	L4C381GMB20

5565905 0003930 540 Arithmetic Logic Units