A DIVISION OF CIRRUS LOGIC

# CS5322
# CS5323

# 24-Bit Variable Bandwidth A/D Converter

## Features

- Monolithic CMOS A/D Converter
- Dynamic Range
  - 130 dB @ 25 Hz Bandwidth
  - 120 dB @ 411 Hz Bandwidth
- Delta-Sigma Architecture
  - Variable Oversampling: 64X to 4096X
  - Internal Track-and-Hold Amplifier
- Flexible Filter Chip
  - Hardware or Software Selectable Options
  - Seven Selectable Filter Corner (-3dB) Frequencies: 25, 51, 102, 205, 411, 824 and 1650 Hz
- Low Power Dissipation: <100 mW

## Description

The CS5323 analog modulator and the CS5322 digital filter function together as a unique high resolution A/D converter intended for geophysical and other applications which require high dynamic range. The CS5323/CS5322 combination performs sampling, A/D conversion, and anti-alias filtering.

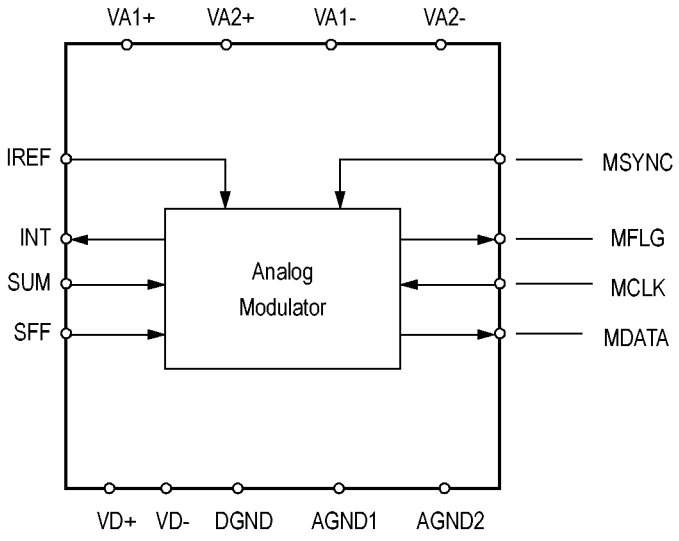
The pair use Delta-Sigma modulation to produce highly accurate conversions. The CS5323 oversamples, virtually eliminating the need for external anti-alias filters. The CS5322 linear-phase FIR digital filter decimates the output to any one of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format.

The CMOS design of the CS5322/CS5323 achieves high reliability while minimizing power dissipation.

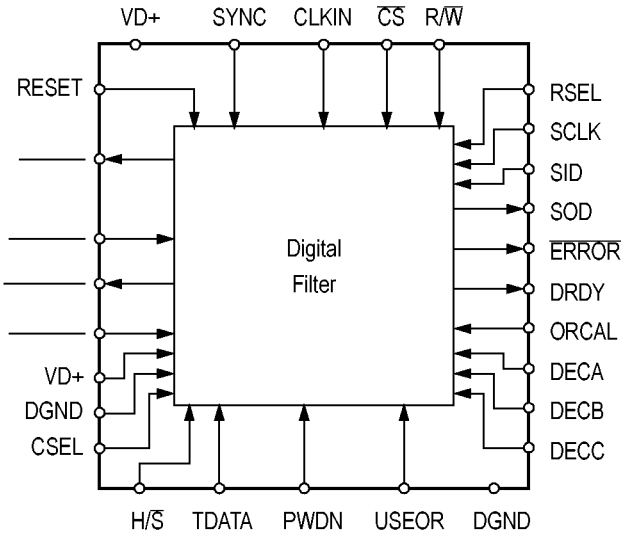
**ORDERING INFORMATION**

| | | |
|---|---|---|
| CS5322-KL | 0° to +70° C | 28-pin PLCC |
| CS5322-BL | -40° to +85° C | 28-pin PLCC |
| CS5323-KL | 0° to +70° C | 28-pin PLCC |
| CS5323-BL | -40° to +85° C | 28-pin PLCC |

**CS5323**




**CS5322**





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## ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to $T_{MAX}$; VA-, VD- = -5V; VA+, VD+ = 5V; AGND = 0V; CLKIN = 1.024 MHz; Device connected as shown in Figure 16; Logic 1 = VD+, Logic 0 = 0V; unless otherwise specified.)

| Parameter* | | Symbol | CS5323-K Min | CS5323-K Typ | CS5323-K Max | CS5323-B Min | CS5323-B Typ | CS5323-B Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| Specified Temperature Range | | | 0 | - | +70 | -40 | - | +85 | °C |
| ***Dynamic Performance*** | | | | | | | | | |
| Dynamic Range | (Note 1) | DR | | | | | | | |
| CLKIN = 1.024 MHz: | $f_O$ = 4000 Hz | | - | 103 | - | - | 103 | - | dB |
| | $f_O$ = 2000 Hz | | - | 118 | - | - | 118 | - | dB |
| | $f_O$ = 1000 Hz | | 116 | 121 | - | 116 | 121 | - | dB |
| | $f_O$ = 500 Hz | | - | 124 | - | - | 124 | - | dB |
| | $f_O$ = 250 Hz | | - | 127 | - | - | 127 | - | dB |
| | $f_O$ = 125 Hz | | - | 129 | - | - | 129 | - | dB |
| | $f_O$ = 62.5 Hz | | - | 130 | - | - | 130 | - | dB |
| CLKIN = 512 kHz: | $f_O$ = 2000 Hz | | - | 99 | - | - | 99 | - | dB |
| | $f_O$ = 1000 Hz | | - | 121 | - | - | 121 | - | dB |
| | $f_O$ = 500 Hz | | - | 125 | - | - | 125 | - | dB |
| | $f_O$ = 250 Hz | | - | 127 | - | - | 127 | - | dB |
| | $f_O$ = 125 Hz | | - | 130 | - | - | 130 | - | dB |
| | $f_O$ = 62.5 Hz | | - | 132 | - | - | 132 | - | dB |
| | $f_O$ = 31.25 Hz | | - | 133 | - | - | 133 | - | dB |
| Signal-to-Distortion: | (Note 2) | SDR | | | | | | | |
| | CLKIN = 1.024MHz | | 100 | 110 | - | 100 | 110 | - | dB |
| | CLKIN = 512 kHz | | - | 120 | - | - | 120 | - | dB |
| Intermodulation Distortion | (Note 3) | IMD | - | 110 | - | - | 110 | - | dB |
| ***dc Accuracy*** | | | | | | | | | |
| Full Scale Error | (Note 4) | FSE | - | - | 4 | - | - | 4 | % |
| Full Scale Drift | (Notes 4, 5) | $TC_{FS}$ | - | 0.005 | - | - | 0.005 | - | %/°C |
| Offset | (Note 4) | $V_{ZSE}$ | - | - | 250 | - | - | 250 | mV |
| Offset after Calibration | (Note 6) | | - | ±100 | - | - | ±100 | - | µV |
| Offset Calibration Range | (Note 7) | | - | 100 | - | - | 100 | - | %F.S. |
| Offset Drift | (Notes 4, 5) | $TC_{ZSE}$ | - | 500 | - | - | 500 | - | µV/°C |

Notes:
1. fo = CS5322 output word rate. Refer to CS5322 Filter Characteristics for details.
2. Tested with full scale input signal of 50 Hz; fo = 500 Hz.
3. Tested with input signals of 30 Hz and 50 Hz, each 6 dB down from full scale fo = 500 Hz.
4. Specification is for the parameter over the specified temperature range and is for the CS5323 device only (IREF = 1 mA). It does not include the effects of external components.
5. Drift specifications are guaranteed by design and characterization.
6. The offset after calibration specification applies to the effective offset voltage for a ±10 volt input to the CS5323 modulator, but is relative to the output digital codes from the CS5322 after ORCAL and USEOR have been made active.
7. The CS5322 offset calibration is performed digitally and includes ± full scale (±10 volts into CS5323). Calibration of offsets greater than ±10% of full scale will begin to subtract from the dynamic range.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

## ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to $T_{MAX}$; VA-, VD- = -5V; VA+, VD+ = 5V; AGND = 0V; CLKIN = 1.024 MHz; Device connected as shown in Figure 16; Logic 1 = VD+, Logic 0 = 0V; unless otherwise specified.)

| Parameter* | Symbol | CS5323-K Min | CS5323-K Typ | CS5323-K Max | CS5323-B Min | CS5323-B Typ | CS5323-B Max | Units |
|---|---|---|---|---|---|---|---|---|
| Specified Temperature Range | | 0 | - | +70 | -40 | - | +85 | °C |
| ***Input Characteristics*** | | | | | | | | |
| Input Signal Frequencies (Note 8) | BW | dc | - | 1500 | dc | - | 1500 | Hz |
| Input Voltage Range (Note 9) | $V_{IN}$ | -10.0 | - | +10.0 | -10.0 | - | +10.0 | V |
| Input Overrange Voltage (Note 9) | $I_{OVR}$ | - | - | 10 | - | - | 10 | %F.S. |
| ***Power Supplies*** | | | | | | | | |
| DC Power Supply Currents (Note 10) | | | | | | | | |
| Positive Supplies (IA+ and ID+) | | - | 7.0 | 10.0 | - | 7.0 | 10.0 | mA |
| Negative Supplies (IA- and ID-) | | - | 8.4 | 10.0 | - | 8.4 | 10.0 | mA |
| Power Consumption (Note 10) | | | | | | | | |
| PWDN Low | $P_{DN}$ | - | 77 | 100 | - | 77 | 100 | mW |
| PWDN High | $P_{DS}$ | - | 0.01 | 10 | - | 0.01 | 10 | mW |
| Power Supply Rejection (Notes 11, 12) | PSR | | | | | | | |
| (dc to f1 Hz): | | | | | | | | |
| VA+ | | - | 60 | - | - | 60 | - | dB |
| VA- | | - | 45 | - | - | 45 | - | dB |
| VD+ | | - | 45 | - | - | 45 | - | dB |
| VD- | | - | 40 | - | - | 40 | - | dB |
| (f1 Hz to 128 kHz): | | | | | | | | |
| VA+ | | - | 60 | - | - | 60 | - | dB |
| VA- | | - | 60 | - | - | 60 | - | dB |
| VD+ | | - | 60 | - | - | 60 | - | dB |
| VD- | | - | 60 | - | - | 60 | - | dB |

Notes:
8. The upper bandwidth limit is determined by the CS5322 digital filter.
9. This input voltage range is for the configuration shown in Figure 16, the System Connection Diagram, and applies to signal from dc to f3 Hz. Refer to CS5322 Filter Characteristics for the values of f3.
10. All outputs unloaded. All logic inputs forced to VA+ or GND respectively. Power down mode power consumption is with the signal source and the voltage reference source either grounded or floating.
11. Tested with a 100 mVp-p sine wave applied separately to each supply (VA1 and VA2 are considered as one input for this test).
12. Refer to CS5322 Filter Characteristics table for the values of f1.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

## FILTER CHARACTERISTICS ($T_A$ = $T_{min}$ to $T_{max}$; VD+ = 5V; GND = 0V; CLKIN = 1.024 MHz; transfer function shown in Figure 2; unless otherwise specified.)

| Output Word Rate $f_0$ (Hz) | Passband f1 (Hz) | Passband Flatness $R_{PB}$ (dB) | -3dB Freq. f2 (Hz) | Stopband f3 (Hz) (Note 13) | Group Delay (ms) |
|---|---|---|---|---|---|
| 4000 | 1500 | 0.2 | 1652.5 | 2000 | 7.25 |
| 2000 | 750 | 0.04 | 824.3 | 1000 | 14.5 |
| 1000 | 375 | 0.08 | 411.9 | 500 | 29 |
| 500 | 187.5 | 0.1 | 205.9 | 250 | 58 |
| 250 | 93.8 | 0.1 | 102.9 | 125 | 116 |
| 125 | 46.9 | 0.1 | 51.5 | 62.5 | 232 |
| 62.5 | 23.4 | 0.1 | 25.7 | 31.25 | 464 |

Note: 13. $G_{SB}$ = -130 dB for all Output Word Rates.

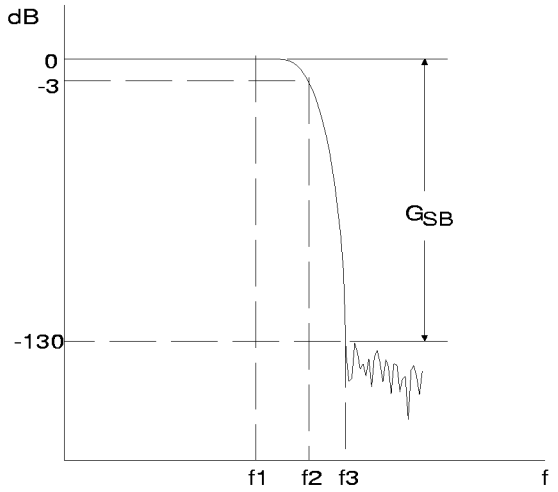



**Figure 1. CS5322 Filter Response**

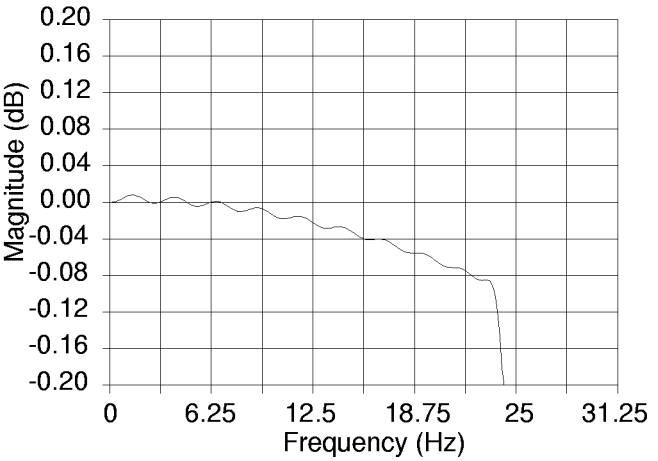



**Figure 2. CS5322 Digital Filter Passband Ripple $f_0$ = 62.5 Hz**

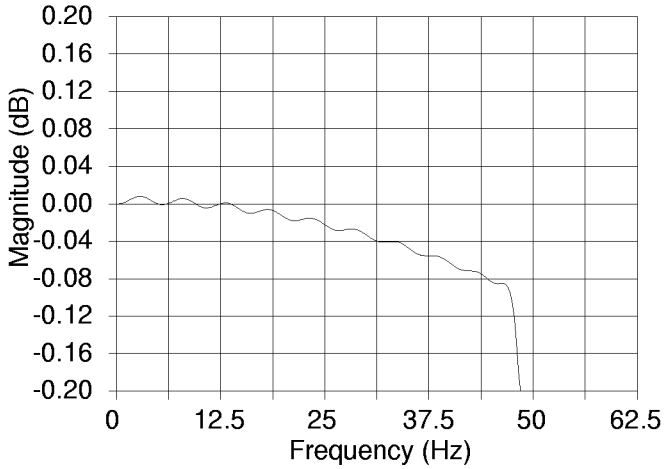



**Figure 3. CS5322 Digital Filter Passband Ripple $f_0$ = 125 Hz**

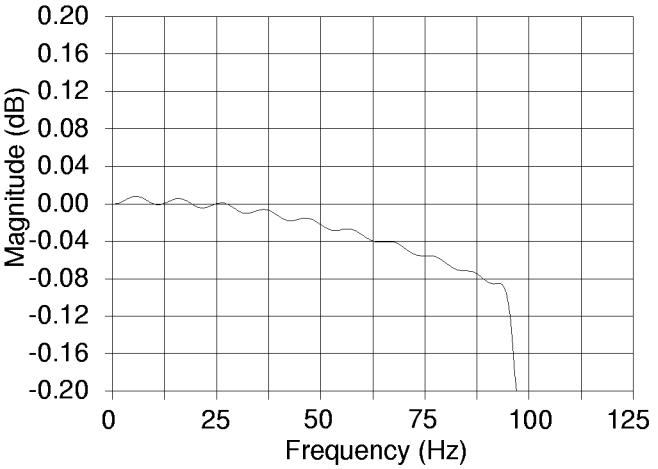



**Figure 4. CS5322 Digital Filter Passband Ripple $f_0$ = 250 Hz**

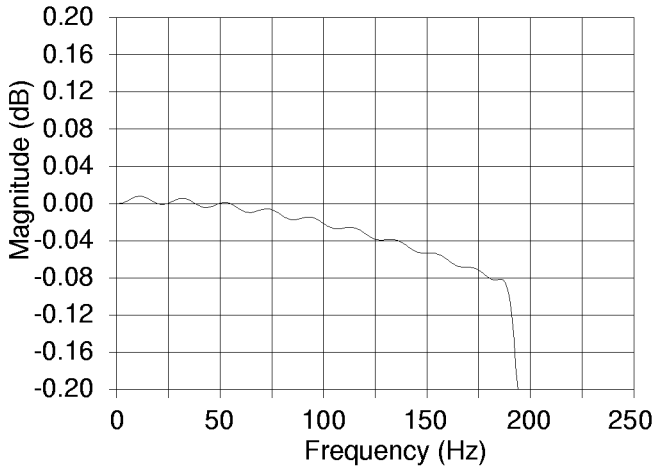



**Figure 5. CS5322 Digital Filter Passband Ripple $f_0$ = 500 Hz**

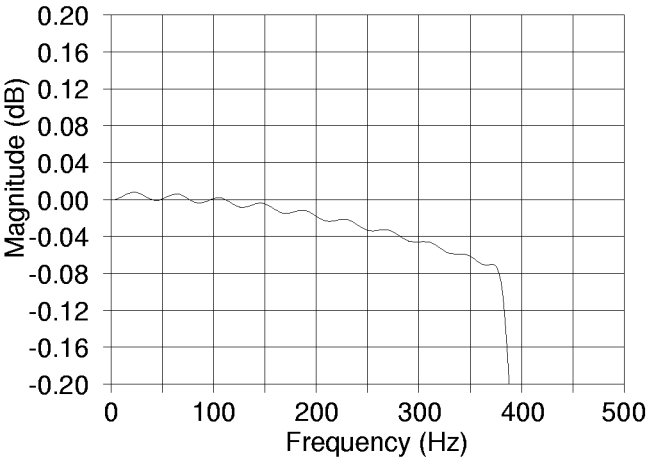



**Figure 6. CS5322 Digital Filter Passband Ripple $f_0$ = 1000 Hz**

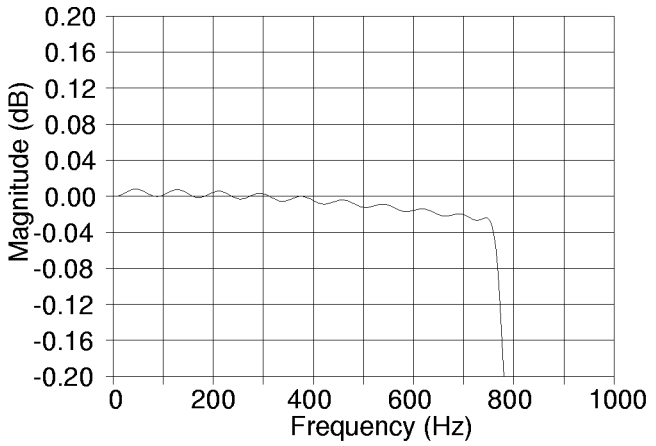



**Figure 7. CS5322 Digital Filter Passband Ripple $f_0$ = 2000 Hz**

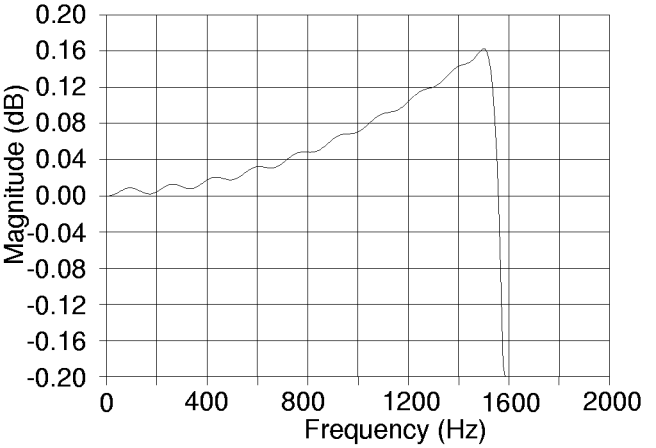



**Figure 8. CS5322 Digital Filter Passband Ripple $f_0$ = 4000 Hz**

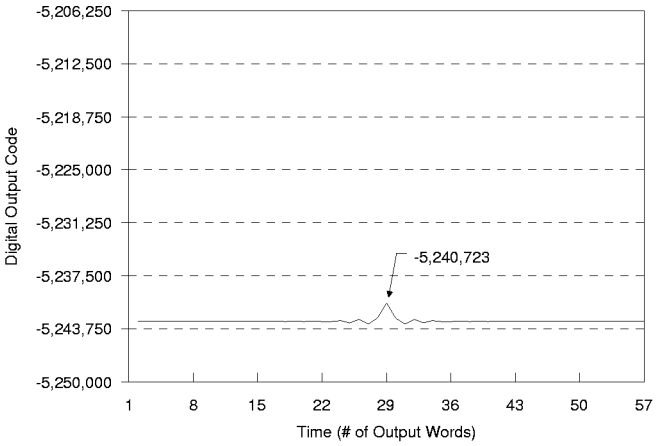



**Figure 9. CS5322 Impulse Response, $f_0$ = 62.5 Hz**

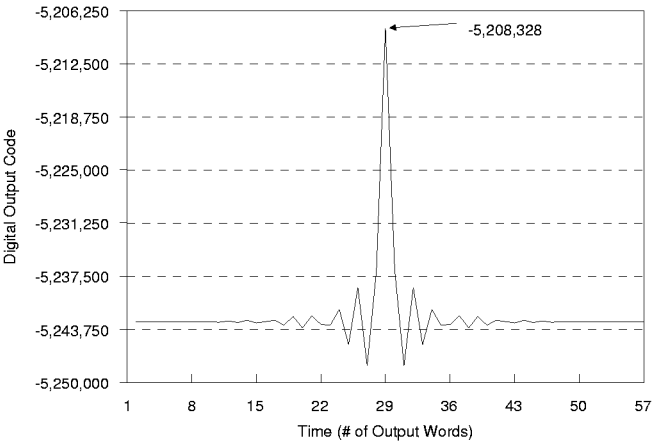



**Figure 10. CS5322 Impulse Response, $f_0$ = 1000 Hz**

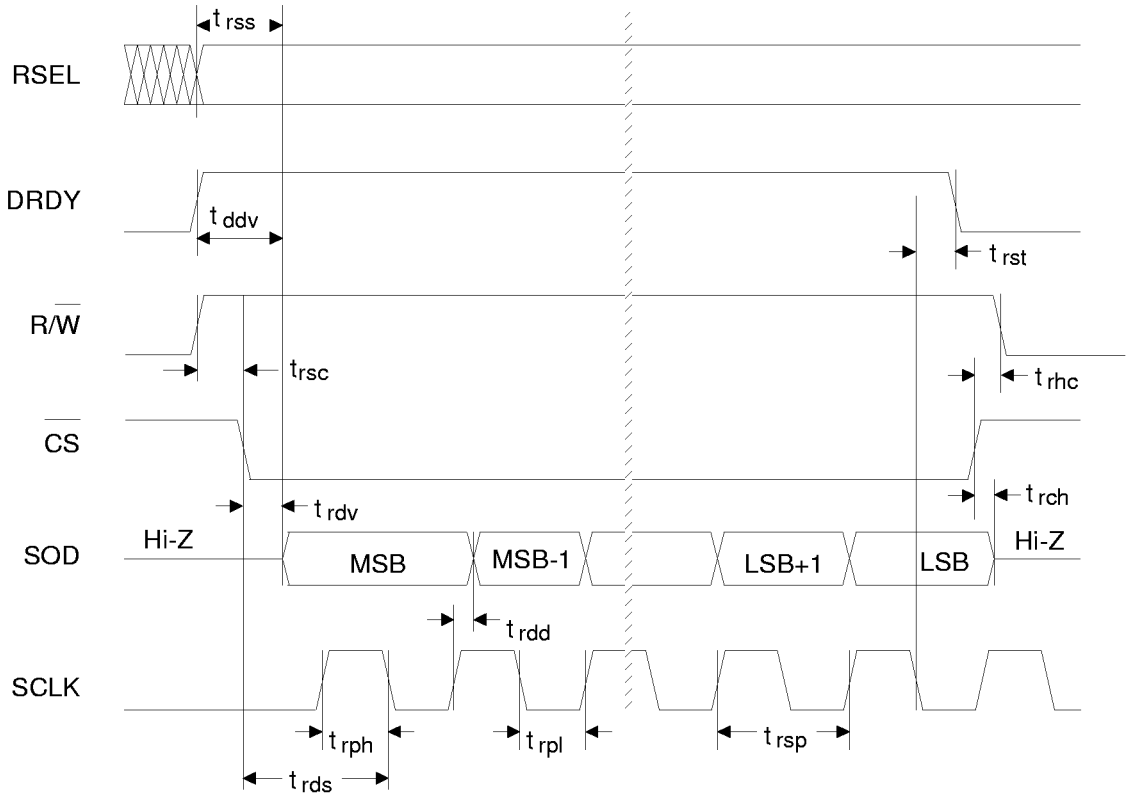
## POWER SUPPLY ($T_A$ = 25°C; VD+ = 5V; CLKIN = 1.024 MHz)

| Parameter* | | CS5322-K | | | CS5322-B | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Specified Temperature Range | | 0 | - | +70 | -40 | - | +85 | °C |
| Power Supply Current: | ID+ (Note 10) | - | 2.2 | 4 | - | 2.2 | 4 | mA |
| Power Dissipation: | (Note 10) | | | | | | | |
| | PWDN Low | - | 11 | 20 | - | 11 | 20 | mW |
| | PWDN High | - | 0.6 | 2.5 | - | 0.6 | 2.5 | mW |

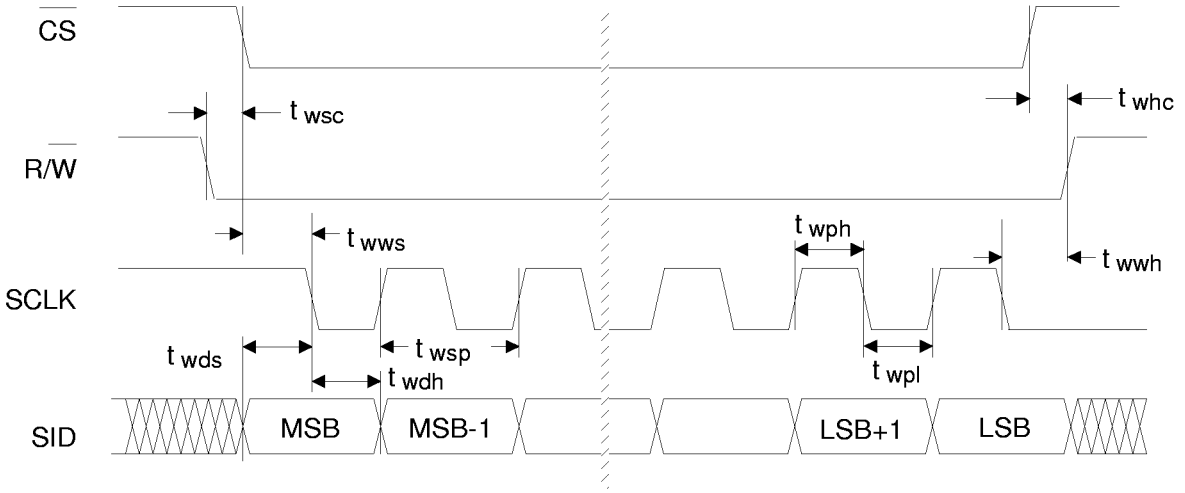
## SWITCHING CHARACTERISTICS ($T_A$ = $T_{min}$ to $T_{max}$; VD+ = 5V±5%; DGND = 0V; Inputs: Logic 0 = 0V Logic 1 = VD+; $C_L$ = 50 pF (Note 14))

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| CLKIN Frequency | | $f_c$ | 0.512 | 1.024 | 1.1 | MHz |
| CLKIN Duty Cycle | | | 40 | - | 60 | % |
| Rise Times: | Any Digital Input | $t_{rise}$ | - | - | 100 | ns |
| | Any Digital Output | | - | 50 | 100 | ns |
| Fall Times: | Any Digital Input | $t_{fall}$ | - | - | 100 | ns |
| | Any Digital Output | | - | 50 | 100 | ns |
| ***Serial Port Read Timing*** | | | | | | |
| DRDY to Data Valid | | $t_{ddv}$ | - | - | 25 | ns |
| RSEL Setup Time before Data Valid | | $t_{rss}$ | 50 | - | - | ns |
| Read Setup Before CS Active | | $t_{rsc}$ | 20 | - | - | ns |
| Read Active to Data Valid | | $t_{rdv}$ | - | - | 50 | ns |
| SCLK rising to New SOD bit | | $t_{rdd}$ | - | - | 50 | ns |
| SCLK Pulse Width High | | $t_{rph}$ | 30 | - | - | ns |
| SCLK Pulse Width Low | | $t_{rpl}$ | 30 | - | - | ns |
| SCLK Period | | $t_{rsp}$ | 100 | - | - | ns |
| SCLK falling to DRDY falling | | $t_{rst}$ | - | - | 50 | ns |
| CS High to Output Hi-Z | | $t_{rch}$ | - | - | 20 | ns |
| Read Hold Time after CS Inactive | | $t_{rhc}$ | 20 | - | - | ns |
| Read Select Setup to SCLK falling | | $t_{rds}$ | 20 | - | - | ns |
| ***Serial Port Write Timing*** | | | | | | |
| Write Setup Before CS Active | | $t_{wsc}$ | 20 | - | - | ns |
| SCLK Pulse Width Low | | $t_{wpl}$ | 30 | - | - | ns |
| SCLK Pulse Width High | | $t_{wph}$ | 30 | - | - | ns |
| SCLK Period | | $t_{wsp}$ | 100 | - | - | ns |
| Write Setup Time to First SCLK falling | | $t_{wws}$ | 20 | - | - | ns |
| Data Setup Time to First SCLK falling | | $t_{wds}$ | 20 | - | - | ns |
| Write Select Hold Time after SCLK falling | | $t_{wwh}$ | 20 | - | - | ns |
| Write Hold Time after CS Inactive | | $t_{whc}$ | 20 | - | - | ns |
| DATA Hold Time after SCLK falling | | $t_{wdh}$ | 20 | - | - | ns |

Note: 14. Guaranteed by design, characterization and/or test.




SERIAL PORT READ TIMING (R/$\overline{W}$ = 1, CS = 0, RSEL = 1
* DRDY Does not toggle if reading status, RSEL = 0)

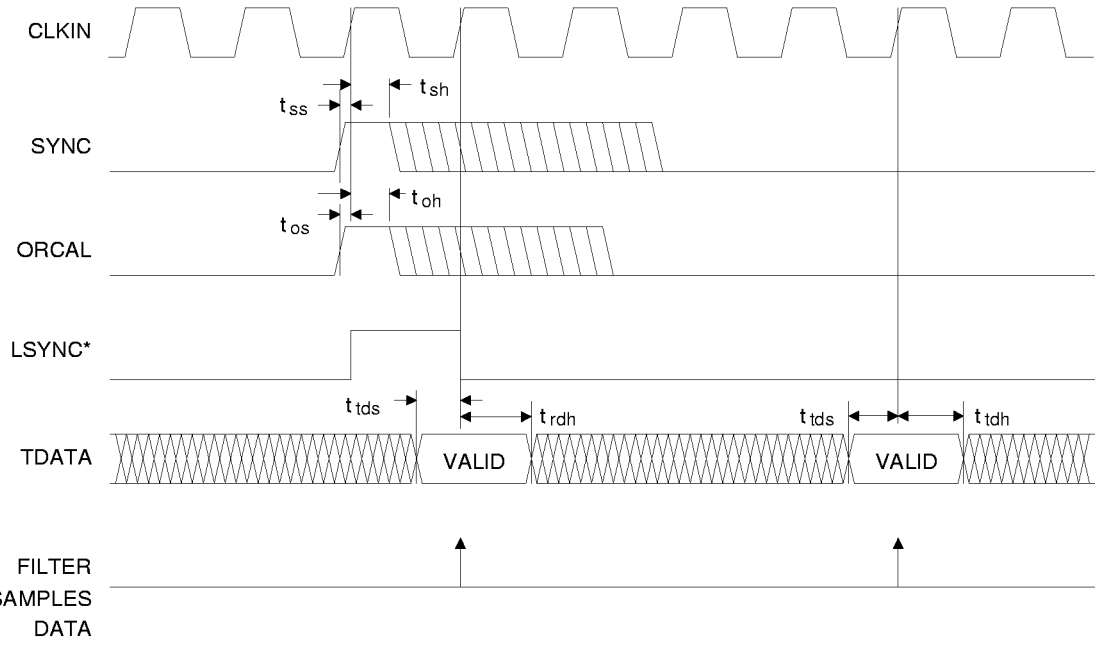



SERIAL PORT WRITE TIMING

**Figure 11. CS5322 Serial Port**

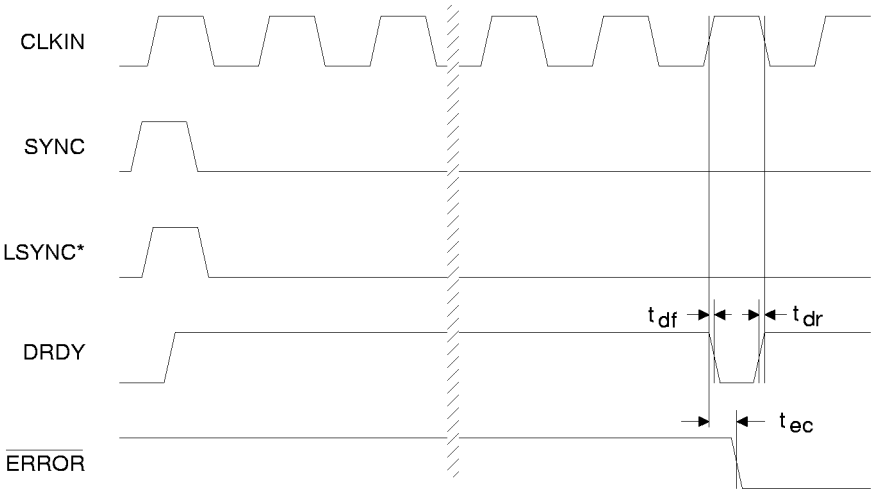
## SWITCHING CHARACTERISTICS (continued)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ***Test Data (TDATA) Timing*** | | | | | |
| SYNC Setup Time to CLKIN rising | $t_{ss}$ | 20 | - | - | ns |
| SYNC Hold Time after CLKIN rising | $t_{sh}$ | 20 | - | - | ns |
| TDATA Setup Time to CLKIN rising after SYNC | $t_{tds}$ | - | 20 | - | ns |
| TDATA Hold Time after CLKIN rising | $t_{tdh}$ | - | 150 | - | ns |
| ORCAL Setup Time to CLKIN rising | $t_{os}$ | 20 | - | - | ns |
| ORCAL Hold Time after CLKIN rising | $t_{oh}$ | 20 | - | - | ns |
| ***DRDY Timing*** | | | | | |
| CLKIN rising to DRDY falling | $t_{df}$ | - | 140 | - | ns |
| CLKIN falling to DRDY rising | $t_{dr}$ | - | 150 | - | ns |
| CLKIN rising to ERROR change | $t_{ec}$ | - | 140 | - | ns |
| ***RESET Timing*** | | | | | |
| RESET Setup Time to CLKIN rising | $t_{rs}$ | 20 | - | - | ns |
| RESET Hold Time after CLKIN rising | $t_{rh}$ | 20 | - | - | ns |
| SYNC Setup Time to CLKIN rising | $t_{ss}$ | 20 | - | - | ns |
| SYNC Hold Time after CLKIN rising | $t_{sh}$ | 20 | - | - | ns |




* Note: Internal timing signal generated in the CS5322

**Figure 12. TDATA Setup/Hold Timing**




*Note: For overwrite case, DRDY will remain high.

**Figure 13. DRDY Timing**

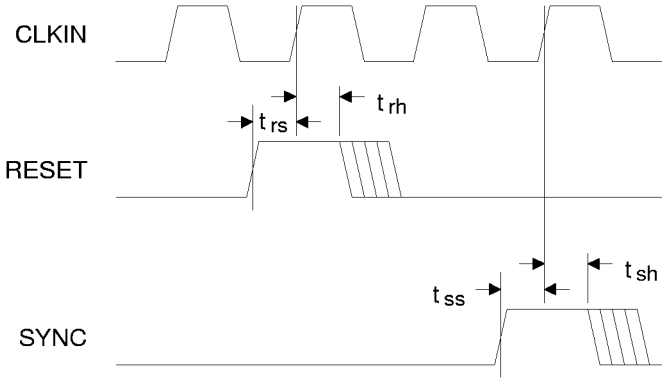
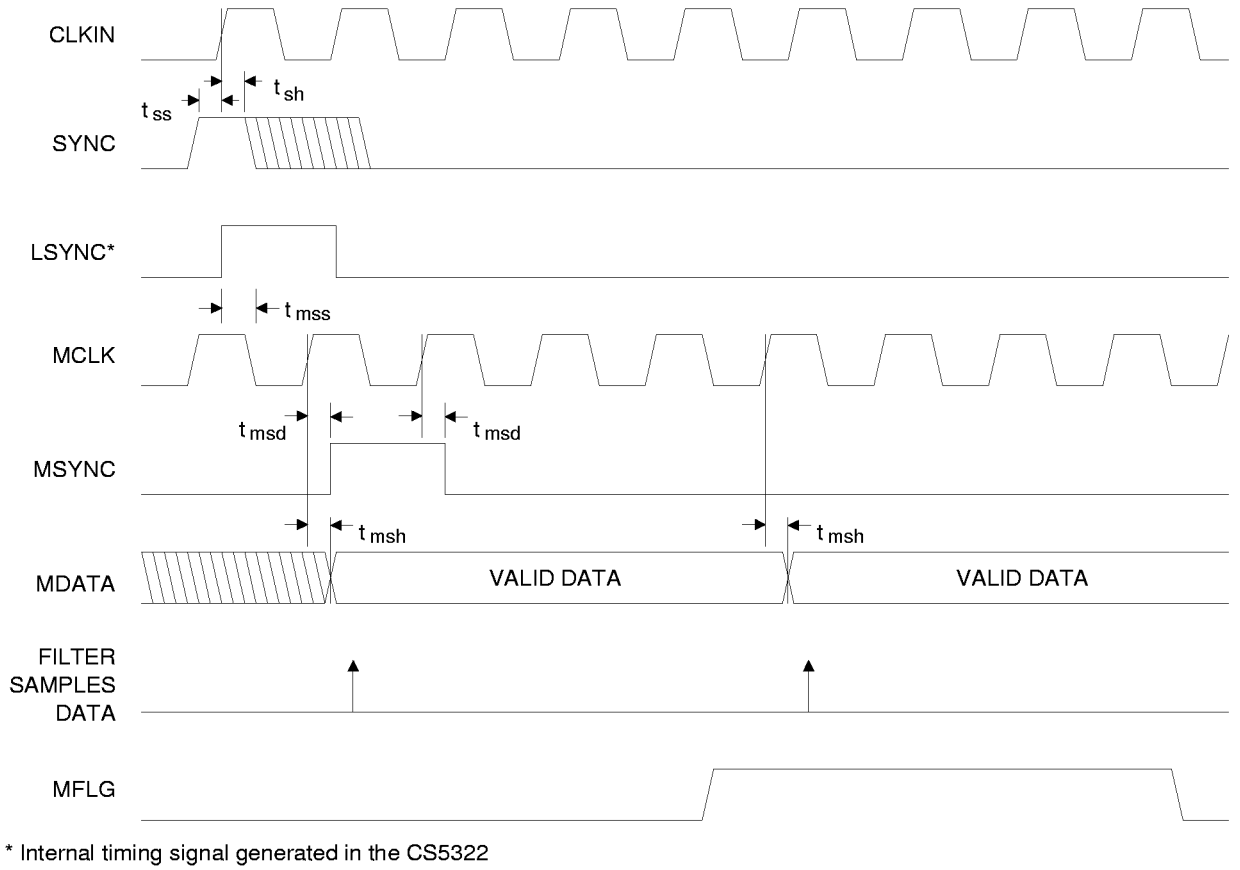



**Figure 14. RESET Timing**

## SWITCHING CHARACTERISTICS (continued)

| Parameter | | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| MCLK Frequency | | (Note 15) | $f_c$ | 0.512 | 1.024 | 1.1 | MHz |
| MCLK Duty Cycle | | | | 40 | - | 60 | % |
| Rise Times: | Any Digital Input | (Note 16) | $t_{rise}$ | - | - | 100 | ns |
| | Any Digital Output | | | - | 50 | 200 | ns |
| Fall Times: | Any Digital Input | (Note 16) | $t_{fall}$ | - | - | 100 | ns |
| | Any Digital Output | | | - | 50 | 200 | ns |
| SYNC Setup Time to CLKIN rising | | | $t_{ss}$ | 20 | - | - | ns |
| SYNC Hold Time after CLKIN rising | | | $t_{sh}$ | 20 | - | - | ns |
| CLKIN edge to MCLK edge | | | $t_{mss}$ | - | 30 | - | ns |
| MCLK rising to Valid MDATA | | | $t_{msh}$ | - | 50 | - | ns |
| MSYNC Delay from MCLK rising | | (Note 17) | $t_{msd}$ | - | 90 | - | ns |

Notes: 15. If MCLK is removed, the device will enter the power down mode.
16. Excludes MCLK input. MCLK should be driven with a signal having rise and fall times of 25 ns or faster.
17. Only the rising edge of MSYNC relative to MCLK is used to synchronize the device. MSYNC can return low at any time as long as it remains high for at least one MCLK cycle.




* Internal timing signal generated in the CS5322

**Figure 15. CS5322/CS5323 Interface Timing**

## DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to $T_{max}$; VD+ = 5.0V±5%; GND = 0V; measurements performed under static conditions)

| Parameter | | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| High-Level Input Drive Voltage | | | $V_{IH}$ | (VD+)-0.3 | - | - | V |
| Low-Level Input Drive Voltage | | | $V_{IL}$ | - | - | 0.3 | V |
| High-Level Input Threshold | | (Note 18) | | (VD+)-1.0 | - | - | V |
| Low-Level Input Threshold | | (Note 18) | | - | - | 1.0 | V |
| High-Level Output Voltage | $I_{OUT}$ = -40µA | (Note 19) | $V_{OH}$ | (VD+)-0.6 | - | - | V |
| Low-Level Output Voltage | | (Note 19) | $V_{OL}$ | | | | |
| | $I_{OUT}$ = +1.6mA | CS5322 | | - | - | 0.4 | V |
| | $I_{OUT}$ = +40µA | CS5323 | | - | - | 0.4 | V |
| Input Leakage Current | All pins except MFLG, SOD | | $I_{LKG}$ | - | - | ±10 | µA |
| Three-State Leakage Current | | | $I_{OZ}$ | - | - | ±10 | µA |
| Digital Input Capacitance | | | $C_{IN}$ | - | 9 | - | pF |
| Digital Output Capacitance | | | $C_{OUT}$ | - | 9 | - | pF |

Notes: 18. Device is intended to be driven with CMOS logic levels.
19. Device is intended to be interfaced to CMOS logic. Resistive loads are not recommended on these pins.

## RECOMMENDED OPERATING CONDITIONS (Voltages with respect to GND = 0V)

| Parameter | | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| DC Supply: | | (Note 20) | | | | | |
| | Positive Analog | | VA+ | 4.75 | 5.0 | 5.25 | V |
| | Negative Analog | | VA- | -4.75 | -5.0 | -5.25 | V |
| | Positive Digital | | VD+ | 4.75 | 5.0 | 5.25 | V |
| | Negative Digital | | VD- | -4.75 | -5.0 | -5.25 | V |
| Ambient Operating Temperature | | -KL | $T_A$ | 0 | - | +70 | °C |
| | | -BL | $T_A$ | -40 | - | +85 | °C |

Notes: 20. The maximum voltage differential between the Positive Supply of the CS5323 and the Positive Digital Supply of the CS5322 must be less than 0.25V.

## ABSOLUTE MAXIMUM RATINGS* (Voltages with respect to GND = 0V)

| Parameter | | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| DC Supply: | | (Note 20) | | | | | |
| | Positive Analog | | VA+ | -0.3 | - | 6.0 | V |
| | Negative Analog | | VA- | 0.3 | - | -6.0 | V |
| | Positive Digital | | VD+ | -0.3 | - | (VA+)+0.3 | V |
| | Negative Digital | | VD- | 0.3 | - | -6.0 | V |
| Input Current, Any Pin Except Supplies | | (Note 21) | $I_{in}$ | - | - | ±10 | mA |
| Digital Input Voltage | CS5322 | | $V_{IND}$ | -0.3 | - | (VD+)+0.3 | V |
| | CS5323 | | $V_{IND}$ | -0.3 | - | (VA+)+0.3 | V |
| Storage Temperature | | | $T_{stg}$ | -65 | - | 150 | °C |

Notes: 21. Transient currents of up to 100 mA will not cause SCR latch up.

*WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

## GENERAL DESCRIPTION

The CS5322 is a monolithic digital Finite Impulse Response (FIR) filter with programmable decimation. The CS5323 is a monolithic CMOS A/D converter designed specifically for very high resolution measurement of signals between dc and 1500 Hz. The CS5322 and CS5323 are intended to be used together to form a unique high resolution A/D system.

The CS5323 utilizes a fourth order oversampling architecture to achieve high resolution A/D conversion. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The first stage of the fourth order modulator uses discrete components external to the chip to maximize signal to noise. The modulator provides an oversample d serial bit stream at 256 Kbits per second (CLKIN = 1.024MHz) to the CS5322 FIR decimation filter.

The CS5322 provides the digital anti-alias filter for the CS5323 modulator output. The CS5322 consists of: A multi-stage FIR filter, four registers (status, data, offset, and configuration), a flexible serial input and output port, and a 2-channel input data multiplexer that selects data from the CS5323 (MDATA) or user test data (TDATA). The CS5322 decimates (64X to 4096X) the output to any of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format. Figure 16 illustrates the CS5322 Block Diagram.

### CS5323 Signal Input and Current Reference

The CS5323 uses a number of external discrete components to achieve maximum rated performance. Figure 17 illustrates the recommended circuit configuration for the current reference and signal input components.

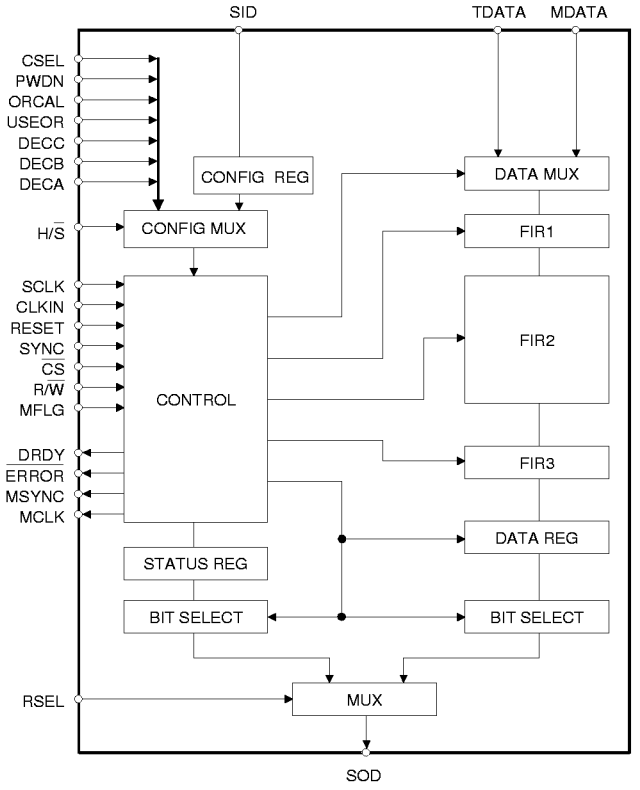



**Figure 16. CS5322 Block Diagram**

The CS5323 is designed to use a current reference of 1 mA into the IREF pin. A current reference rather than a voltage reference was chosen to achieve better noise performance. For optimum performance the dc source impedance at the IREF pin should be approximately 10 kΩ. This calls for a 10 volt reference source driving the 10 k 128MW ($R_6$ + $R_7$) resistor to achieve the desired 1 mA current source. The IREF input sets the full scale gain of the A/D converter.

A current source 1/4 the size of the IREF input current must be sourced into the integrator summing junction at the SUM pin. This requires a 40 kΩ resistance ($R_4$ + $R_5$) be placed from the 10 volt reference to the SUM pin.

The 1 mA IREF current and the 250 µA sources have capacitive filtering to aid in reducing the broadband current noise from the voltage reference. These capacitors should be of quality construction. Particular attention should be paid to leakage current variation over the desired operating temperature, as this leakage will affect t he system gain.

The signal input pin (SUM) of the CS5323 is the summing junction of the input integrator stage. This integrator is designed to use an external input resistor ($R_1$) and integrating capacitor ($C_1$). In addition, a capacitor ($C_2$) is required at this node for proper compensation of the integrator. The size of the input resistor ( $R_1$) is determined

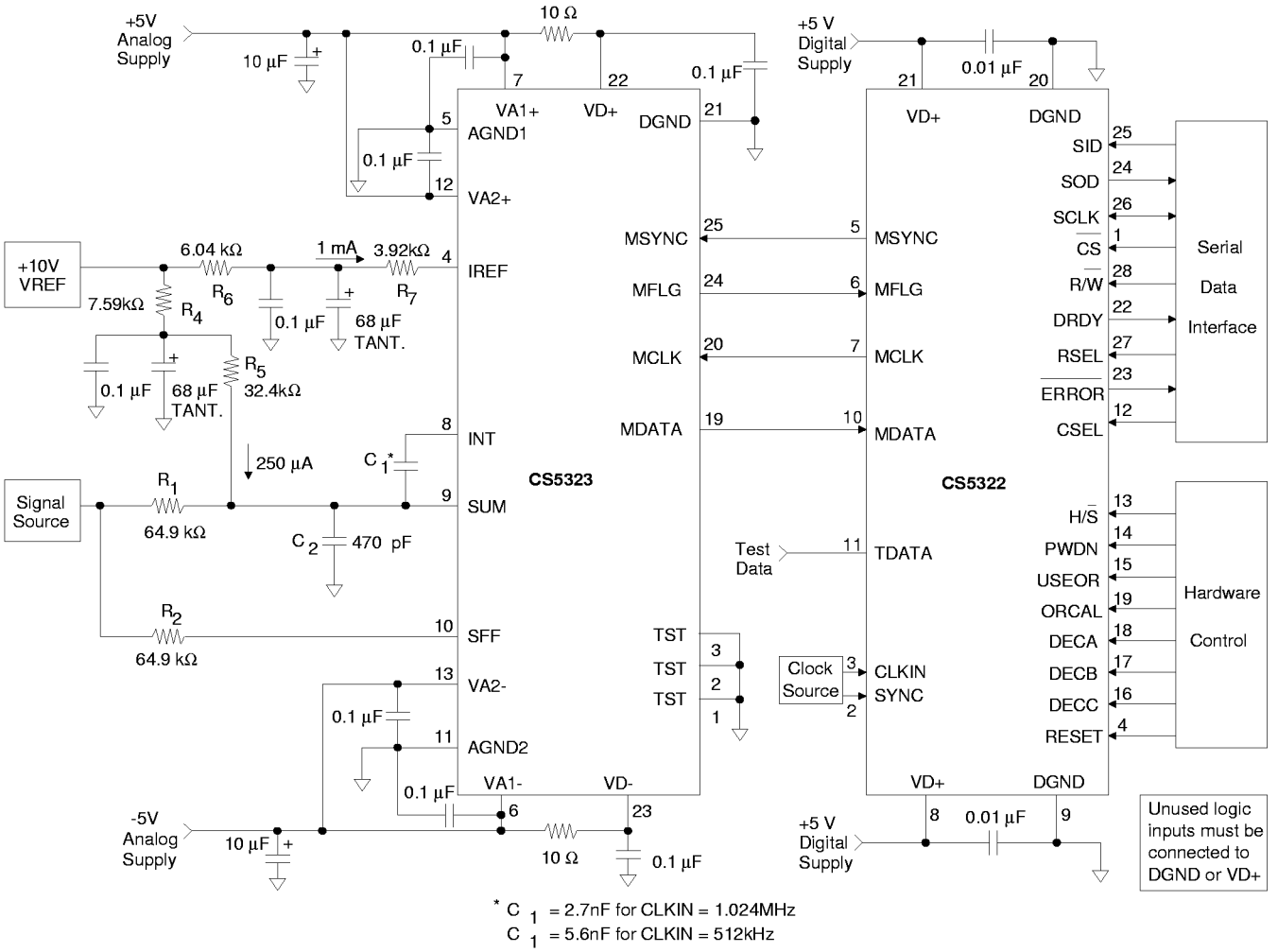



**Figure 17. System Connection Diagram**

by the magnitude of the signal current. With a maximum input voltage onto the resistor, the integrator input current must be set equal to approximately 0.15 the current value injected into the IREF pin. With a 1 mA IREF current, the full scale signal current should be about 150 µA. Additionally, to minimize current noise into the summing junction, the value of the effective input resistor should be above 8 kΩ. Using the 64.9 kΩ resistor for $R_1$ sets the full scale input voltage onto the integrating resistor to a value near 10 volts. The input signal then spans $20V_{p-p}$.

The integrator resistor and capacitor combination should yield a frequency ($f=1/(2\pi R_1C_1)$) between 850 and 950 Hz to achieve maximum performance. This results in a capacitor value of 2.7 nF. The capacitor should be chosen to minimize leakage, dielectric absorption, and the voltage coefficient of capacitance. High quali ty film capacitors may be acceptable in many applications.

The signal into the SFF pin (Signal Feedforward) of the CS5323 bypasses the input stage of the input integrator and improves distortion performance in the passband. The resistor ($R_2$) used at this input should be identical in value and performance characteristics to that of the resistor on the input of the SUM pin ($R_1$).

Although the CS5323 (Figure 17) input is designed to accept 20 Vp-p, modulator loop stability can be adversely affected by high frequency out-of-band signals. Therefore, input signals above 8kHz should be at least 6dB below full scale to prevent oscillation in the modulator loop and to ensure proper conversion data.

## RESET Operation

The RESET pin puts the CS5322 into a known initialized state. RESET is recognized on the next CLKIN rising edge after the RESET pin has been brought high (RESET=1). All internal logic is initialized when RESET is active.

Normal device operation begins on the second CLKIN rising edge after RESET is brought low. The CS5322 will remain in an idle state, not performing convolutions, until triggered by a SYNC event.

A RESET operation clears memory, sets the data output register, offset register, and status flags to all zeroes, and sets the configuration register to the the state of the corresponding hardware pins (PWDN, ORCAL, DECC, DECB, DECA, USEOR, and CSEL). The reset state is entered on power on, independent of the RESET pin. If RESET is low, the first CLKIN will exit the power on reset state.

## Power-down Operation

The PWDN pin puts the CS5322 into the power-down state. The power-down state is entered on the first CLKIN rising edge after the PWDN pin is brought high. While in the power-down state, the MCLK and MSYNC signals to the CS5323 analog modulator are held low. The loss of the MCLK signal to the modulator causes it to power-down. The signals on the MDATA and MFLG pins are ignored. The serial interface of the CS5322 remains active allowing read and write operations. Information in the data register, offset register, configuration register, and convolution data memory are maintained during power-down. The internal controller requires 64 clock cycles after PWDN is asserted before CLKIN stops.

The CS5322 exits the power-down state on the first CLKIN rising edge after the PWDN pin is brought low. The CS5322 then enters an idle state until triggered by a SYNC event.

To avoid possible high current states while in the power down state, the following conditions apply:

1. CLKIN must be active for at least 64 clock cycles after PWDN entry.
2. CSEL and TDATA must not both be asserted high.

## SYNC Operation

The SYNC pin is used to start convolutions and synchronize the CS5322 and CS5323 to an external sampling source or timing reference. The SYNC event is recognized on the first CLKIN rising edge after the SYNC pin goes high. SYNC may remain high indefinitely. Only the sequence of SYNC rising followed by CLKIN rising generates a SYNC event.

The SYNC event aligns the output sample and causes the filter to begin convolutions. The first SYNC event causes an immediate DRDY provided DRDY is low. Subsequent data ready events will occur at a rate determined by the decimation rate inputs DECC, DECB, and DECA. Multiple SYNC events can be applied with no effect on operation if they are perfectly timed according to the decimation rate. Any SYNC event not in step with the decimation rate will cause a re-alignment and loss of data.

## Serial Read Operation

Serial read is used to obtain status or conversion data. The $\overline{CS}$, R/$\overline{W}$, SCLK, RSEL, and SOD pins control the read operation. The serial read operation is activated when $\overline{CS}$ goes low ($\overline{CS}$=0) with the R/$\overline{W}$ pin high (R/$\overline{W}$=1). The RSEL pin selects between conversion data (data register) or status information (sta tus register). The selected serial bit stream is output on the SOD (Serial Output Data) pin.

On read select, SCLK can either be high or low, the first bit appears on the SOD pin and should be latched on the falling edge of SCLK. After the first SCLK falling edge, each SCLK rising edge shifts out a new bit. Status reads are 16 bits, and data reads are 24 bits. Both streams are supplied as MSB first, LSB last.

In the event more SCLK pulses are supplied than necessary to clock out the requested information, trailing zeroes will be output for data reads and trailing LSB's for status reads. If the read operation is terminated before all the bits are read, the internal bit pointer is reset to the MSB so that a re-read will give the same data as the first r ead, with one exception. The status error flags are cleared on read and will not be available on a re-read.

The status error flags must be read before entering the powerdown state. If an error has occurred before entering powerdown and the status bit (ERROR) has not been read, the status bits (ERROR, OVERWRITE, MFLG, ACC1 and ACC2) may not be cleared on status reads. Upon exiting the powerdown state and entering normal operation, the user may be flagged that an error is still present.

The SOD pin floats when read operation is deactivated (R/$\overline{W}$=1, $\overline{CS}$=1). This enables the SID and SOD pins to be tied together to form a bi-directional serial data bus. There is an internal nominal 100kΩ pull-up resistor on the SOD pin.

## Serial Write Operation

Serial write is used to write data to the configuration register. The $\overline{CS}$, R/$\overline{W}$, SCLK and SID pins control the serial write operation. The serial write operation is activated when $\overline{CS}$ goes low ($\overline{CS}$=0) with R/$\overline{W}$ pin low (R/$\overline{W}$=0).

Serial input data on the SID pin is sampled on the falling edge of SCLK. The input bits are stored in a temporary buffer until either the write operation is terminated or 8 bits have been received. The data is then parallel loaded into the configuration register. If fewer than 8 bits are input before the write termination, the other bits may be i ndeterminate.

Note that a write will occur when $\overline{CS}$ = 0 and R/$\overline{W}$ = 0 even if SCLK is not toggled. Failure to clock in data with the appropriate number of SCLKs can leave the configuration register in an indeterminate condition.

The serial bit stream is received MSB first, LSB last. The order of the input control data is PWDN first, followed by ORCAL, USEOR, CSEL, Reserved, DECC, DECB, and DECA The configuration data bits are defined in Table1. The configuration data controls device operation when only in the software mode, i.e., the H/$\overline{S}$ pin is low (H/$\overline{S}$=0 ). The Reserved configuration data bit must always be written low.

## Offset Calibration Operation

The offset calibration routine computes the offset produced by the CS5323 modulator and stores this value in the offset register. The USEOR pin or bit determines if the offset register data is to be used to correct output words.

After power is applied to the chip set the CS5322 must be RESET. To begin an offset calibration, the CS5323 analog input must represent the offset value. Then in software mode (H/$\overline{S}$ = 0) the ORCAL bit must be toggled from a low to a high. In hardware mode the ORCAL pin must be toggled low for at least one CLKIN cycle, then taken high (except when ORCAL = 1 and the CS5322 is RESET as this toggles the ORCAL internally). After ORCAL has been toggled, the SYNC signal must be applied to the CS5322. The filter settles on the input value in 56 output words. The output word rate is determined by the state of the the decimation rate control pins, DECC, DECB, and DECA. On the 57th output wo rd, the CS5322 issues the ORCALD status flag, outputs the offset data sample, and internally loads the offset register. During calibration, the offset register value is not used.

If USEOR is high (USEOR=1), subsequent samples will have the offset subtracted from the output. The state of USEOR must remain high

| Input Bit # | Equivalent Hardware Function | Description |
|---|---|---|
| 1 (MSB) | PWDN | Standby mode |
| 2 | ORCAL | Self-offset calibration |
| 3 | USEOR | Use Offset Register |
| 4 | CSEL | Channel Select |
| 5 | Reserved | Factory use only |
| 6 | DECC | Filter BW selection |
| 7 | DECB | Filter BW selection |
| 8 (LSB) | DECA | Filter BW selection |

**Table 1. Configuration Data Bits**

| Output Bit # | Function | Description |
|---|---|---|
| 1 (MSB) | ERROR | Detects one of the errors below |
| 2 | OVERWRITE Error | Overwrite Error |
| 3 | MFLG Error | Modulator Flag Error |
| 4 | ACC1 Error | Accumulator 1 Error |
| 5 | ACC2 Error | Accumulator 2 Error |
| 6 | DRDY | Data Ready |
| 7 | 1SYNC | First sample after SYNC |
| 8 | ORCALD | Offset calibration done |
| 9 | PWDN | Standby mode |
| 10 | ORCAL | Self-offset calibration |
| 11 | USEOR | Use Offset Register |
| 12 | CSEL | Channel Select |
| 13 | Reserved | Factory use only |
| 14 | DECC | Bandwidth Selection Status |
| 15 | DECB | Bandwidth Selection Status |
| 16 | DECA | Bandwidth Selection Status |

**Table 2. Status Data (from the SOD Pin)**

for the complete duration of the convolution cycle. If USEOR is low (USEOR=0), the output word is not corrected, but the offset register retains its value for later use. The results of the last calibration will be he ld in the offset register until the end of a new calibration, or until the CS5322 is reset using the RESET pin. USEOR does not alter the offset register value, only its usage.

To restart a calibration, ORCAL and SYNC must be taken low for at least one CLKIN cycle. ORCAL must then be taken high. The calibration will restart on the next SYNC event. If the ORCAL pin remains in a high state, only a single calibration will start on the first SYNC signal.

## Status Bits

The Status Register is a 16- bit register which allows the user to read the flags and configuration settings of the CS5322. Table 2 documents the data bits of the Status Register.

The ERROR flag, $\overline{\text{ERROR}}$, is the OR'ed result of OVERWRITE, MFLG, ACC1, and ACC2. The ERROR bit is active high whenever any of the four error bits are set due to a fault condition. The $\overline{\text{ERROR}}$ output has a nominal 100KΩ internal pull-up resistor.

The OVERWRITE bit is set when new conversion data is ready to be loaded into the data register, but the previous data was not completely read out. This can occur on either of two conditions: a read operation is in progress or a read operation was started, then aborted, and not completed. These two conditions are data read attempts. The attempt is identified by the first SCLK low edge (MSB read) of a data register read. If a data register read is not attempted, the CS5322 assumes that data is not wanted and does not assert OVERWRITE, and the old data is over-written by the new data. On an OVERWRITE condition, the old partially read data is preserved, and the new data word is lost.

Status reads have no effect on OVERWRITE assert operations. The OVERWRITE bit is cleared on a status register read or RESET.

The MFLG error bit reflects the CS5323 MFLG signal. Any high level on the CS5322 MFLG pin will set the MFLG status bit. The bit is cleared on a status register read or RESET operation, only if the MFLG pin on the CS5322 has returned low. A internal nominal 100KΩ pulldown resistor is on the MFLG pin.

The accumulator error bits, ACC1 and ACC2, indicate that an underflow or overflow has occurred in the FIR1 filter for ACC1, or the FIR2 and FIR3 filters for ACC2.Both errors are cleared on a status read, provided the error conditions are no longer present. In normal operation the ACC1 error will only occur when the input data stream to FIR1 is all 1's for more than 32 bits. The ACC2 error cannot occur in normal operation.

The DRDY bit reflects the state of the DRDY pin. DRDY rising edge indicates that a new data word has been loaded into the data register and is available for reading. DRDY will fall after the SCLK falling edge that reads the data register LSB. If no data read attempt is made, DRDY will pulse low for 1/2 CLKIN cycle, providing a positive edge on the new data availability. In the OVERWRITE case, DRDY remains high because new data is not loaded at the normal end of conversion time.

The 1SYNC status bit provides an indication of the filter group delay. It goes high on the second output sample after SYNC and is valid for only that sample. For repetitive SYNC operations, SYNC must run at one fourth the output word rate or slower to avoid interfering with the 1SYNC operation. With these slower repetitive SYNC's or non-periodi c SYNC's separated by at least three output words, 1SYNC will occur on the second output sample after SYNC.

ORCALD indicates that calibration of the offset register is complete and the offset sample is available in the output register. This flag is high only during that sample and is otherwise low.

The remaining eight status bits (PWDN, ORCAL, USEOR, CSEL, Reserved, DECC, DECB, AND DECA) provide configuration readback for the user. These bits echo the control source for the CS5322 such that in the hardware mode ($H/\overline{S}$=1), they follow the corresponding input pins. In host mode ($H/\overline{S}$=0) they follow the corresponding config uration bits.

A brief explanation of the eight bits are as follows:

PWDN - When high, indicates that the CS5322 is in the power-down state.

ORCAL - When high, indicates a potential calibration start.

USEOR - When high, indicates the Offset Register is used. During calibration, this bit will read zero indicating the offset register is not being used during calibration.

CSEL- When high, TDATA is selected as the filter source. When low, the MDATA output signal from the CS5323 is selected as the input source to the filter.

Reserved - Always read slow.

| DECC | DECB | DECA | Output Word Rate (Hz) | Clocks Filter Output |
|---|---|---|---|---|
| 0 | 0 | 0 | 62.5 | 16384 |
| 0 | 0 | 1 | 125 | 8192 |
| 0 | 1 | 0 | 250 | 4096 |
| 0 | 1 | 1 | 500 | 2048 |
| 1 | 0 | 0 | 1000 | 1024 |
| 1 | 0 | 1 | 2000 | 512 |
| 1 | 1 | 0 | 4000 | 256 |
| 1 | 1 | 1 | Reserved | - |

**Table 3. Bandwidth Selection: Truth Table**

DECC, DECB,and DECA - Indicate the decimation rate of the filter and are defined in Table 3.

## Digital Output and Data Format

For proper operation the CS5322 must be provided with a CMOS-compatible clock into the CLKIN pin. The normal operating frequency is 1.024 MHz. This clock determines the input sample rate. The sample rate is CLKIN/4 while the output word rate is determined by the status of the DECC, DECB, and DECA input pins or configuration bits; depending whether in the hardware mode or host mode.

The CS5322 computes a serial 24-bit output word in two's complement format. The output codes range from decimal -5242880 to +5242879 for a ±10V sine wave input into the CS5323 modulator as shown in Table 4.

| Modulator Input Signal | Digital Filter Output Code | |
|---|---|---|
| | HEX | Decimal |
| approx. +16V† | 7FEFFF | +8384511 |
| approx. +11V | 57FFFF | +5767167 |
| approx. +10V | 4FFFFF | +5242879 |
| 0V | 000000 | 0 |
| approx. -10V | B00000 | -5242880 |
| approx. -11V | A00000 | -5767168 |
| approx. -16V† | 800000 | -8388608 |

† This is an overrange condition

**Table 4. Output Coding for the CS5322 and CS5323 combination**

## Performance

The CS5322/23 A/D converter is intended for use in seismic and passive sonar applications. These applications require particularly high dynamic range capability. The CS5322/23 offers high dynamic range without compromising spectral purity. The CS5322/23 typically achieves 120 dB of dynamic range, while maintaining signal/distortion at 110 dB.

An A/D converter system using the CS5322/23 A/D converter as its core was tested using Fast Fourier Transform techniques. Data was collected from the CS5322/23 serially via a UART interface to a PC-compatible computer. The output from the CS5322 was submitted to a windowing algorithm and then to the FFT algorithm. Figure 18 illustrates the performance of the CS5322/23 when tested with a full scale 100Hz signal for the 2ms filter selection. The CS5322/23 exhibits some second harmonic but no third harmonic. The test frequency of 100Hz was selected, as this was the center frequency of a bandpass filter constructed to reject harmonics and line frequencies present at the output of the sig nal generator. Figure19 illustrates the performance of the CS5322/23 (100 Hz input signal) for the 1 ms filter selection. Note that the performance of the CS5322/23 will generally exceed the capability of most available sine wave

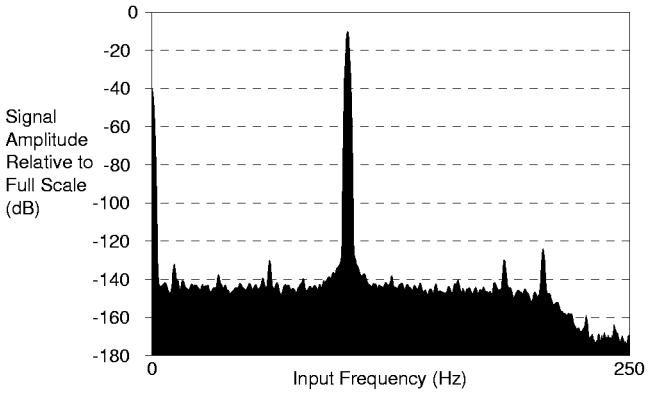



**Figure 18. 1024 Point FFT Plot with Full Scale Input, 100 Hz.**

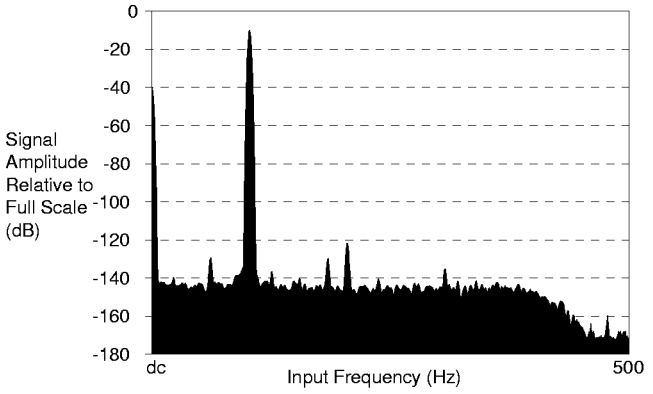



**Figure 19. 1024 Point FFT Plot with Full Scale Input, 100 Hz.**

test generators for frequencies between 2-500Hz. The excess noise is due to the signal source.

## Clock Source Considerations

To obtain maximum performance from the CS5322/CS5323 chip set requires a CLKIN signal with a very low level of clock jitter, i.e., less than 10 picoseconds of jitter. A well designed crystal-based clock is preferred. The clock oscillator should have a wellregulated supply, with local bypass capacitors at the oscillator. The output from the oscillator should pass through as few logic gates or counter-divider stages as possible. Excess clock jitter will reduce the signal/noise performance of the A/D converter.

## Power Supply Rejection Ratio

The power supply rejection ratio of the CS5323 is frequency dependent. The rejection for frequencies between dc and $f_1$ Hz (CLKIN=1.024 MHz) is nearly constant. Above $f_1$ Hz, the CS5322 digital filter will aid in rejecting interference until the frequencies near CLKIN/21.3 (above 48 kHz for CLKIN=1.024 MHz). Power supply interferen ce above this frequency may cause noise to be modulated into the passband (dc to $f_1$ Hz), degrading the performance of the A/D.

## Power Supply Considerations

The system connection diagram, Figure 17, illustrates the recommended power supply arrangements. The CS5323 has two positive analog supply pins and two negative analog supply pins. Multiple pins are used to minimize the possibility of noise coupling on the chip. All six power supply pins should be decoupled to their respective grounds, with a 0.1 µF capacitor located near the device. The digital supplies are decoupled from the analog supplies with a 10Ω resistors to minimize the effects of digital noise in the converter.

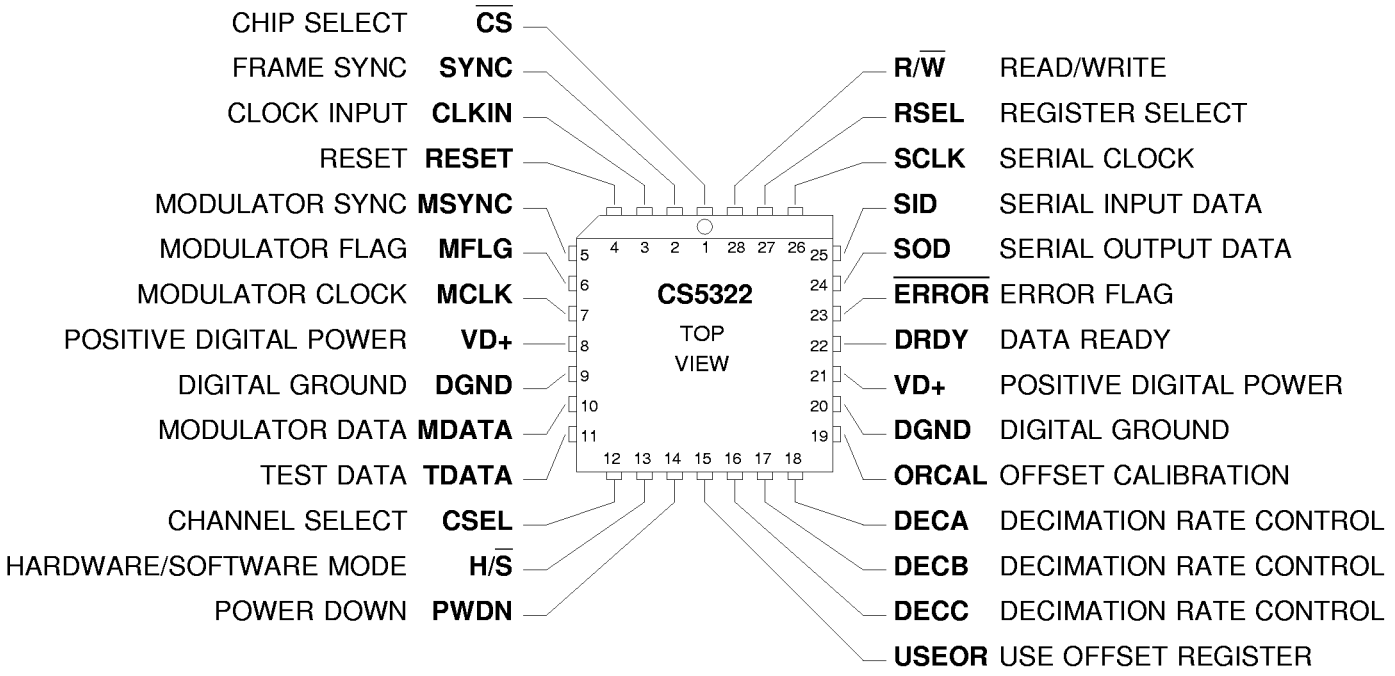
*The positive digital power supply of the CS5323 must never exceed either positive analog supply by more than a diode drop, or the CS5323 could experience permanent damage.* If separate supplies are used for the analog and digital sections of the chip, care must be taken that the analog supply comes up first at power-up. Additionally, the power supplies to the CS5323 should be active before the reference current generator supplies the IREF input current.

The maximum voltage differential between the positive digital supply of the CS5323 and the positive digital supply of the CS5322 must be less than 0.25V. Operation beyond this con-

straint may result in loss of analog performance in the CS5322 and CS5323 chip set.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filter.

To achieve maximum performance, the dc-dc converter operating frequency should be located below 48 kHz (see Power Supply Rejection). A synchronous dc-dc converter, whose operating frequency is derived from the1.024 MHz clock used to drive the CS5322, will minimize the potential for "beat frequencies" appearing in the dc to $f_1$ Hz passband.




## CS5322 PIN DESCRIPTIONS

### *Power Supplies*

**VD+ – Positive Digital Power, PIN 8,21**

Positive digital supply voltage. Nominally +5 volts.

**DGND – Digital Ground, PIN 9,20**

Digital ground reference.

### *Digital Outputs*

**MCLK – Modulator Clock Output, PIN 7**

A CMOS-compatible clock output (nominally 1.024 MHz) that provides the necessary clock for operation of the modulator.

**MSYNC – Modulator Sync, PIN 5**

The transition from a low to high level on this output will re-initialize the CS5323.

**$\overline{\text{ERROR}}$ - Error Flag, PIN 23**

This signal is the output of an open pull-up NOR gate with a nominal 100 kΩ pull-up resistor to which the error status data (OVERWRITE error, MFLG error, ACC1 error and ACC2 error) are inputs. When low, it notifies the host processor that an error condition exists. The $\overline{\text{ERROR}}$ signal can be wire OR'd together with other filters' outputs. The value of the internal pull-up resistor is 100 kΩ.

**DRDY - Data Ready, PIN 22**

When high, data is ready to be shifted out of the serial port data register.

**SOD - Serial Output Data, PIN 24**

The output coding is 2's complement with the data bits presented MSB first, LSB last. Data changes on the rising edge of SCLK. An internal nominal 100 kΩ pull-up resistor is included.

*Digital Inputs*

**MDATA – Modulator Data, PIN 10**

Data will be presented in a one-bit serial data stream at a bit rate of 256 KHz; (CLKIN = 1.024 MHz).

**TDATA - Test Data, PIN 11**

Input for user test data.

**MFLG – Modulator Flag, PIN 6**

A transition from a low to high level signals that the CS5323 modulator is unstable due to an over-range on the analog input. A Status Bit will be set in the digital filter indicating an error condition. An internal nominal 100 kΩ pull-down resistor included on the input pin.

**RESET - Filter Reset, PIN 4**

Performs a hard reset on the chip, all registers and accumulators are cleared. All signals to the device are locked out except CLKIN. The error flags in the Status Register are set to zero and the Data Register and Offset Register are set to zero. The configuration register is set to the values of the corresponding input pins. SYNC must be applied to resume convolutions after RESET deasserts.

**CLKIN - Clock Input, PIN 3**

A CMOS-Compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation the modulator and filter.

**SYNC - Frame Sync, PIN 2**

Conversion synchronization input. This signal synchronizes the start of the filter convolution. More than one SYNC signal can occur with no effect on filter performance, providing the SYNC signals are perfectly timed at intervals equal to the output sample period.

**CSEL - Channel Select, PIN 12**

When high, information on the TDATA pin is presented to the digital filter. A low causes data on the MDATA input to be presented to the digital filter.

**PWDN - Powerdown, PIN 14**

Powers down the filter when taken high. Convolution cycles in the digital filter and the MCLK signal are stopped. The registers maintain their data and the serial port remains active. SYNC must be applied to resume convolutions after PWDN deasserts.

**DECA - Decimation Rate Control , PIN 18**

See Table 3.

**DECB - Decimation Rate Control , PIN 17**

See Table 3.

**DECC - Decimation Rate Control, PIN 16**

See Table 3.

**H/$\overline{S}$ - Hardware/Software Mode Select, PIN 13**

When high, the device pins control device operation; when low, the value entered by a prior configuration write controls device operation.

**$\overline{CS}$ - Chip Select, PIN 1**

When high, all signal activity on the SID, R/$\overline{W}$ and SCLK pins is ignored. The DRDY and $\overline{ERROR}$ signals indicate the status of the chip's internal operation.

**R/$\overline{W}$ - Read/Write, PIN 28**

Used in conjunction with $\overline{CS}$ such that when both signals are low, the filter inputs data from the SID pin on the falling edge of SCLK. If $\overline{CS}$ is low and R/$\overline{W}$ is high, the filter outputs data on the SOD pin on the rising edge of SCLK. R/$\overline{W}$ low floats the SOD pin allowing SID and SOD to be tied together, forming a bidirectional serial data bus.

**SCLK - Serial Clock, PIN 26**

Clock signal generated by host processor to either input data on the SID input pin, or output data on the SOD output pin. For write, data must be valid on the SID pin on the falling edge of SCLK. Data changes on the SOD pin on the rising edge of SCLK.

**SID - Serial Data Input, PIN 25**

Data bits are presented MSB first, LSB last. Data is latched on the falling edge of SCLK.

**RSEL - Register Select, PIN 27**

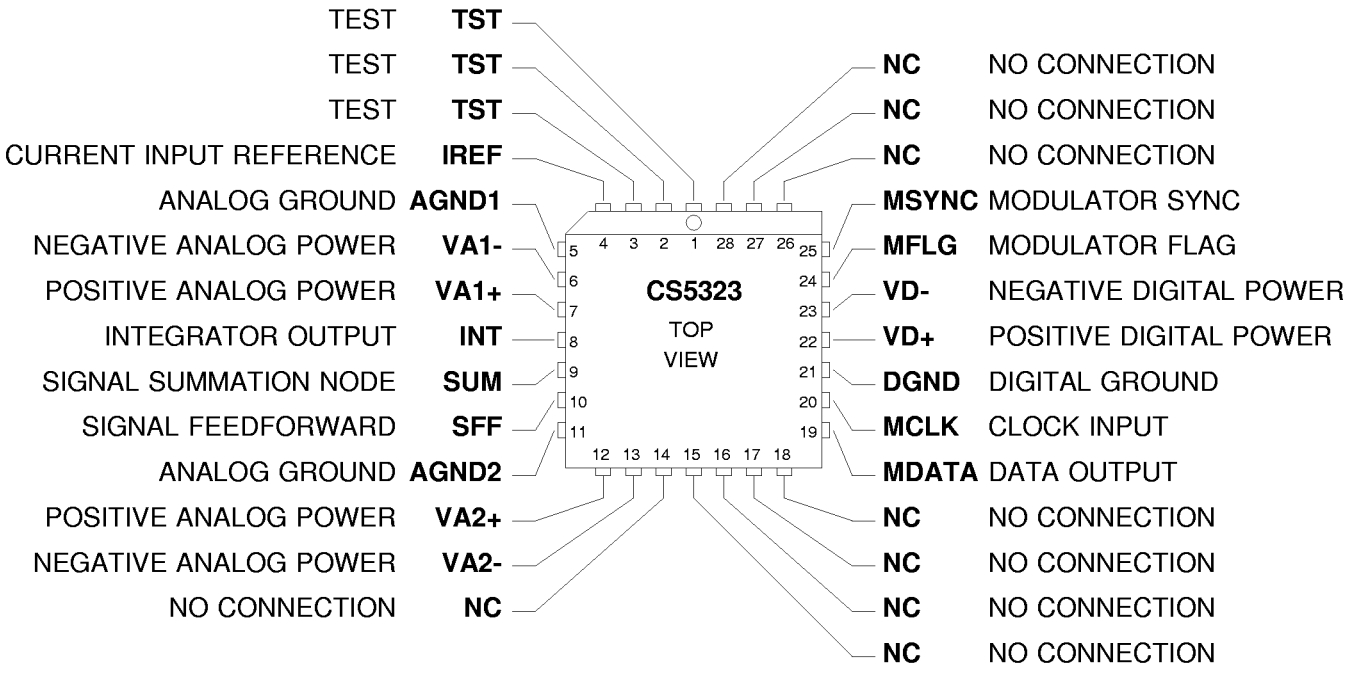
Selects conversion data when high, or status data when low.

**USEOR - Use Offset Register, PIN 15**

Use offset register value to correct output words when high. Output words will not be offset corrected when low.

**ORCAL - Offset Register Calibrate, PIN 19**

Initiates an offset calibration cycle when SYNC goes high after ORCAL has been toggled from low to high. The offset value is output on the 57th word following SYNC. Subsequent words will have their offset correction controlled by USEOR.




## CS5323 PIN DESCRIPTIONS

### *Power Supplies*

**VA1+, VA2+ – Positive Analog Power, PINS 7, 12**
Positive analog supply voltage. Nominally +5 Volts.

**VA1-, VA2- – Negative Analog Power, PINS 6, 13**
Negative analog supply voltage. Nominally -5 Volts.

**AGND1, AGND2 – Analog Ground, PINS 5, 11**
Analog ground reference.

**VD+ – Positive Digital Power, PIN 22**
Positive digital supply voltage. Nominally +5 Volts.

**VD- – Negative Digital Power, PIN 23**
Negative digital supply voltage. Nominally -5 Volts.

**DGND – Digital Ground, PIN 21**
Digital ground reference.

*Analog Inputs*

**IREF – Current Input Reference Node, PIN 4**

This node accepts a 1 mA reference current to set the signal gain of the A/D converter.

**SFF – Signal Feedforward, PIN 10**

The input signal is fed forward around the integrator input stage by means of this input pin. This maximizes signal performance.

**SUM – Signal Summation node, PIN 9**

This is the input integrator virtual ground summing junction. The external integrator input resistor and integrating capacitor are connected to this node, along with a 250 µA bias current network.

**INT – Integrator Output, PIN 8**

Output pin of the input integrator stage. The external integrating capacitor is connected to this pin for proper operation.

*Digital Inputs*

**MCLK – Clock Input, PIN 20**

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

**MSYNC – Modulator Sync, PIN 25**

A transition from a low to high level on this input will re-initialize the CS5323. MSYNC resets a divide-by-four counter to align the output bit stream from the CS5323 for proper input to the CS5322.

*Digital Outputs*

**MDATA – Modulator Data Output, PIN 19**

Data will be presented in a one-bit serial data stream at a bit rate of 256 kHz.

**MFLG – Modulator Flag, PIN 24**

A transition from a low to high level signals that the CS5323 modulator is unstable due to an over-range on the analog input. A Status Bit will be set in the digital filter indicating an error condition.

*Miscellaneous*

**TST – Test, PINS 1,2,3**

Reserved for production test facility. Should be tied to DGND for normal operation.

**NC – No Connection, PINS 14,15,16,17,18,26,27,28**

No internal connection. Tie to ground for optimum operation.

## PARAMETER DEFINITIONS

### Dynamic Range

The ratio of the full-scale (rms) signal to the broadband (rms) noise signal. Broadband noise is measured with the input grounded within the bandwidth of 1 Hz to $f_3$ Hz. Units in dB.

### Signal-to-Distortion

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to $f_3$ Hz. Units in dB.

### Intermodulation Distortion

The ratio of the rms sum of the two test frequencies (50 and 70 Hz) which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the the bandwidth of dc to $f_3$ Hz. Units in dB.

### Full Scale Error

The ratio of the difference between the value of the voltage reference and analog input voltage to the full scale span (two times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted. Measurement of this parameter uses the circuitry illustrated in the System Connection Diagram. Units in %.

### Full Scale Drift

The change in the Full Scale value with temperature. Units in %/°C.

### Offset

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5323/22 of 000000(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

### Offset Drift

The change in the Offset value with temperature. Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in µV/°C.

# • Notes •

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**CDB5323**

# Evaluation Board for CS5323 and CS5322

## Features

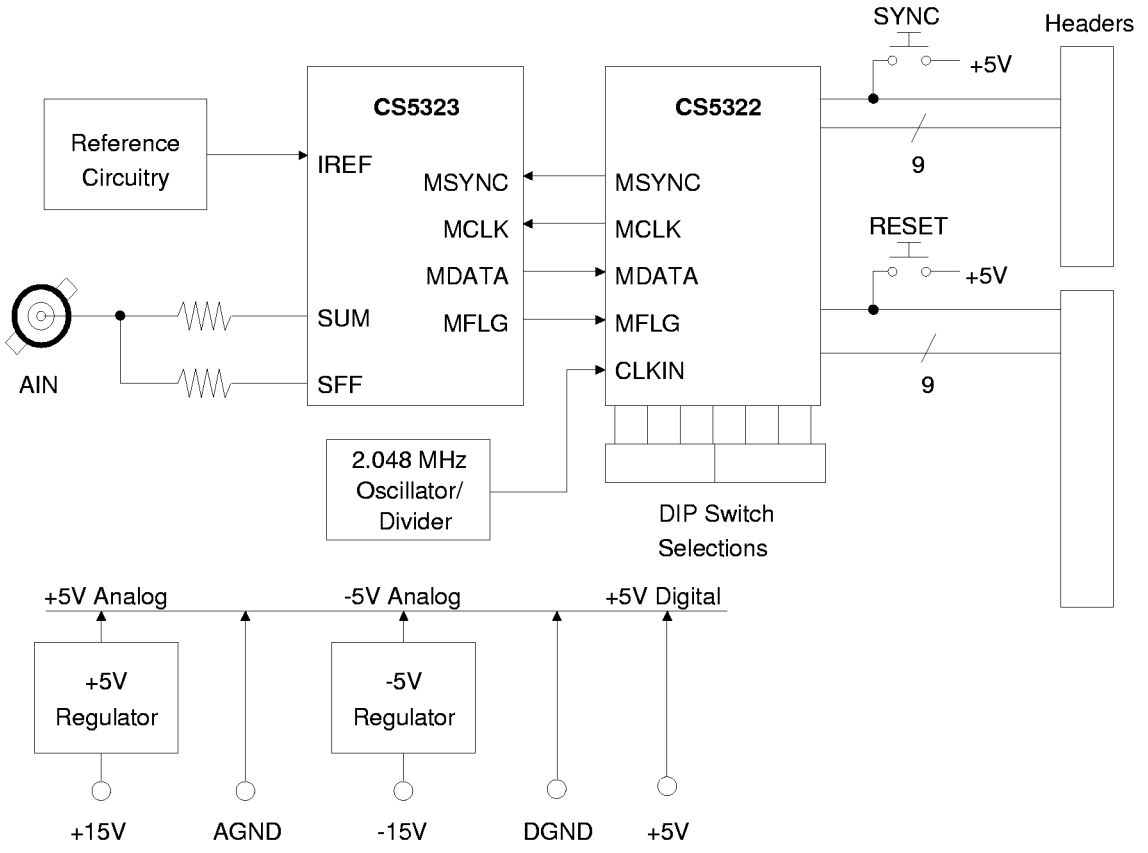
- DIP switch control of all CS5322 logic pins
- Header control of all CS5322 logic pins
- Supports manual operation of RESET and SYNC

## Description

The CDB5323 is an evaluation board that allows laboratory characterization of the CS5322/CS5323 A/D converter chip-set. The chip-set supports seven different selectable word rates: 4kHz, 2kHz, 1kHz, 500Hz 250Hz, 125Hz and 62.5Hz. Input to the board is 20 volts peak-to-peak. Output is via header connections to the CS5322 serial interface.

**ORDERING INFORMATION**

CDB5323 Evaluation Board





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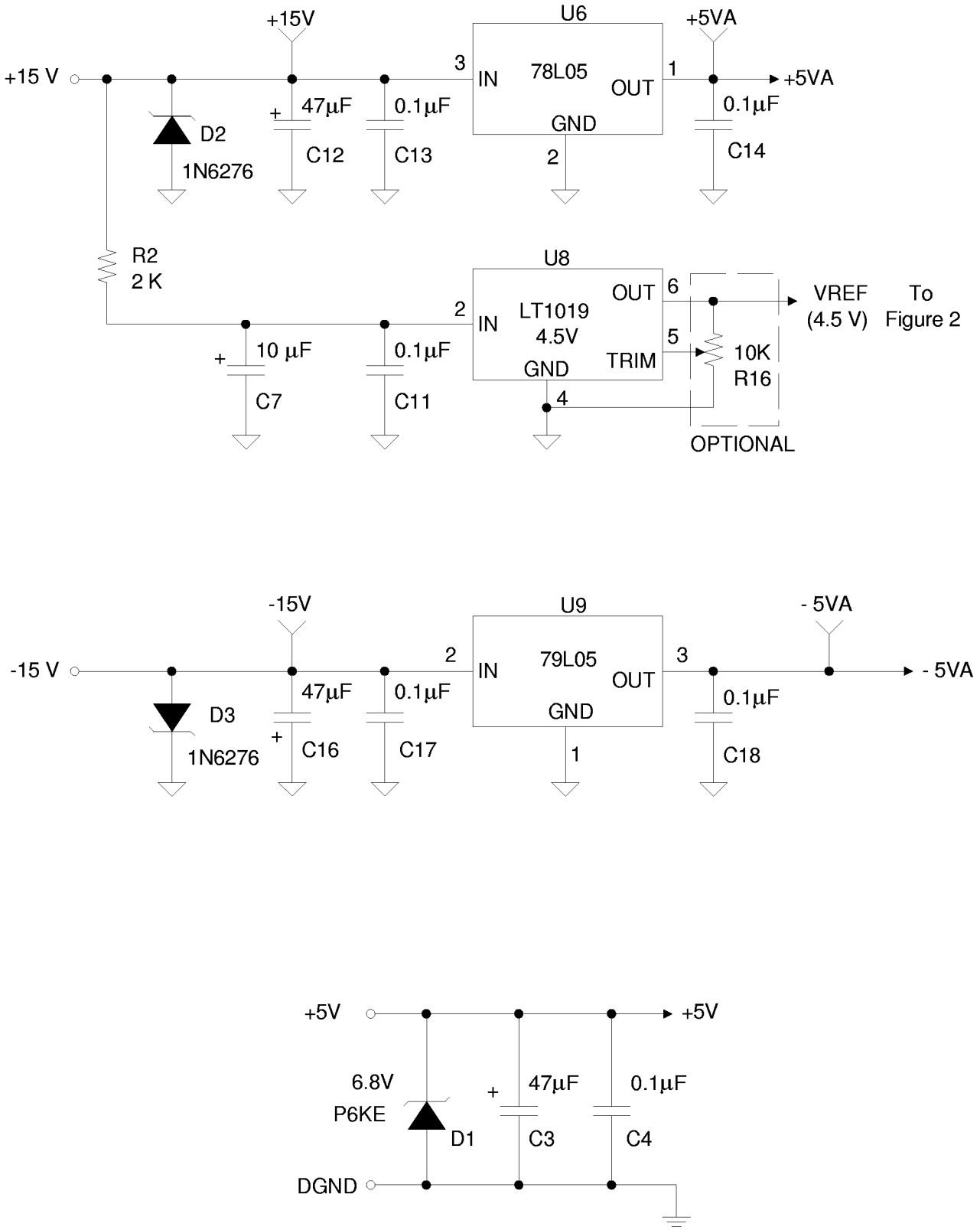


**Figure 1. Power Supplies**

## OVERVIEW

The CDB5323 evaluation board requires three separate power supplies for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The +5V input supplies the CS5322 filter and logic support devices on the board. The +15V and -15V inputs are regulated down to provide +5V and -5V supplies necessary for the CS5323 modulator. Figure 1 also illustrates the LT1021 10V reference used with the CS5323 modulator.

Figure 2 illustrates the CS5323 modulator circuitry, including the analog BNC input for the test signal source. Figure 3 illustrates the 2.048 MHz oscillator and dual D flip flop clock

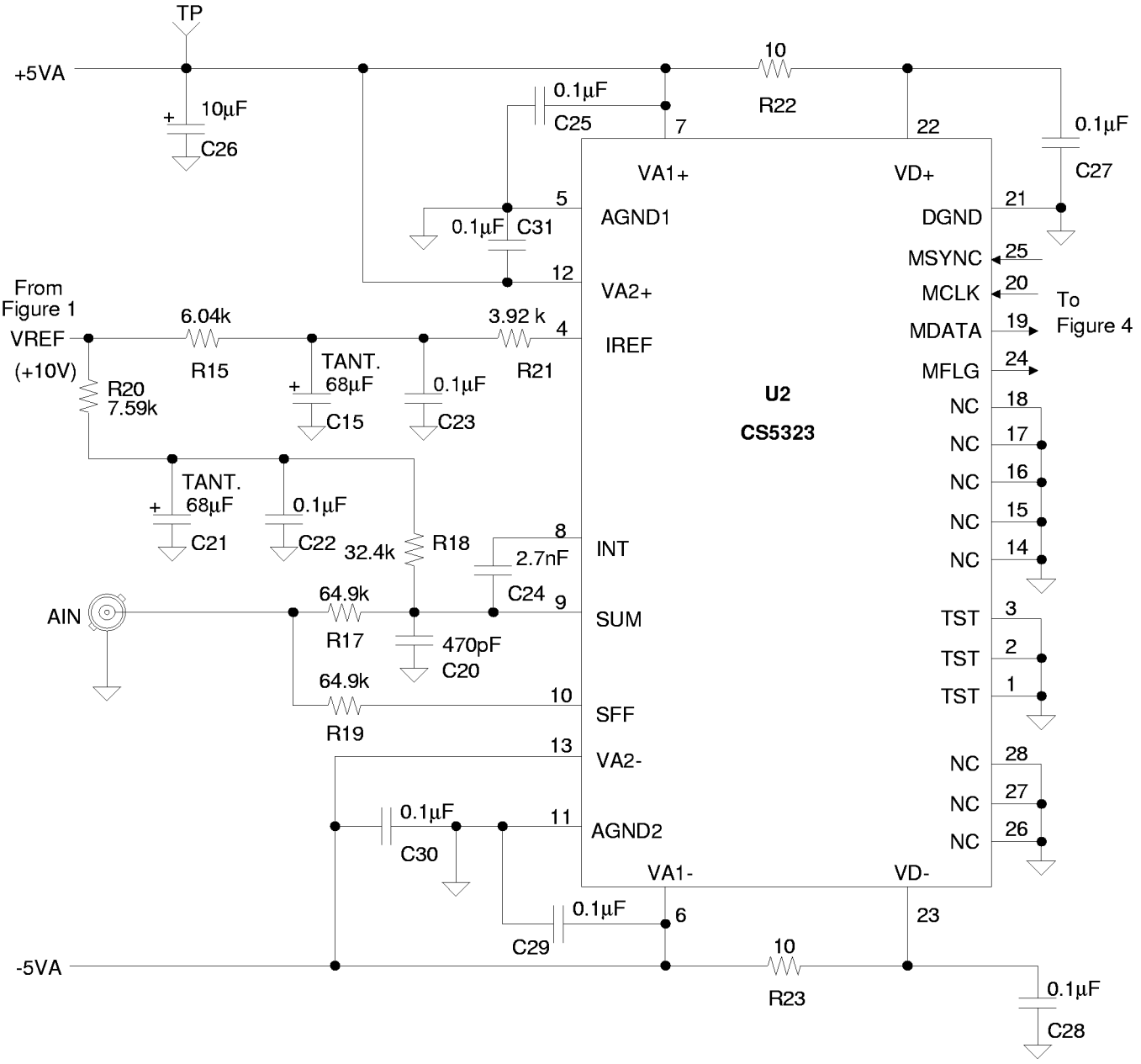


**Figure 2. CS5323 Modulator Input Circuitry.**

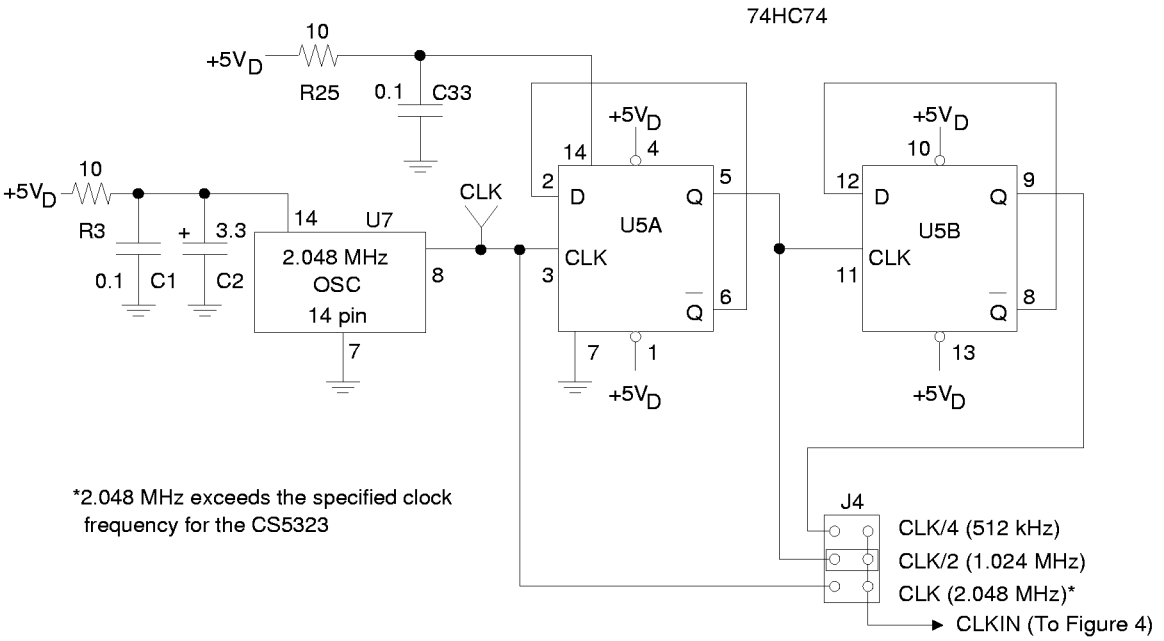


**Figure 3. Oscillator / Divider**

divider. Note that both the oscillator and the divider are separately decoupled from the +5V supply to reduce clock jitter which can be introduced from noisy supplies. Jumper J4 should be set in the CLK/2 position to source 1.024 MHz to the CS5322 chip for normal operation. If operation from 512 kHz clock is desired, the J4 jumper should be changed to the CLK/4 position. The board can be tested at 512 kHz without modification. In production applications, the CS5323 integrator capacitor (C24) should be doubled to 5.6 nF for 512 kHz operation to achieve optimum performance.

The digital interface pins to the CS5322 filter chip are all available on the header connectors J1, J2, and J3 as shown in Figures 4, and 5. Note that one row of pins on each of the headers is ground. It is advised that any connections made to control lines be done with twisted pair ribbon cable; with each twisted pair containing one signal and one ground connection. This minimizes radiated noise.

## CAUTION!

Caution is advised when interfacing the evaluation board to any circuitry powered from another source. For example, when interfacing to a computer I/O card be sure that the evaluation board and the computer are both powered up before connecting to the evaluation board headers. Always disconnect header connections when powering down the board but not the computer. Failure to follow this advice may cause damage to either the computer I/O or to the CS5322, because the computer outputs try to power the CDB5322/23 board.

Tables 1 and 2 illustrate the DIP switch positions of switches S3 and S4. The switch positions with asterisks indicate preferred settings for driving the interface of Figure 6.

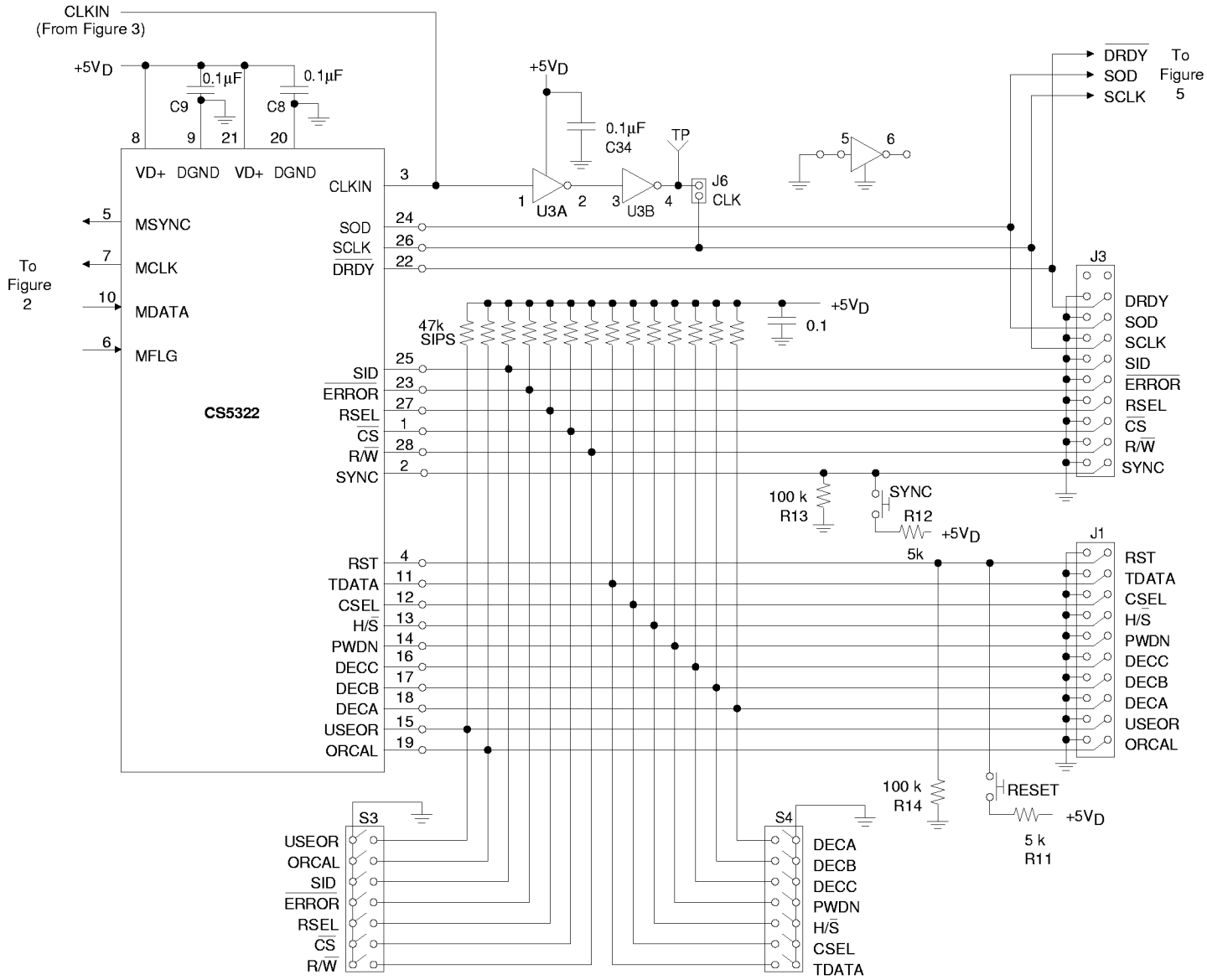


**Figure 4. CS5322 Filter Interface**

| | | |
|---|---|---|
| USEOR | ON* | Do not use offset register |
| | OFF | Use offset register |
| ORCAL | ON* | Disable offset register calibration |
| | OFF | Enable offset register calibration |
| SID | ON | Sets SID to Logic 0 |
| | OFF* | Allows pull-up on SID line |
| ERR | ON | Sets ERR to logic 0 |
| | OFF* | Allows CS5322 ERROR output |
| RSEL | ON | Select status register |
| | OFF* | Select conversion data register |
| CS | ON* | Chip select active |
| | OFF | Chip select inactive |
| R/$\overline{W}$ | ON | Enables write mode via SID pin |
| | OFF* | Enables read mode via SOD pin |

OFF = OPEN = 1

*Default to use Figure 6 interface.

**Table 1. S3 DIP Switch Selections**

| | | |
|---|---|---|
| DECA | Selection via hardware pins | **ABC Output Word Rate**<br>0 0 0 62.5<br>1 0 0 125<br>0 1 0 250<br>1 1 0 500<br>0 0 1 1000<br>1 0 1 2000<br>0 1 1 4000 |
| DECB | | |
| DECC | | |
| PWDN | ON* | Normal Operation |
| | OFF | Power down active |
| H/$\overline{S}$ | ON | Selects configuration register for operating mode |
| | OFF* | Select hardware pins for operating mode |
| CSEL | ON* | Selects MDATA from modulator |
| | OFF | Selects TDATA as filter input |
| TDATA | ON* | Sets TDATA input to logic 0 |
| | OFF | Enables TDATA from J1 header |

OFF = OPEN = 1

*Default to use Figure 6 interface.

**Table 2. S4 DIP switch selections**

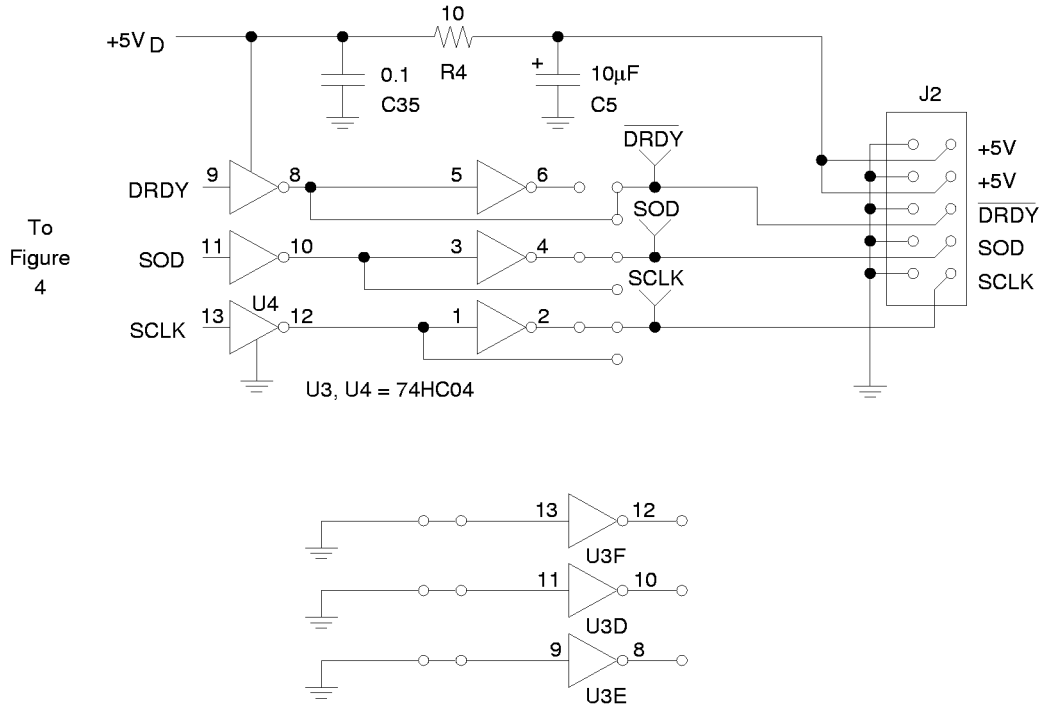


**Figure 5. Serial Latch Interface**

Figure 5 illustrates the logic used to drive connections at header J2.

By using the signals at header J2, the evaluation board can be set up to output its conversion words into three 74HC595 serial to parallel registers. This provides 24-bit parallel data. Figure 6 illustrates the circuitry which can be interfaced to the J2 connections to provide an isolated digital interface to three 74HC595 registers (the circuitry of Figure 6 is not provided on the board). Signals from connector J2 (+5 volts, GND, SCLK, SOD, and $\overline{\text{DRDY}}$) are interfaced to the GND1 side of the opto-isolated interface. The 74HC595 registers require SCLK rising to latch data bits and DRDY rising to parallel latch data. Jumpers must be placed to select the proper phase of these signals as the CS5322 provides data bits to be latched by the falling edge of SCLK and causes DRDY to fall when the last data bit is clocked out. A flip-flop is used to delay DRDY by one-half SCLK cycle before it is used to latch the parallel latch. Jumper J6 (CLK) is used to connect the 1.024 MHz clock as the SCLK signal to clock serial data from the chip. A second isolated +5 volts should be provided to the GND2 side of the interface. Opto-isolation eliminates any ground loop between the board and the computer interface.

The CS5322 filter should be set up for hardware mode (H/$\overline{\text{S}}$ on switch S4 open). DIP switch S4 can then be used to select the desired output word rate. After the selection on the DECA, DECB, and DECC positions of the S4 DIP switch, the S2 RESET switch must be activated, followed by the S1 SYNC switch (unless these signals are controlled via the J1 and J3 header signals).

Figure 7 illustrates the component layout of the board while figures 8 and 9 illustrate the board layout (not to scale).

## Using the Evaluation Board

Connect the appropriate power supplies to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency(50/60 Hz) interference.

Power up the supplies. Then connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter chip set will exceed the capability of most signal generators, especially with respect to noise and line frequency interference.

Once power has been applied to the board, connect the ribbon cable to the appropriate headers (J1, J2, and/or J3). The reset and the sync signals to the CS5322 must be applied before normal operation can commence. This can be done by using the S2 RESET switch and the S1 SYNC switch or by interfacing to these signals via the J1 and J3 headers.

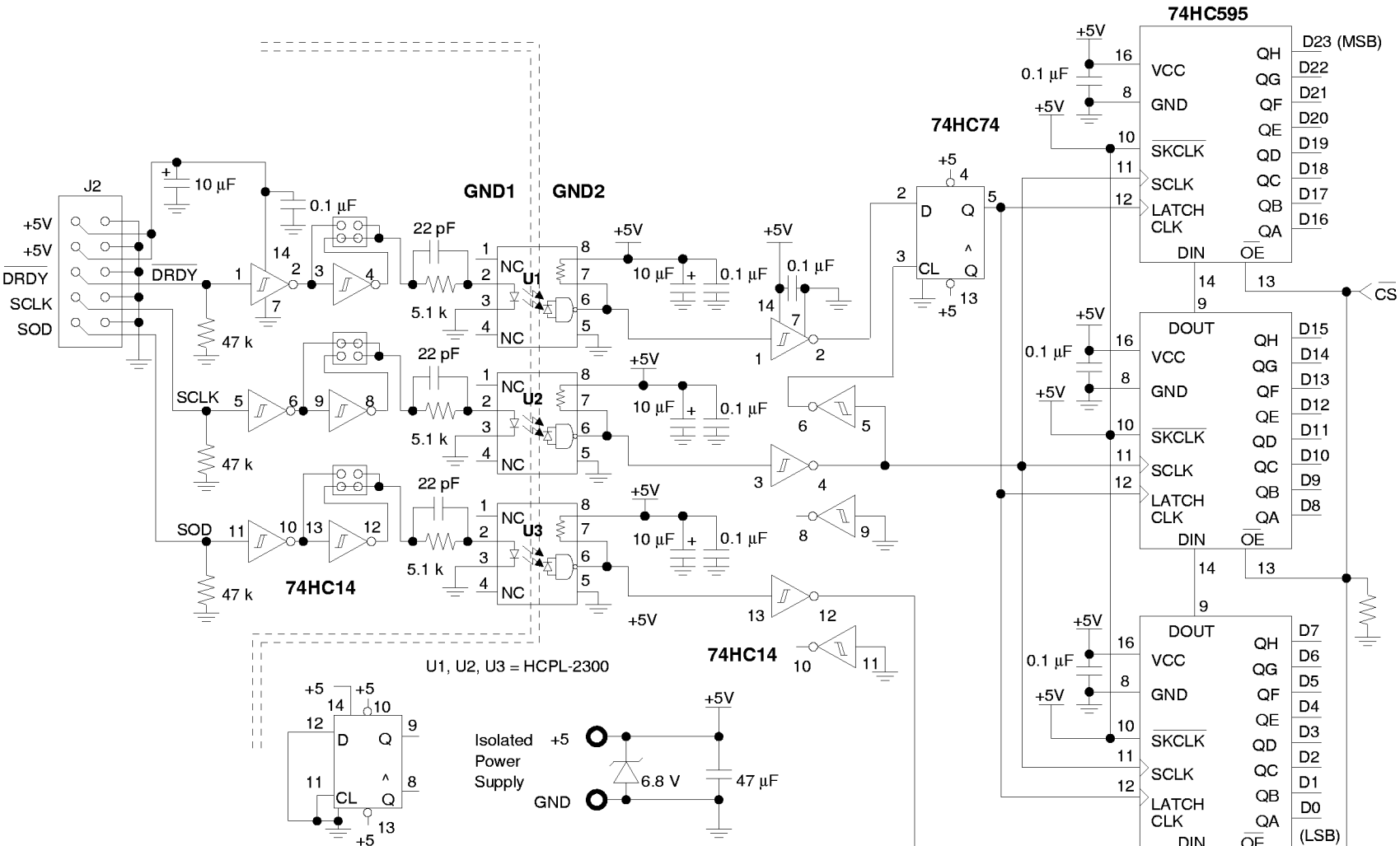


**Figure 6. Suggested Opto-coupled Interface Between A/D and Serial-to-parallel Registers (Not Provided)**

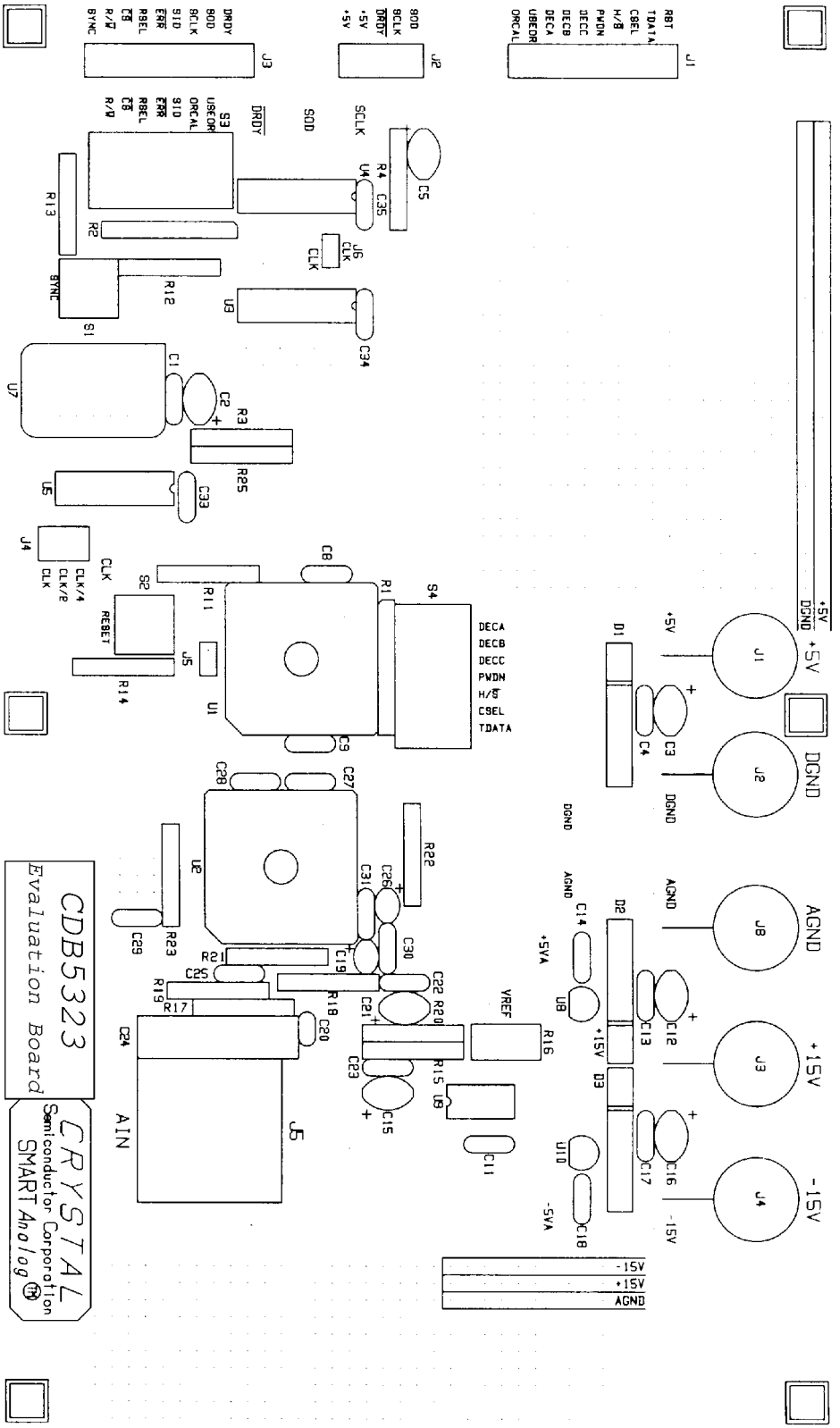


**Figure 7. CDB5323 Component Layout (Not to Scale)**

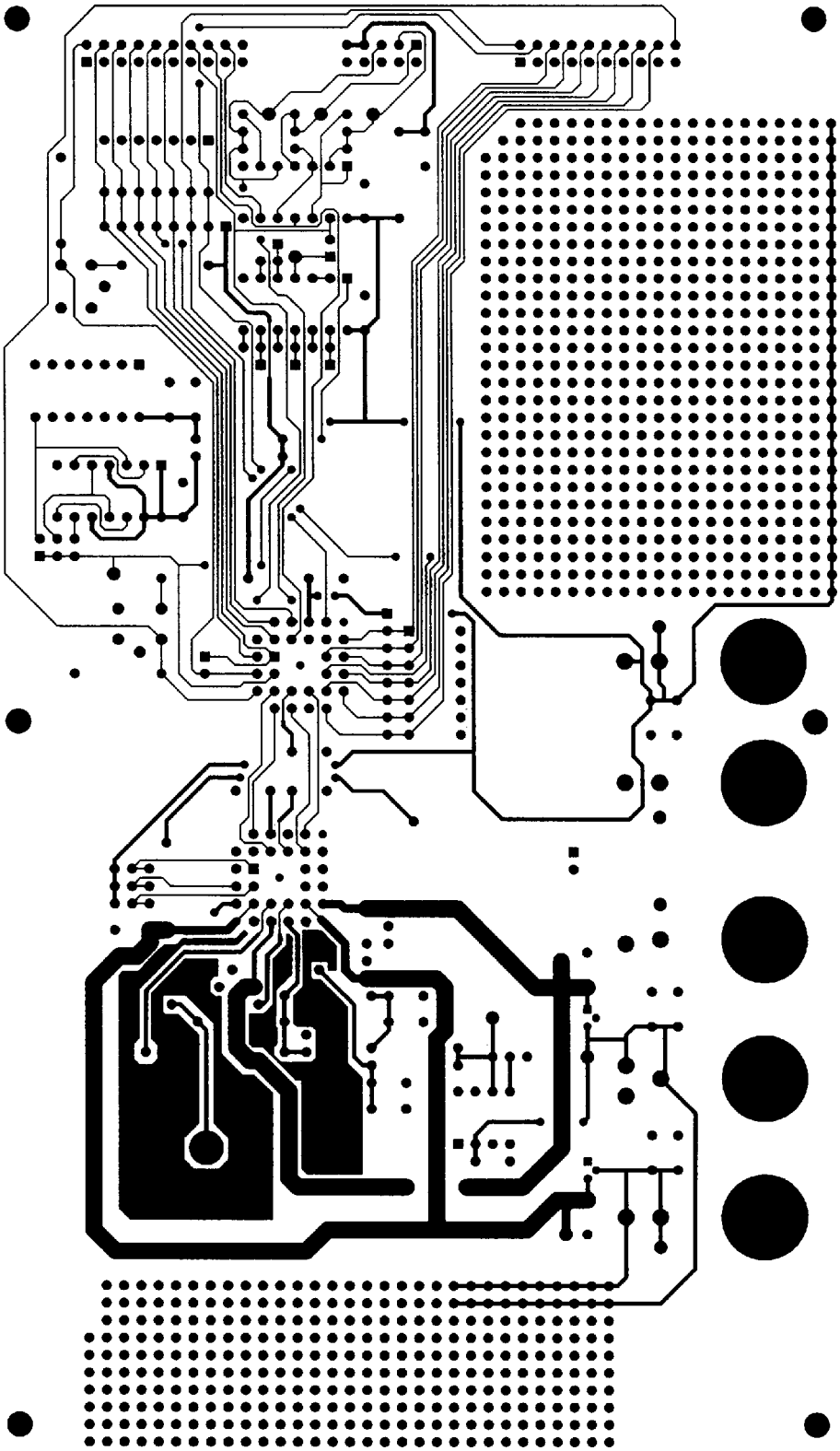

Figure 8. CDB5323 Solder Trace Layer (Not to Scale)

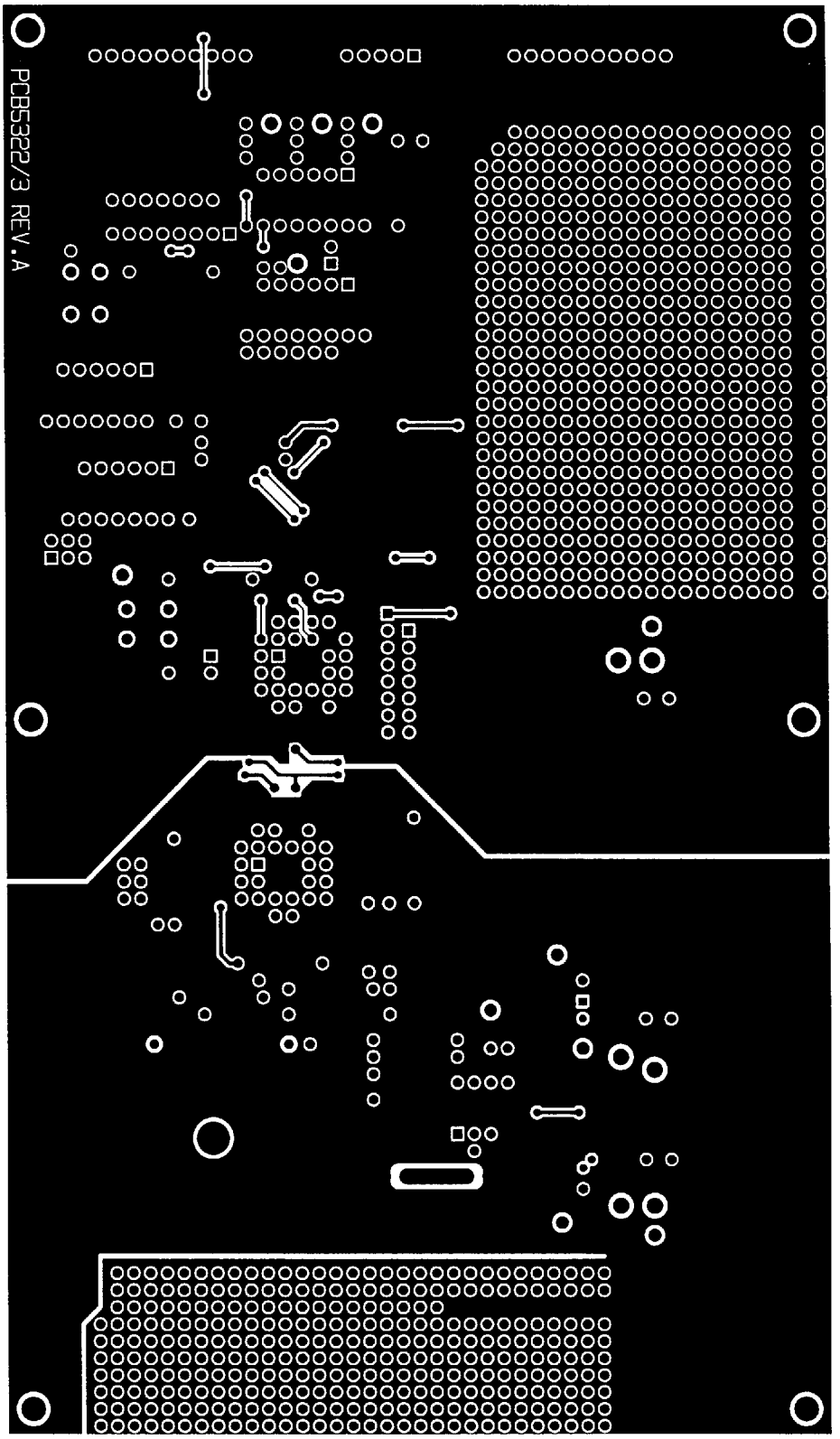


Figure 9. CDB5323 Ground Plane Layer (Not to Scale)