Semiconductor Corporation

# CS5345

## Low Power, Stereo A/D Converter for Digital Audio

### Features

- Single +5 V Power Supply
- 91 dB Dynamic Range
- Linear Phase Digital Anti-Alias Filtering
  0.05dB Passband Ripple
  73.5dB Stopband Rejection
- Low Power Dissipation: 100 mW
  Power-Down Mode for Portable Applications
- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Internal 64X Oversampling
- Evaluation Board Available

### General Description

The CS5345 is a complete stereo analog-to-digital converter which performs anti-alias filtering, sampling and analog-to-digital conversion generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

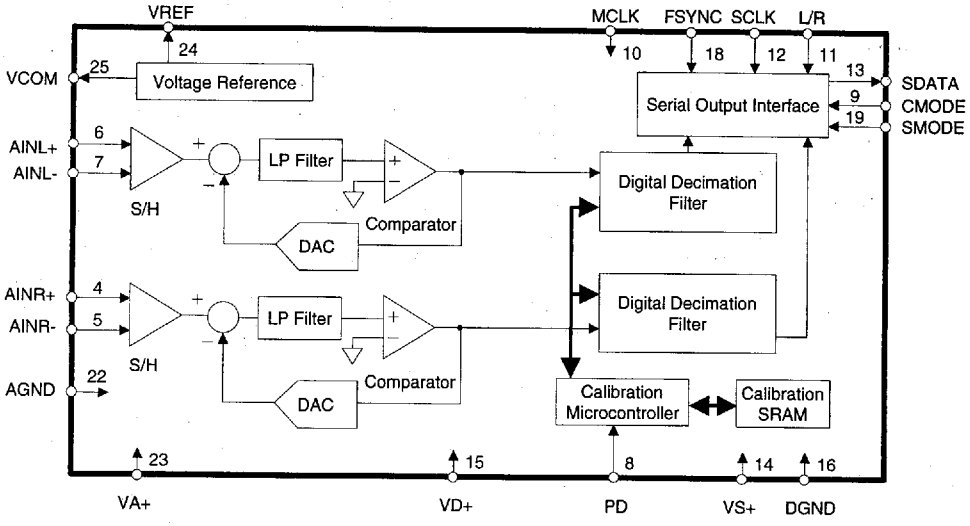
The CS5345 operates from a single +5V supply and requires only 100 mW for normal operation, making it ideal for battery-powered applications.

The ADC uses delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The linear-phase digital filter has a passband of dc to 22 kHz, 0.05 dB passband ripple and >73.5 dB stopband rejection.

The device is available in a 0.3" wide 28-pin SOIC surface mount package.

**ORDERING INFORMATION:**

| Model | Temp. Range | Package Type |
|---|---|---|
| CS5345-KS | 0° to 70°C | 28-pin plastic SOIC |
| CDB5345 | | Evaluation Board |




*Preliminary Product Information* | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.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## ANALOG CHARACTERISTICS ($T_A$ = 25°C; VA+, VS+, VD+ = 5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 150Ω with 1500 pF across AIN+, AIN-; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified, Logic 0=0V, Logic 1=VD+.)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Resolution | | | 16 | - | - | Bits |
| ***Dynamic Performance*** | | | | | | |
| Dynamic Range | A-weighted | | -<br>- | 91<br>88 | -<br>- | dB<br>dB |
| Total Harmonic Distortion+Noise | 0dB<br>-20dB<br>-60dB | THD+N | -<br>-<br>- | -86<br>-68<br>-28 | -<br>-<br>- | dB<br>dB<br>dB |
| Total Harmonic Distortion | 0dB | THD | - | .0018 | - | % |
| Interchannel Phase Deviation | | | - | 0.0001 | - | Degree |
| Interchannel Isolation | (dc to 20 kHz) | | - | 100 | - | dB |
| ***dc Accuracy*** | | | | | | |
| Interchannel Gain Mismatch | | | - | 0.05 | - | dB |
| Gain Error | | | - | ±2 | ±5 | % |
| Gain Drift | | | - | 60 | - | ppm/°C |
| Bipolar Offset Error | (After Calibration) | | - | ±5 | ±30 | LSB |
| ***Analog Input*** | | | | | | |
| Differential Input Voltage Range (Full Scale) (Note 1) | | VIN | 3.46 | 3.75 | 4.06 | Vpp |
| Input Impedance | | ZIN | - | 85 | - | kΩ |
| ***Power Supplies*** | | | | | | |
| Power Supply Current<br>Normal Operation | VA+<br>(VD+) + (VS+) | IA+<br>ID+ | -<br>- | 10.5<br>9.5 | 16<br>14 | mA<br>mA |
| Power Supply Current<br>Power-Down Mode | VA+<br>(VD+) + (VS+) | IA+<br>ID+ | -<br>- | 50<br>50 | -<br>- | µA<br>µA |
| Power Dissipation | <br>Power Down | | -<br>- | 100<br>0.5 | 150<br>- | mW<br>mW |

Notes: 1. The peak-to-peak input voltage range for each input is equal to {(VA+)-VREF}x0.625. The nominal value for (VA+) - VREF is 3 Volts. The differential peak-to-peak input voltage is equal to twice the individual voltage range. (See Figure 5)

* Refer to Parameter Definitions at the end of this data sheet.

Specifications are subject to change without notice.

## DIGITAL FILTER CHARACTERISTICS

($T_A$ = 25 °C; VA+, VS+, VD+ = 5V ± 5%; Output word rate (Fs) of 48 kHz)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Passband | (-0.05 dB)<br>(-2.8 dB)<br>(-6.5 dB) | | -<br>-<br>- | 0 to 18<br>0 to 22<br>0 to 24 | -<br>-<br>- | kHz<br>kHz<br>kHz |
| Passband Ripple | | | - | - | ±0.05 | dB |
| Stopband | | | 32 | - | 3040 | kHz |
| Stopband Attenuation | (Note 2) | | 73.5 | - | - | dB |
| Group Delay (OWR = Output Word Rate) | (Note 3) | $t_{gd}$ | - | 8/OWR | - | s |
| Group Delay Variation vs. Frequency | | $\Delta t_{gd}$ | - | - | 0.0 | µs |

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency ( n x 3.072MHz ±18kHz where n = 0,1,2,3...).

3. Group delay for OWR = 48kHz, $t_{gd}$ = 8/48kHz = 167µs

## DIGITAL CHARACTERISTICS

($T_A$ = 25 °C; VA+, VS+, VD+ = 5V ± 5%)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IH}$ | 70% VD+ | - | - | V |
| Low-Level Input Voltage | $V_{IL}$ | - | - | 30% VD+ | V |
| High-Level Output Voltage at Io = -20 µA | $V_{OH}$ | 4.4 | - | - | V |
| Low-Level Output Voltage at Io = 20 µA | $V_{OL}$ | - | - | 0.1 | V |
| Input Leakage Current | Iin | - | 1.0 | - | µA |

## ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DC Power Supplies: | Positive Analog<br>Positive Digital | VA+<br>VD+ | -0.3<br>-0.3 | -<br>- | +6.0<br>+6.0 | V<br>V |
| Input Current, Any Pin Except Supplies | | Iin | - | - | ±10 | mA |
| Analog Input Voltage | | $V_{INA}$ | -0.3 | - | (VA+)+0.3 | V |
| Digital Input Voltage | | $V_{IND}$ | -0.3 | - | (VD+)+0.3 | V |
| Ambient Temperature (power applied) | | $T_A$ | -55 | - | +125 | °C |
| Storage Temperature | | $T_{stg}$ | -65 | - | +150 | °C |

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

## SWITCHING CHARACTERISTICS

($T_A$ = 25 °C; VA+, VS+, VD+ = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VA+, VS+, VD+; $C_L$ = 20 pF)

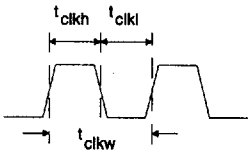
| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| MCLK Period (CMODE low) | $t_{clkw1}$ | 78.13 | - | 781.3 | ns |
| MCLK Low (CMODE low) | $t_{clkl1}$ | 31.25 | - | - | ns |
| MCLK High (CMODE low) | $t_{clkh1}$ | 31.25 | - | - | ns |
| MCLK Period (CMODE high) | $t_{clkw2}$ | 52.0 | - | 520.8 | ns |
| MCLK Low (CMODE high) | $t_{clkl2}$ | 20.83 | - | - | ns |
| MCLK High (CMODE high) | $t_{clkh2}$ | 20.83 | - | - | ns |
| L/R duty cycle | | 25 | - | 75 | % |
| SCLK Period | $t_{sclkw}$ | 312.5 | - | - | ns |
| SCLK Pulse Width Low | $t_{sclkl}$ | 100 | - | - | ns |
| SCLK Pulse Width High | $t_{sclkh}$ | 100 | - | - | ns |
| SCLK falling to SDATA valid | $t_{dss}$ | - | - | 70 | ns |
| L/R edge to MSB valid | $t_{lrdss}$ | - | - | 70 | ns |
| PD pulse width | $t_{pdw}$ | 150 | - | - | ns |
| PD falling to SDATA valid | $t_{pcf}$ | - | 8224/OWR | - | s |
| Rising SCLK to L/R edge delay | $t_{slr1}$ | 30 | - | - | ns |
| L/R edge to rising SCLK setup time | $t_{slr2}$ | 30 | - | - | ns |
| SCLK Falling to FSYNC delay | $t_{fs}$ | -70 | - | +70 | ns |

## RECOMMENDED OPERATING CONDITIONS

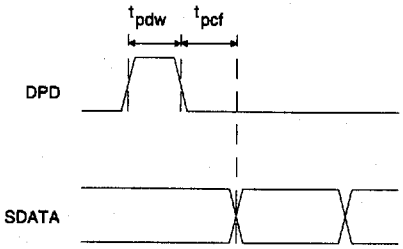
(AGND, DGND = 0V; all voltages with respect to ground)

| Parameter | | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| DC Power Supplies: | Positive Analog | (Note 5) | VA+ | 4.75 | 5.0 | 5.25 | V |
| | Positive Digital | | VD+ | 4.75 | 5.0 | 5.25 | V |
| | Positive Substrate | | VS+ | 4.75 | 5.0 | 5.25 | |
| Differential Analog Input Voltage | | (Notes 1&6) | VIN | - | 3.75 | - | Vpp |
| Analog Input Bias Voltage | | | | - | 0.5VA+ | - | V |

Notes: 5. VD+ must be within 0.3V of VA+.
6. The output codes will clip at full scale with differential input signals >3.75 Vpp.

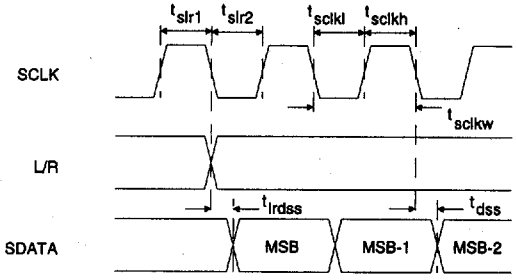



MCLK Definition

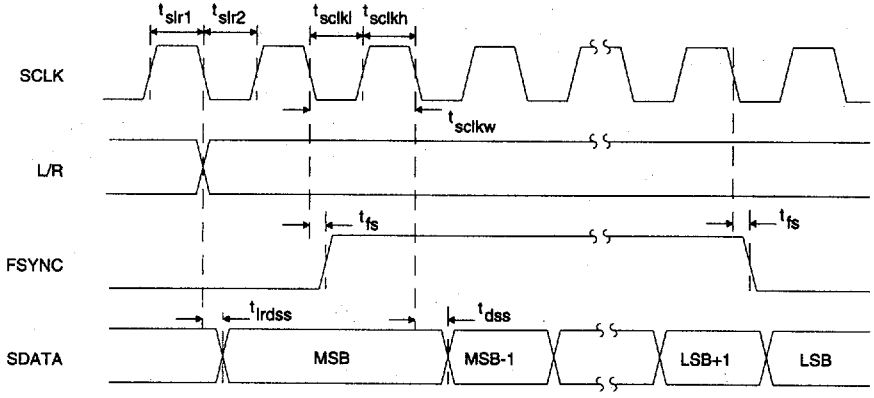



Power Down & SDATA Valid






SCLK to L/R & SDATA-Mode 1 (SMODE High), FSYNC Ignored
Mode 2 - FSYNC High (SMODE Low)




SCLK to L/R, SDATA & FSYNC - Mode 2 - FSYNC Controlled (SMODE Low)

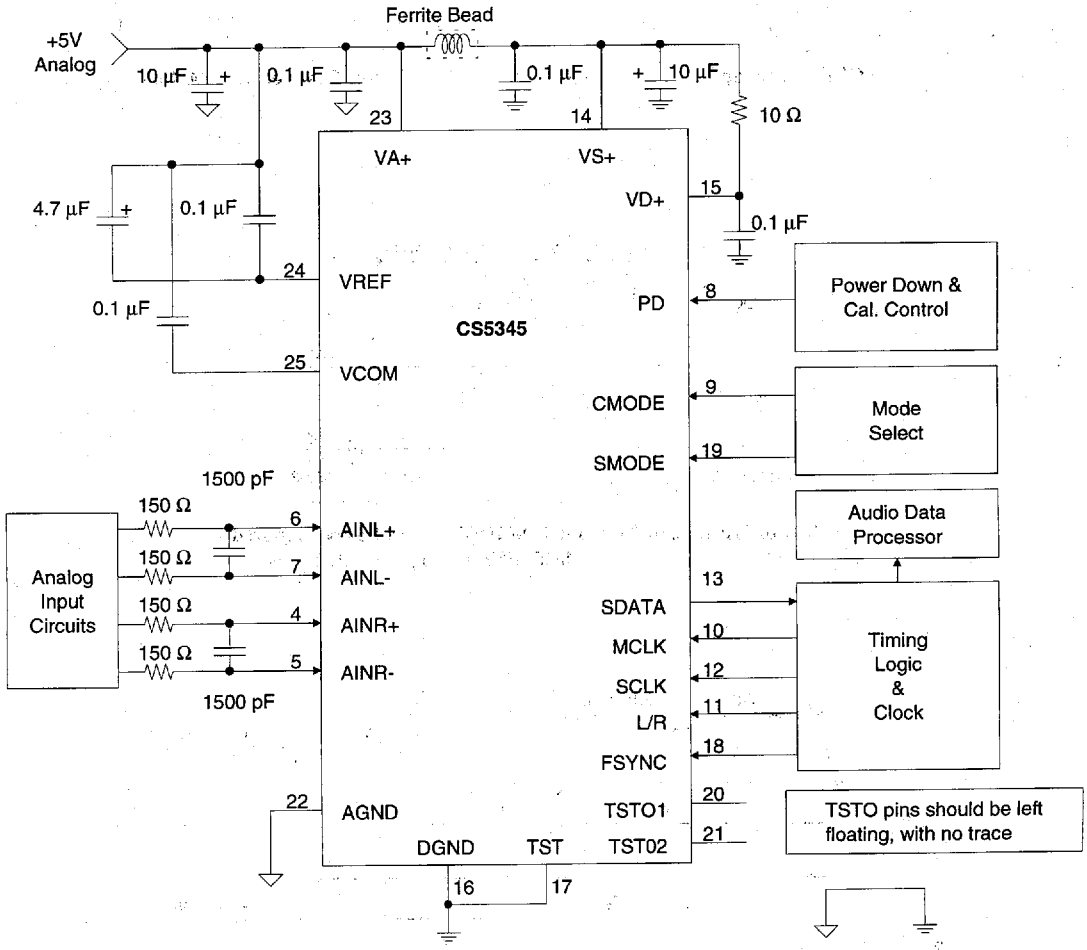



**Figure 1. Typical Connection Diagram**

## GENERAL DESCRIPTION

The CS5345 is a 16-bit, 2-channel A/D converter designed for stereo digital audio applications that require a single +5V supply. The device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for a differential input signal range of 3.75 Vpp. Offsets are internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption is 100 mW. This can be further reduced to .05 mW using the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside this ADC, see the references at the end of this data sheet.

| L/R (kHz) | CMODE | MCLK (MHz) | SCLK (MHz) |
|---|---|---|---|
| 32 | low | 8.192 | 2.048 |
| 32 | high | 12.288 | 2.048 |
| 44.1 | low | 11.2896 | 2.8224 |
| 44.1 | high | 16.9344 | 2.8224 |
| 48 | low | 12.288 | 3.072 |
| 48 | high | 18.432 | 3.072 |

**Table 1. Common Clock Frequencies**

## SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

3

### *Master Clock Input*

The master input clock (MCLK) into the ADC runs the digital filter and it is used to generate the delta-sigma modulator sampling clock. CMODE high will set the required MCLK frequency to 384 X the output word rate (OWR), while CMODE low will set the required MCLK frequency to 256 X OWR. Table 1 shows some common clock frequencies.

### *Serial Data Interface*

The serial data interface has 2 possible modes of operation. L/R, SCLK and FSYNC are inputs in both interface modes. L/R must be derived from MCLK and be equal to the OWR. SCLK should also be derived from MCLK and be equal to the delta-sigma modulator sample rate (64 X OWR) to eliminate the possibility of interference tones in the output data. An SCLK frequency of 32 X OWR is possible but may cause interference tones. Data bits are clocked out via the SDATA pin using SCLK, L/R and FSYNC inputs. The serial nature of the output data results in the left and right data words being read at different times. However, the words within a L/R cycle represent simultaneously sampled analog inputs.

Mode 1 (SMODE high) is shown in Figure 2. The falling edge of SCLK causes the ADC to output each data bit. Notice the one SCLK cycle delay between L/R edges and the data MSB. FSYNC is ignored and should be tied either High or Low in this mode. Mode 1 is compatible with $I^2S$.

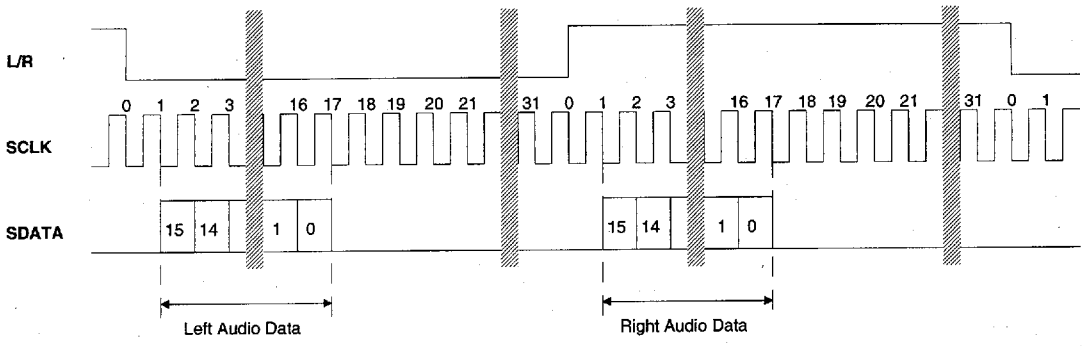



**Figure 2. Data Output Timing - Mode 1 (FSYNC High or Low)**

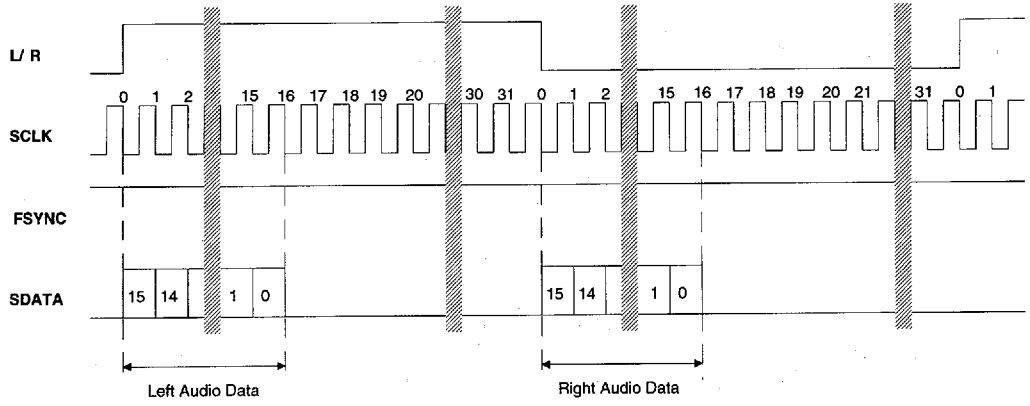



**Figure 3. Data Output Timing - Mode 2 - FSYNC High**

Mode 2-FSYNC High (SMODE low) is shown in Figure 3. The falling edge of SCLK causes the ADC to output each data bit with the exception of the MSB which is clocked out by the L/R edge.

In Mode 2-FSYNC Controlled, as shown in Figure 4, only the MSB is clocked out after the L/R edge with FSYNC low, SCLK is ignored. When it is desired to output data, bringing FSYNC high will enable SCLK to clock out data. This feature is particularly useful to position the data bits in time onto a common serial bus.

### *Analog Connections*

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+, AINR- and AINL+, AINL- pins. Each analog input will accept a maximum of 1.88 Vpp centered at +2.5 V. The + and - input signals are 180° out of phase resulting in a differential input voltage of 3.75 Vpp. Figure 5 shows the input signal levels for full scale.

The CS5345 samples the analog inputs at 3.072 MHz for a 12.288 MHz MCLK (CMODE low). The digital filter rejects all noise between

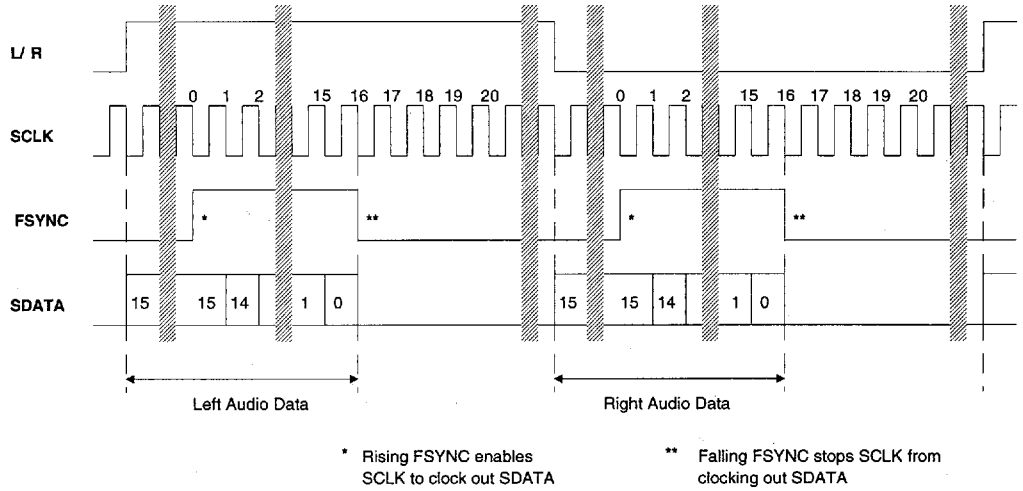



**Figure 4. Data Output Timing- Mode 2 - FSYNC Controlled**

32 kHz and (3.072 MHz-32 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 150 Ω resistor in series with each analog input and a 1500 pF capacitor across the inputs will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these will degrade signal linearity. NPO, COG and polyester film capacitors are acceptable. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

Figure 6 is a suggested active input buffer circuit which provides a differential signal and level shifts up to +2.5 V. This circuit has been implemented on the CDB5345 evaluation board which is available from Crystal Semiconductor.

The on-chip voltage reference ((VA+) - 3.0 V) is connected to VREF (pin 24). A 4.7 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached between VREF and VA+ eliminates the effects of high frequency noise. Notice that VREF is decoupled to VA+ not AGND. This requirement is a result of the modulator sampling between VREF and VA+. No load current may be taken from the VREF output pin.

An additional on-chip voltage reference {(VA+) - 2.5 V)}is connected to VCOM (pin 25). This output may be used to bias the analog input circuitry if a high impedance, low-bias current buffer is used.

### *Power-Down and Offset Calibration*

The ADC has a power-down mode wherein typical consumption drops to 0.5 mW. PD is the power down pin for the device. When high, it places the analog and digital circuitry in the power-down mode. Bringing this pin low will release the power-down mode and initiate a calibration sequence.

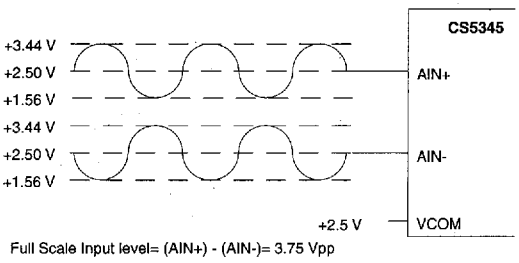



**Figure 5. Full Scale Input Voltage**

The delta-sigma modulator +/- inputs are internally disconnected from the AIN pins and shorted together during calibration. The digital section of the device measures and stores a value corresponding to the DC offset of each channel in the calibration registers. This calibration value is then subtracted from all future conversions during normal operation. 8224 L/R cycles are required for a calibration sequence. A short delay of approximately 18 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals. During calibration, the digital output of both channels is forced to a 2's complement zero.

### *Power-up Considerations*

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered, either through the application of power or by exiting the power-down mode. The voltage reference takes a longer time to reach a final value due to the presence of large external capacitance on the VREF pin. The calibration period is optimized to allow the reference to settle for capacitor values of up to 4.7 µF. The use of larger capacitors can cause erroneous calibration or make the device inoperable and is not recommended.

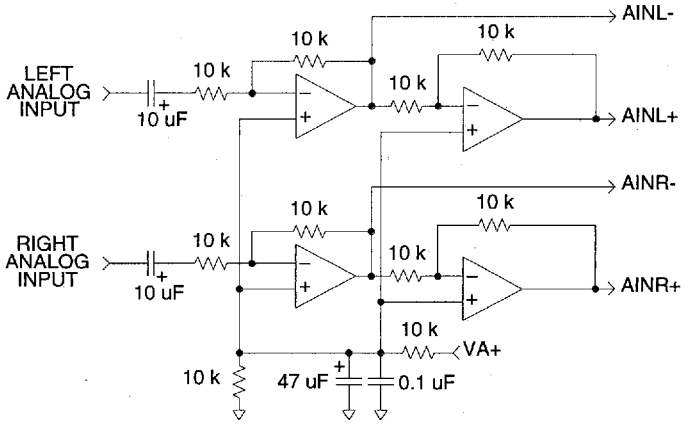



**Figure 6. Example Input Buffer Circuit**

### *Grounding and Power Supply Decoupling*

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5 V supply. VS+ and VD+ should be powered from VA+ via a ferrite bead to minimize noise coupling. To further minimize noise coupling into the ADC, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The Crystal Semiconductor application note "*Layout and Design Rules for Data Converters*" is available Crystal Semiconductor data books and should be considered required reading. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the CS5345.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

### *Synchronization of Multiple CS5345*

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling.

Synchronous sampling is achieved by connecting all PD pins to a single control signal and supplying the same L/R and MCLK to all converters.

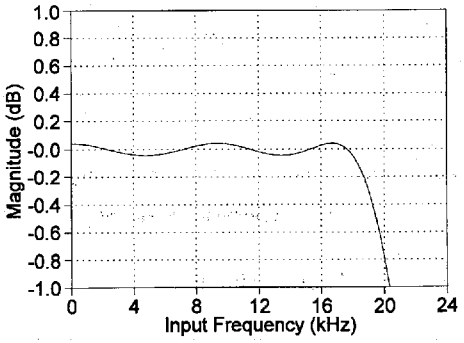



**Figure 8. CS5345 Digital Filter Passband Ripple**

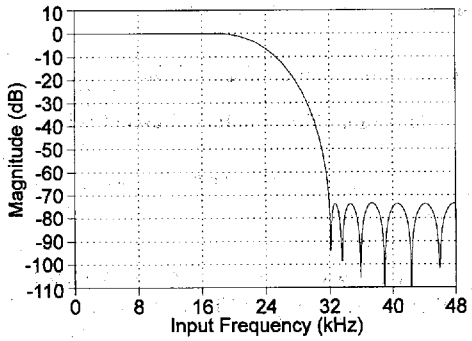



**Figure 7. CS5345 Digital Filter Stopband Rejection**

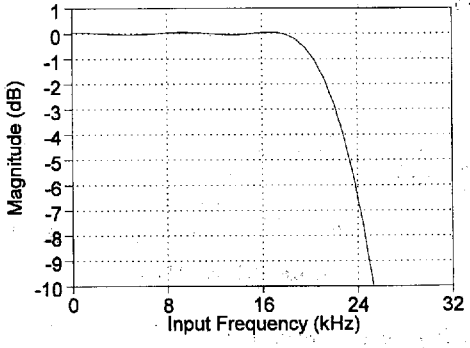



**Figure 9. CS5345 Digital Filter Transition Band**

## PERFORMANCE

### *Digital Filter*

Figures 7, 8, and 9 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple

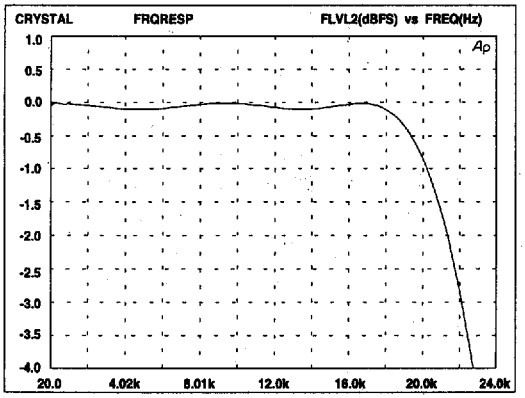



**Figure 10. Frequency Response**

is flat to ± 0.05 dB maximum.

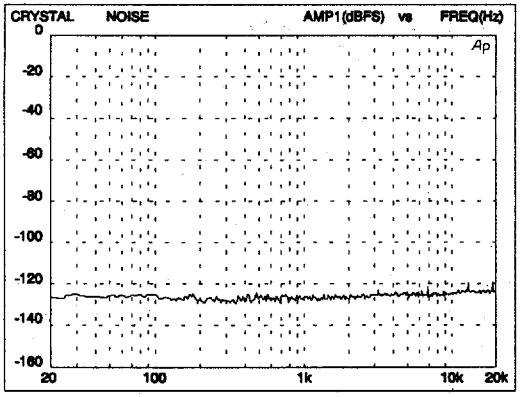



**Figure 11. Noise Floor**

### *Performance Measurements*

All the following performance measurements were taken using an Audio Precision System

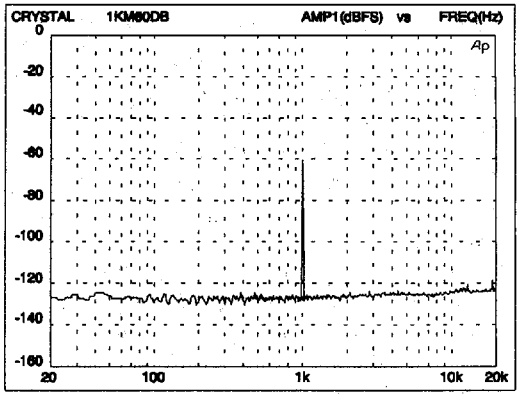



**Figure 12. 1 kHz -60 dB**

One Dual Domain tester. The CS5345 was in a CDB5345 evaluation board, running at 48 kHz word rate and interfaced to the System One via the digital audio interface using a CS8402 transmitter.

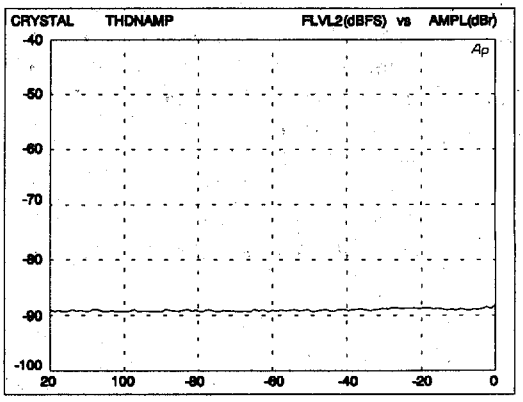



**Figure 13. THD+N vs Input Level at 1kHz**

Figure 10 shows the CS5345 frequency response.

Figure 11 shows the noise floor with zero input signal level. A 16 K point FFT was used.

Figure 12 shows a 1 kHz, -60 dB input signal FFT plot. Notice the lack of harmonic distortion

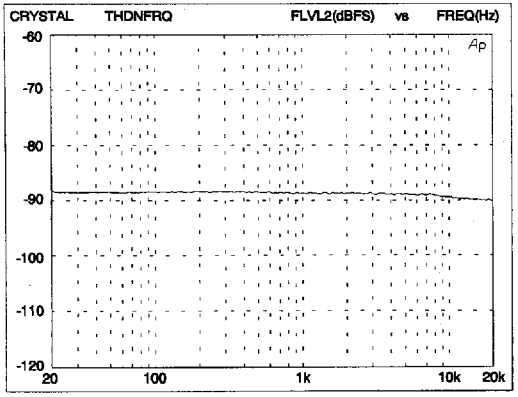



**Figure 14. THD+N vs Frequency at -1dB**

components. This is a direct result of the perfect differential non-linearity of the delta-sigma architecture

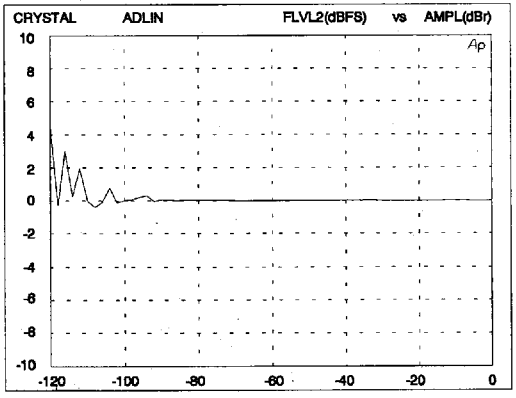


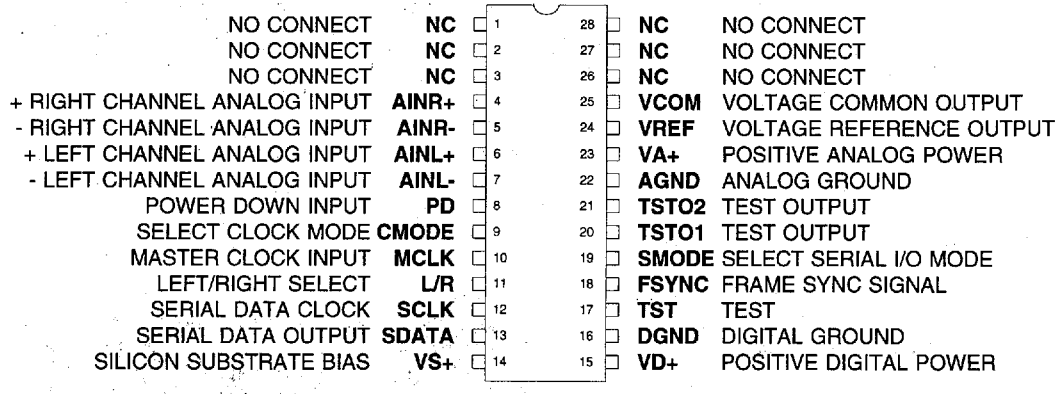

**Figure 15. Output Level Error vs Input Level**

Figure 13 shows the THD+N versus input level at 1 kHz. This plot indicates an unweighted dynamic range of 88 dB.

Figure 14 shows THD+N versus frequency at -1 dB input.

Figure 15 shows the linearity of the CS5345. The input signal is at 500 Hz and is varied from 0 dB (full scale) to -120 dB. At each input level, the output level is measured and compared to the perfect value. Any deviation is plotted as a deviation away from 0 dB. Notice the close conformance to perfect linearity, until the noise starts to influence the readings at about -100 dB.

## PIN DESCRIPTIONS




*Power Supply Connections*

**VA+- Analog Power, PIN 23**

Positive supply for the analog section. Nominally +5 volts.

**VS+ - Digital Power, PIN 14**

Positive supply for the silicon substrate. Nominally +5 volts.

**VD+ - Digital Power, PIN 15**

Positive supply for the digital section. Nominally +5 volts.

**AGND - Analog Ground, PIN 22**

Analog ground reference.

**DGND - Digital Ground, PIN 16**

Digital ground for the digital section.

*Analog Inputs*

**±AINL, ±AINR - Differential Left and Right Channel Analog Inputs, PINS 6, 7, 4, 5**

Analog input connections for the left and right input channels. A nominal differential input voltage of 3.75 Vpp will produce a full scale digital output.

*Analog Outputs*

**VREF - Voltage Reference Output, Pin 24**

Internal voltage reference output. Nominally (VA+) - 3.0 V. Must be bypassed to VA+ with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF electrolytic capacitor.

**VCOM - Voltage Common Output, PIN 25**

Nominally (VA+) - 2.5 volts. May be used to bias the analog input circuitry if an additional buffer is used.

*Digital Inputs*

**MCLK - Master Input Clock, PIN 10**

Sampling rates, output rates and digital filter characteristics scale to MCLK frequency. MCLK frequency is either 256 or 384 X the output word rate (see CMODE). For example, a 12.288 MHz MCLK corresponds to an output word rate of 48 kHz per channel with CMODE low.

**SCLK - Serial Data Clock, PIN 12**

SCLK is an input clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). Data is clocked out on the falling edge of SCLK. See the descriptions of Data Output Mode 1 and Mode 2.

**L/R - Left/Right Select, PIN 11**

L/R is an input which selects the left or right channel for output on SDATA. The L/R frequency must be at the output word rate. Although the outputs of each channel are transmitted at different times, the two words in an L/R cycle represent simultaneously sampled analog inputs.

Left channel data is on SDATA when L/R is low in Mode 1 (SMODE high). Right channel data is on SDATA when L/R is high. The MSB data bit appears on SDATA one SCLK cycle after L/R changes.

Left channel data is on SDATA when L/R is high in Mode 2 (SMODE low). Right channel data is on SDATA when L/R is low. The rising edge of L/R clocks out the MSB of the left channel data. The falling edge of L/R clocks out the MSB of the right channel data.

**PD - Analog Power Down, PIN 8**

Device power-down command. The analog and digital circuitry are in power-down mode when PD is logic high.

**CMODE - Clock Mode Select, PIN 9**

CMODE should be tied low to select an MCLK frequency of 256 X the output word rate. CMODE should be tied high to select an MCLK frequency of 384 X the output word rate.

**SMODE - Serial Interface Mode Select, PIN 19**

SMODE must be tied high to select serial interface Mode 1. SMODE must be tied low to select serial interface Mode 2. In all interface modes, L/R, FSYNC and SCLK should be derived from MCLK using external dividers.

**FSYNC - Frame Synchronization Signal, PIN 18**

In Mode 1 (SMODE high), FSYNC is ignored but must be connected to VD+ or DGND.

In Mode 2 (SMODE low), FSYNC is an input which controls the output of data on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/R transitions. If it is desired to delay the data bits from the L/R edge, then FSYNC must be low during the delay period. Bringing FSYNC high will enable SCLK to clock out of the SDATA bits. Note that the MSB will be clocked out based on the L/R edge, independent of the state of FSYNC.

*Digital Outputs*

**SDATA - Serial Data Output, PIN 13**

Audio data bits are presented MSB first, in 2's complement format.

*Miscellaneous*

**NC - No Connection, PINS 1, 2, 3, 26, 27, 28**

No internal connection.

**TSTO1, TSTO2 -Test Pins, PIN 20, 21**

These pins are factory test outputs and must not be connected to any external component or length of PC trace.

**TST - Test Input, PIN 17**

Allows access to the CS5345 test modes. Must be connected to digital ground for normal operation.

## PARAMETER DEFINITIONS

**Resolution** - The total number of possible output codes is equal to $2^N$, where N = the number of bits in the output word for each channel.

**Dynamic Range** - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

**Total Harmonic Distortion+Noise** - The ratio of the rms sum of all spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), excluding signal, to the rms value of the signal.

**Total Harmonic Distortion** - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal.

**Interchannel Phase Deviation** - The difference between the left and right channel sampling times.

**Interchannel Isolation** - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

**Interchannel Gain Mismatch** - The gain difference between left and right channels. Units in decibels.



**Gain Error** - The deviation of the measured full scale amplitude from the ideal full scale amplitude value.

**Gain Drift** - The change in gain value with temperature. Units in ppm/°C.

**Bipolar Offset Error** - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal . Units in LSBs.

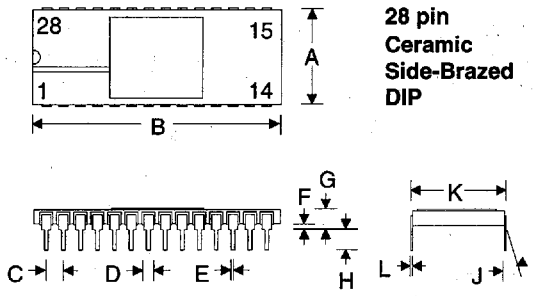
**REFERENCES - All reprinted in this data book.**

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

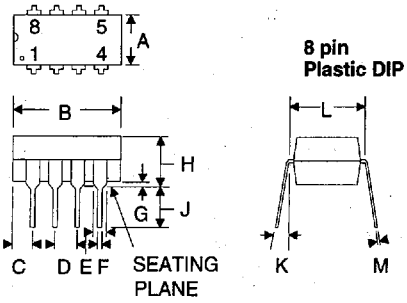
3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

## MECHANICAL DATA




**28 pin Ceramic Side-Brazed DIP**

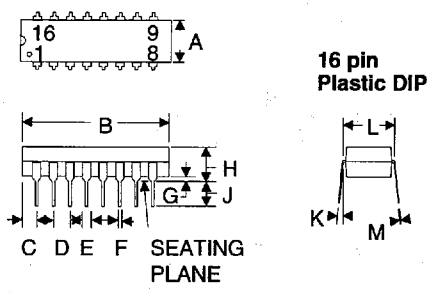
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 14.73 | 15.34 | 0.580 | 0.604 |
| B | 35.20 | 35.92 | 1.386 | 1.414 |
| C | 2.54 BSC | | 0.100 BSC | |
| D | 0.76 | 1.40 | 0.030 | 0.055 |
| E | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.79 | 4.32 | 0.110 | 0.170 |
| H | 2.54 | 4.57 | 0.100 | 0.180 |
| J | - | 10° | - | 10° |
| K | 14.99 | 15.49 | 0.590 | 0.610 |
| L | 0.20 | 0.30 | 0.008 | 0.012 |




**8 pin Plastic DIP**

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 6.10 | 6.60 | 0.240 | 0.260 |
| B | 9.14 | 10.2 | 0.360 | 0.400 |
| C | 0.38 | 1.52 | 0.015 | 0.060 |
| D | 2.54 BSC | | 0.100 BSC | |
| E | 1.02 | 1.78 | 0.040 | 0.070 |
| F | 0.38 | 0.53 | 0.015 | 0.021 |
| G | 0.51 | 1.02 | 0.020 | 0.040 |
| H | 3.81 | 5.08 | 0.150 | 0.200 |
| J | 2.92 | 3.43 | 0.115 | 0.135 |
| K | 0° | 10° | 0° | 10° |
| L | 7.62BSC | | 0.300BSC | |
| M | 0.20 | 0.38 | 0.008 | 0.015 |

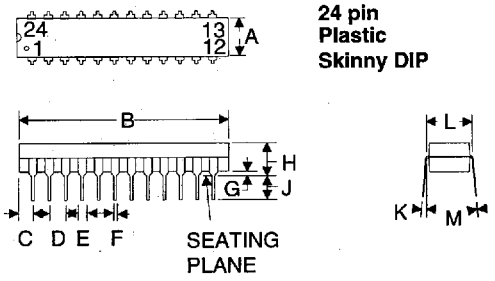
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.




**16 pin Plastic DIP**

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 6.10 | 6.60 | 0.240 | 0.260 |
| B | 18.80 | 19.30 | 0.740 | 0.760 |
| C | 1.32 | 2.89 | 0.015 | 0.035 |
| D | 2.54 BSC | | 0.100 BSC | |
| E | 1.02 | 1.78 | 0.040 | 0.070 |
| F | 0.38 | 0.53 | 0.015 | 0.021 |
| G | 0.51 | 1.02 | 0.020 | 0.040 |
| H | 3.81 | 5.08 | 0.150 | 0.200 |
| J | 2.92 | 3.43 | 0.115 | 0.135 |
| K | 0° | 10° | 0° | 10° |
| L | 7.62BSC | | 0.300BSC | |
| M | 0.20 | 0.38 | 0.008 | 0.015 |

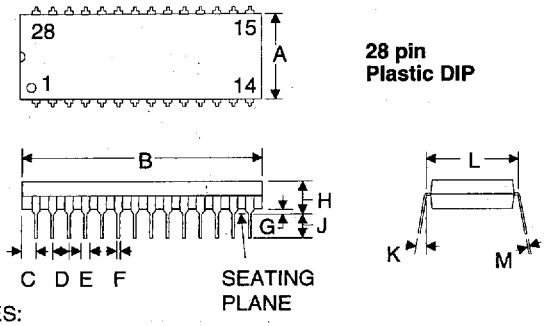
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.




**24 pin**
**Plastic**
**Skinny DIP**

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 6.10 | 6.60 | 0.240 | 0.260 |
| B | 31.37 | 32.13 | 1.235 | 1.265 |
| C | 1.65 | 2.16 | 0.065 | 0.085 |
| D | 2.54 BSC | | 0.100 BSC | |
| E | 1.02 | 1.52 | 0.040 | 0.060 |
| F | 0.36 | 0.56 | 0.014 | 0.022 |
| G | 0.51 | 1.02 | 0.020 | 0.040 |
| H | 3.94 | 4.57 | 0.155 | 0.180 |
| J | 2.92 | 3.43 | 0.115 | 0.135 |
| K | 0° | 15° | 0° | 15° |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0.20 | 0.38 | 0.008 | 0.015 |

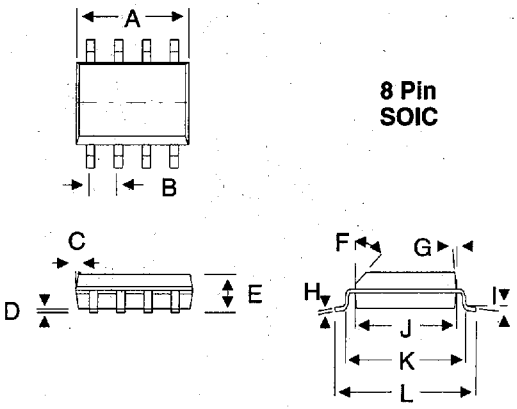
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.




**28 pin**
**Plastic DIP**

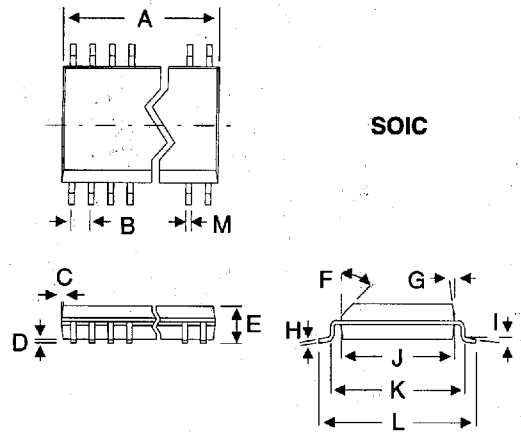
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 13.72 | 14.22 | 0.540 | 0.560 |
| B | 36.45 | 37.21 | 1.435 | 1.465 |
| C | 1.65 | 2.16 | 0.065 | 0.085 |
| D | 2.54 BSC | | 0.100 BSC | |
| E | 1.02 | 1.52 | 0.040 | 0.060 |
| F | 0.36 | 0.56 | 0.014 | 0.022 |
| G | 0.51 | 1.02 | 0.020 | 0.040 |
| H | 3.94 | 5.08 | 0.155 | 0.200 |
| J | 2.92 | 3.43 | 0.115 | 0.135 |
| K | 0° | 15° | 0° | 15° |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0.20 | 0.38 | 0.008 | 0.015 |

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.




8 Pin
SOIC

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 5.25 | 5.30 | 0.207 | 0.209 |
| B | 1.27 TYP | | 0.050 TYP | |
| C | 7° NOM | | 7° NOM | |
| D | 0.120 | 0.180 | 0.005 | 0.007 |
| E | 1.80 | 1.86 | 0.071 | 0.073 |
| F | 45° NOM | | 45° NOM | |
| G | 7° NOM | | 7° NOM | |
| H | 0.195 | 0.205 | 0.0078 | 0.0082 |
| I | 2° | 4° | 2° | 4° |
| J | - | - | - | - |
| K | 6.57 | 6.63 | 0.259 | 0.261 |
| L | 7.85 | 7.95 | 0.308 | 0.312 |

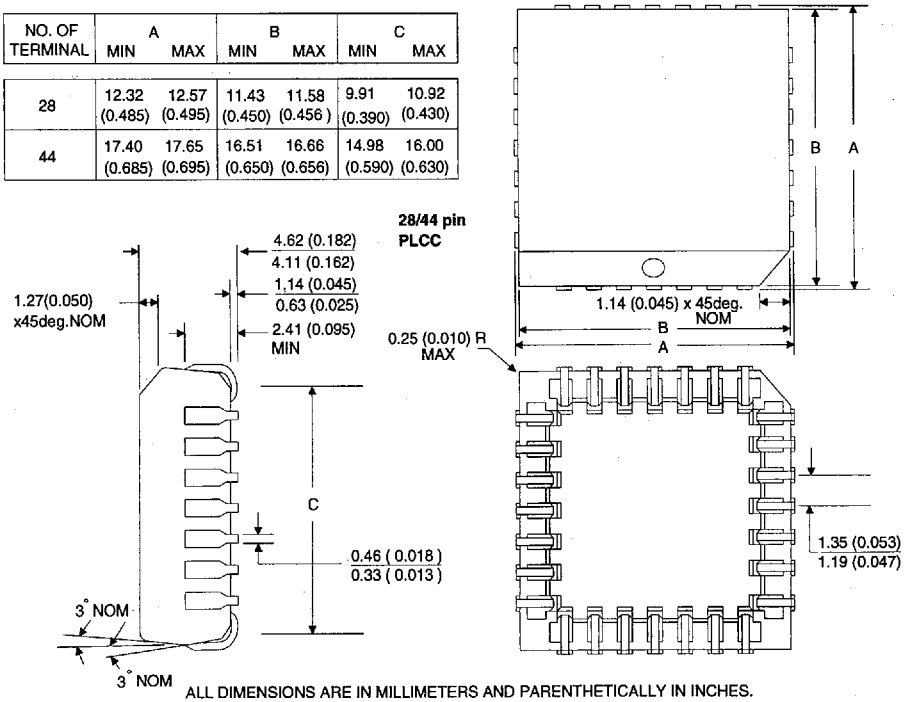



SOIC

| pins | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 16 | 9.91 | 10.41 | 0.390 | 0.410 |
| 20 | 12.45 | 12.95 | 0.490 | 0.510 |
| 24 | 14.99 | 15.50 | 0.590 | 0.610 |
| 28 | 17.53 | 18.03 | 0.690 | 0.710 |

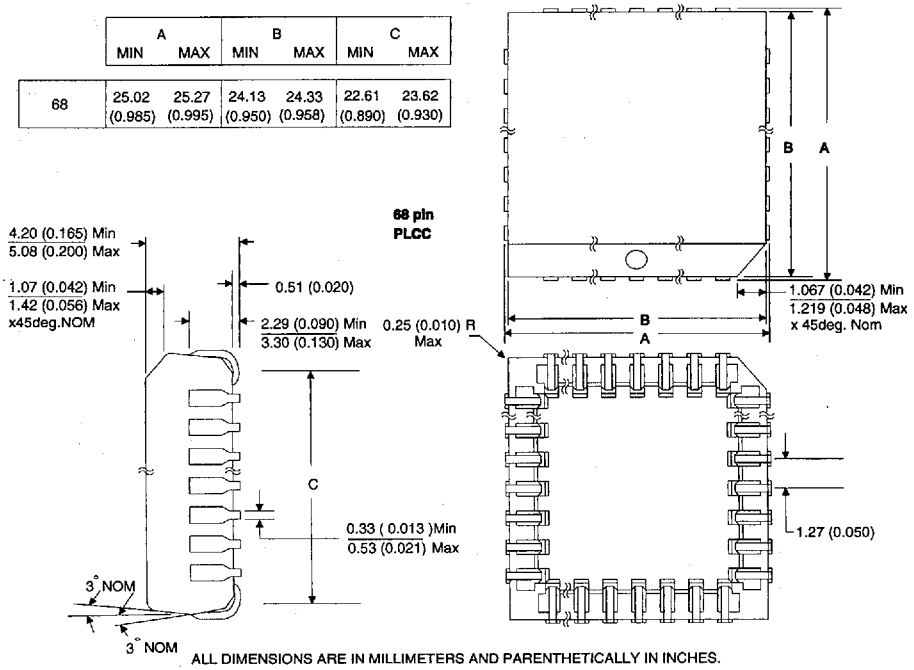
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | see table above | | | |
| B | 1.27 | BSC | 0.050 | BSC |
| C | 7° | NOM | 7° | NOM |
| D | 0.127 | 0.330 | 0.005 | 0.013 |
| E | 2.41 | 2.67 | 0.095 | 0.105 |
| F | 45° | NOM | 45° | NOM |
| G | 7° | NOM | 7° | NOM |
| H | 0.203 | 0.381 | 0.008 | 0.015 |
| I | 2° | 8° | 2° | 8° |
| J | 7.42 | 7.59 | 0.292 | 0.298 |
| K | 8.76 | 9.02 | 0.345 | 0.355 |
| L | 10.16 | 10.67 | 0.400 | 0.420 |
| M | 0.33 | 0.51 | 0.013 | 0.020 |

| NO. OF TERMINAL | A MIN | A MAX | B MIN | B MAX | C MIN | C MAX |
|---|---|---|---|---|---|---|
| 28 | 12.32 (0.485) | 12.57 (0.495) | 11.43 (0.450) | 11.58 (0.456) | 9.91 (0.390) | 10.92 (0.430) |
| 44 | 17.40 (0.685) | 17.65 (0.695) | 16.51 (0.650) | 16.66 (0.656) | 14.98 (0.590) | 16.00 (0.630) |




ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

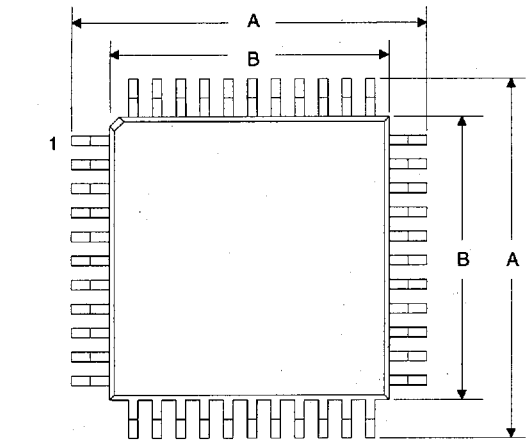
| | A MIN | A MAX | B MIN | B MAX | C MIN | C MAX |
|---|---|---|---|---|---|---|
| 68 | 25.02 (0.985) | 25.27 (0.995) | 24.13 (0.950) | 24.33 (0.958) | 22.61 (0.890) | 23.62 (0.930) |



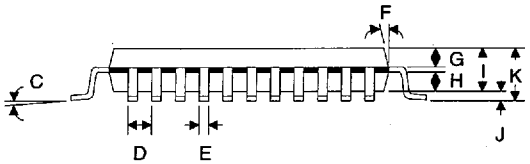

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

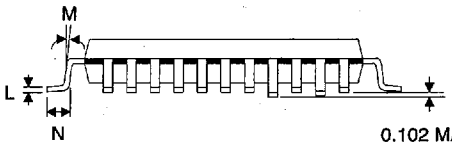
11

## 44 PIN QUAD FLATPACK

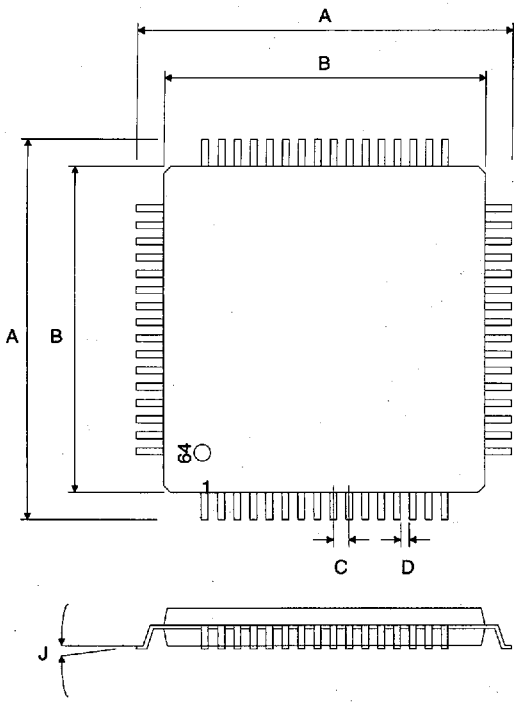


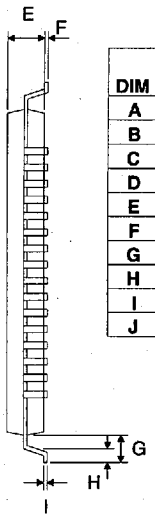

| | 44 Pin TQFP 1.4 mm Package Thickness | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| DIM | MIN | MAX | MIN | MAX |
| A | 11.75 | 12.25 | 0.463 | 0.482 |
| B | 9.90 | 10.10 | 0.390 | 0.398 |
| C | 0° | 7° | 0° | 7° |
| D | 0.80 BSC | | 0.031 BSC | |
| E | 0.35 BSC | | 0.014 BSC | |
| F | | 12° | | 12° |
| G | 0.54 | 0.74 | 0.021 | 0.029 |
| H | 0.54 | 0.74 | 0.021 | 0.029 |
| I | 1.35 | 1.50 | 0.053 | 0.059 |
| J | 0.05 | | 0.002 | |
| K | | 1.60 | | 0.063 |
| L | | 0.17 | | 0.007 |
| M | 2° | 10° | 2° | 10° |
| N | 0.35 | 0.65 | 0.014 | 0.026 |



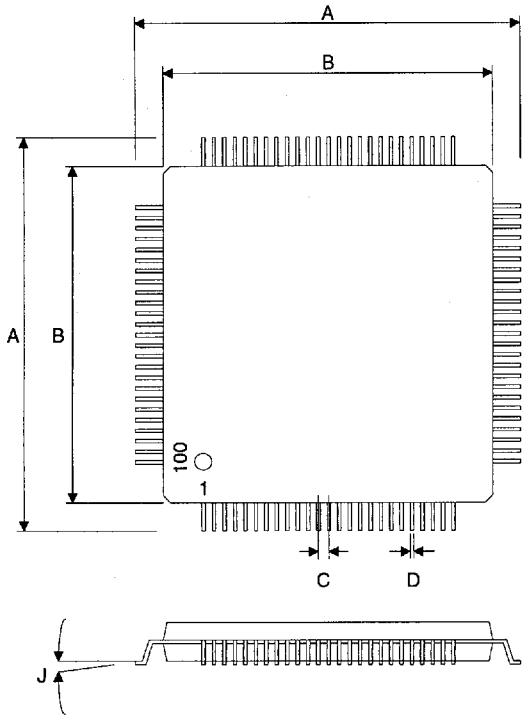

0.102 MAX
Lead Coplanarity

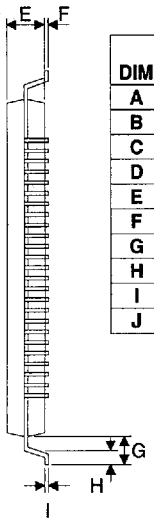



64 Pin TQFP

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 12.00 BSC | | 0.472 BSC | |
| B | 10.00 BSC | | 0.393 BSC | |
| C | 0.50 BSC | | 0.020 BSC | |
| D | 0.14 | 0.30 | 0.005 | 0.012 |
| E | 0.95 | 1.12 | 0.037 | 0.044 |
| F | 0.05 | 0.15 | 0.002 | 0.006 |
| G | 1.00 BSC | | 0.039 BSC | |
| H | 0.45 | 0.75 | 0.018 | 0.030 |
| I | 0.09 | 0.18 | 0.003 | 0.007 |
| J | 0° | 7° | 0° | 7° |




**100-pin TQFP**

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 15.75 | 16.25 | 0.620 | 0.640 |
| B | 13.90 | 14.10 | 0.547 | 0.555 |
| C | 0.50 BSC | | 0.020 BSC | |
| D | 0.10 | 0.20 | 0.004 | 0.012 |
| E | 1.25 | 1.55 | 0.049 | 0.061 |
| F | 0.00 | 0.20 | 0.000 | 0.008 |
| G | 1.00 BSC | | 0.039 BSC | |
| H | 0.35 | 0.65 | 0.014 | 0.026 |
| I | 0.077 | 0.177 | 0.003 | 0.007 |
| J | 0° | 10° | 0° | 10° |

11