Semiconductor Corporation

CS5390

20-Bit, Stereo A/D Converter for Digital Audio

Features

- 110 dB Dynamic Range (A-Weighted)
- THD + N better than -100dB
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - >100dB StopBand Attenuation
  - 0.005dB Passband Ripple
- Low Power Dissipation: 550 mW
  - Power-Down Mode
- Pin Compatible with CS5389
- Evaluation Board Available

General Description

The CS5390 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 20-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

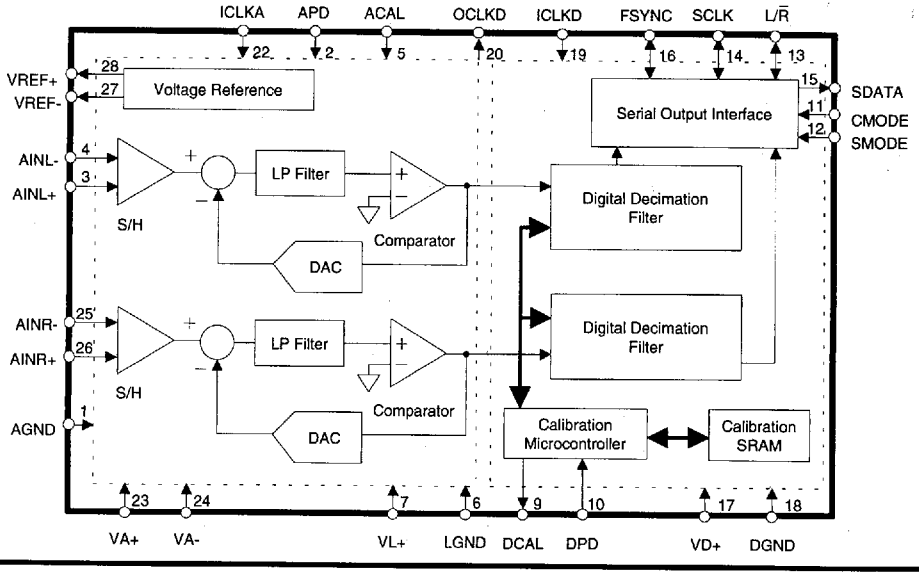
The CS5390 uses 5th-order, delta-sigma modulation with 64X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5390 has a filter passband of dc to 21.7kHz. The filters have linear phase, 0.005 dB passband ripple, and >100 dB stopband rejection.

The CS5390 is targeted for the highest performance professional audio systems requiring wide dynamic range, negligible distortion and low noise. Pin compatibility with the CS5389 allows a simple upgrade path without hardware changes.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS5390-KP	0° to 70°C	28-pin Plastic DIP



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VL+,VD+ = 5V; VA- = -5V; Full-scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 39Ω with 6.8 nF across AIN+, AIN-; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = VD+;

Parameter	Symbol	Min	CS5390-K Typ	Max	Units
Resolution		20	-	-	Bits
Dynamic Performance					
Dynamic Range		TBD	107	-	dB
(A-weighted)		-	110	-	dB
Total Harmonic Distortion + Noise	THD+N				
0 dB		-	-100	-	dB
-20 dB		-	-87	TBD	dB
-60 dB		-	-47	TBD	dB
Interchannel Phase Deviation		-	0.0001	-	°
Interchannel Isolation		106	120	-	dB
dc Accuracy					
Interchannel Gain Mismatch		-	0.05	-	dB
Gain Error		-	±1	±5	%
Gain Drift		-	50	150	ppm/°C
Bipolar Offset Error (After Calibration)		-	±5	±20	LSB
Offset Calibration Range		-	±50	-	mV
Analog Input					
Full-scale Differential Input Voltage (Note 1)	V_{IN}	14.0	14.72	-	Vpp
Input Impedance	Z_{IN}	-	25	-	kΩ
Common-Mode Rejection	CMRR	-	115	-	dB
Power Supplies					
Power Supply Current (VA+)+(VL+)	I_{A+}	-	37.5	55	mA
with APD, DPD low VA-	I_{A-}	-	37.5	55	mA
(Normal Operation) VD+	I_{D+}	-	35.0	TBD	mA
Power Supply Current (VA+)+(VL+)	I_{A+}	-	100	-	µA
with APD, DPD high VA-	I_{A-}	-	100	-	µA
(Power-Down Mode) VD+	I_{D+}	-	100	-	µA
Power Consumption (APD, DPD Low)	PDN	-	550	TBD	mW
(APD, DPD High)	PDS	-	1.5	-	mW
Power Supply (dc to 29 kHz)	PSRR	-	65	-	dB
Rejection Ratio (29 kHz to 3.046 MHz)		-	90	-	dB

Notes: 1. Specified for a fully differential input ±{(AINR+)-(AINR-)}.The ADC accepts input voltages up to the analog supplies (VA+, VA-). Full-scale outputs will be produced for differential inputs beyond V_{IN}. This value is subject to the gain error tolerance specification

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%; Output word rate of 48 kHz)

Parameter		Symbol	Min	Typ	Max	Units
Passband	(-0.005 dB)		0	-	21.7	kHz
Passband Ripple			-	-	±0.005	dB
Stopband			29	-	3043	kHz
Stopband Attenuation	(Note 2)		100		-	dB
Group Delay (OWR = Output Word Rate)		t_{gd}	-	18/OWR	-	s
Group Delay Variation vs Frequency		Δt_{gd}	-	-	0.0	µs

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are (n x 3.072MHz) ±21.7kHz, where n = 0,1,2,3...

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30%VD+	V
High-Level Output Voltage at I_O = -20 µA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at I_O = 20 µA	V_{OL}	-	-	0.1	V
Input Leakage Current	I_{in}	-	1.0	-	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	-	+6.0	V
	Negative Analog	VA-	+0.3	-	-6.0	V
	Positive Logic	VL+	-0.3	-	+6.0	V
	Positive Digital	VD+	-0.3	-	+6.0	V
	|VA+ - VD+|		-	-	0.4	V
	|VA+ - VL+|		-	-	0.4	V
	|VD+ - VL+|		-	-	0.4	V
Input Current	Any Pin Except Supplies	I_{in}	-	-	±10	mA
Peak Analog Input Voltage (AINL+/- and AINR +/- pins)		V_{IN}	(VA-)-0.4	-	(VA+)+0.4	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+)+0.4	V
Ambient Operating Temperature (Power Applied)		T_A	-55	-	+125	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

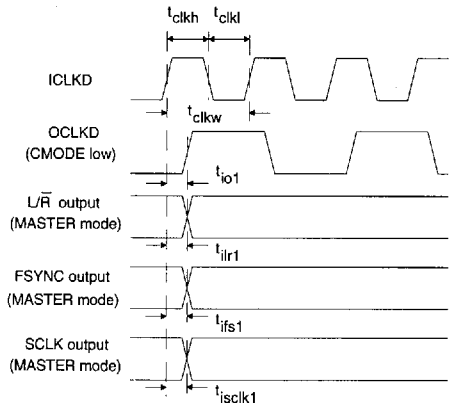
WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

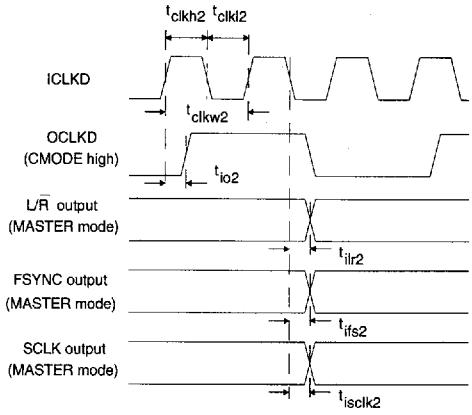
(T_A = 25 °C; VA+, VL+, VD+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low)	t_{clkw1}	78	-	390.6	ns
ICLKD Low (CMODE low)	t_{clkl1}	31	-	-	ns
ICLKD High (CMODE low)	t_{clkh1}	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t_{io1}	5	-	40	ns
ICLKD Period (CMODE high)	t_{clkw2}	52	-	260.4	ns
ICLKD Low (CMODE high)	t_{clkl2}	20	-	-	ns
ICLKD High (CMODE high)	t_{clkh2}	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 3)	t_{io2}	5	-	45	ns
ICLKD rising to L/$\overline{R}$ edge (CMODE low, MASTER mode)	t_{ilr1}	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t_{ifs1}	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t_{isclk1}	5	-	50	ns
ICLKD falling to L/$\overline{R}$ edge (CMODE high, MASTER mode)	t_{ilr2}	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t_{ifs2}	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t_{isclk2}	5	-	50	ns
SCLK falling to SDATA valid (MASTER mode)	t_{sdo}	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK falling to L/$\overline{R}$ (MASTER mode)	t_{mslr}	-20	-	20	ns
SCLK falling to FSYNC (MASTER mode)	t_{msfs}	-20	-	20	ns
SCLK Period (SLAVE mode)	t_{sclkw}	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t_{sclkh}	60	-	-	ns
SCLK falling to SDATA valid (SLAVE mode)	t_{dss}	-	-	50	ns
L/$\overline{R}$ edge to MSB valid (SLAVE mode)	t_{lrdss}	-	-	50	ns
Rising SCLK to L/$\overline{R}$ edge delay (SLAVE mode)	t_{slr1}	30	-	-	ns
L/$\overline{R}$ edge to rising SCLK setup time (SLAVE mode)	t_{slr2}	30	-	-	ns
Rising SCLK to rising FSYNC delay (SLAVE mode)	t_{sfs1}	30	-	-	ns
Rising FSYNC to rising SCLK setup time (SLAVE mode)	t_{sfs2}	30	-	-	ns
DPD pulse width	t_{pdw}	2 x t_{clkw}	-	-	ns
DPD rising to DCAL rising	t_{pcr}	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t_{pcf}		4096		1/OWR

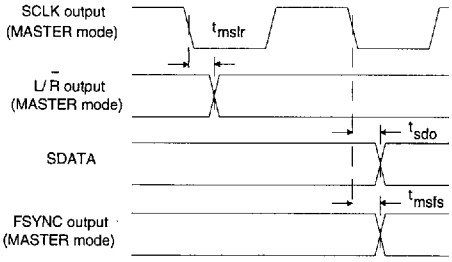
Notes: 3. ICLKD rising or falling depends on DPD to L/$\overline{R}$ timing (see Figure 2).



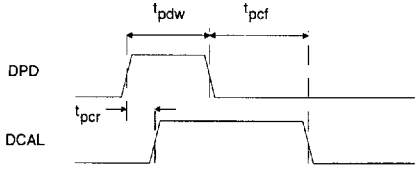
ICLKD to Outputs Propagation Delays (CMODE low)



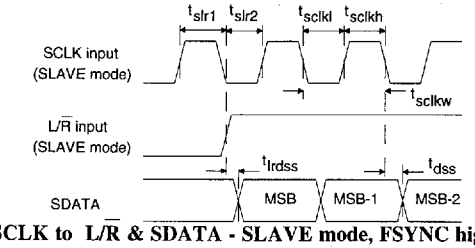
ICLKD to Outputs Propagation Delays (CMODE high)



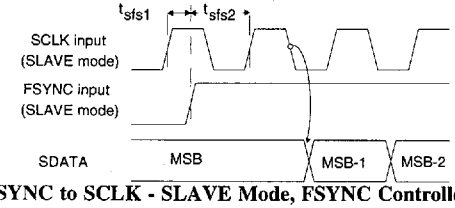
SCLK to SDATA, L/R & FSYNC - MASTER Mode



Power Down & Calibration Timing



SCLK to L/R & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Logic	VL+	4.75	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	-4.75	-5.0	-5.25	V
	IVA+ - VD+I	-	-	-	0.4	V

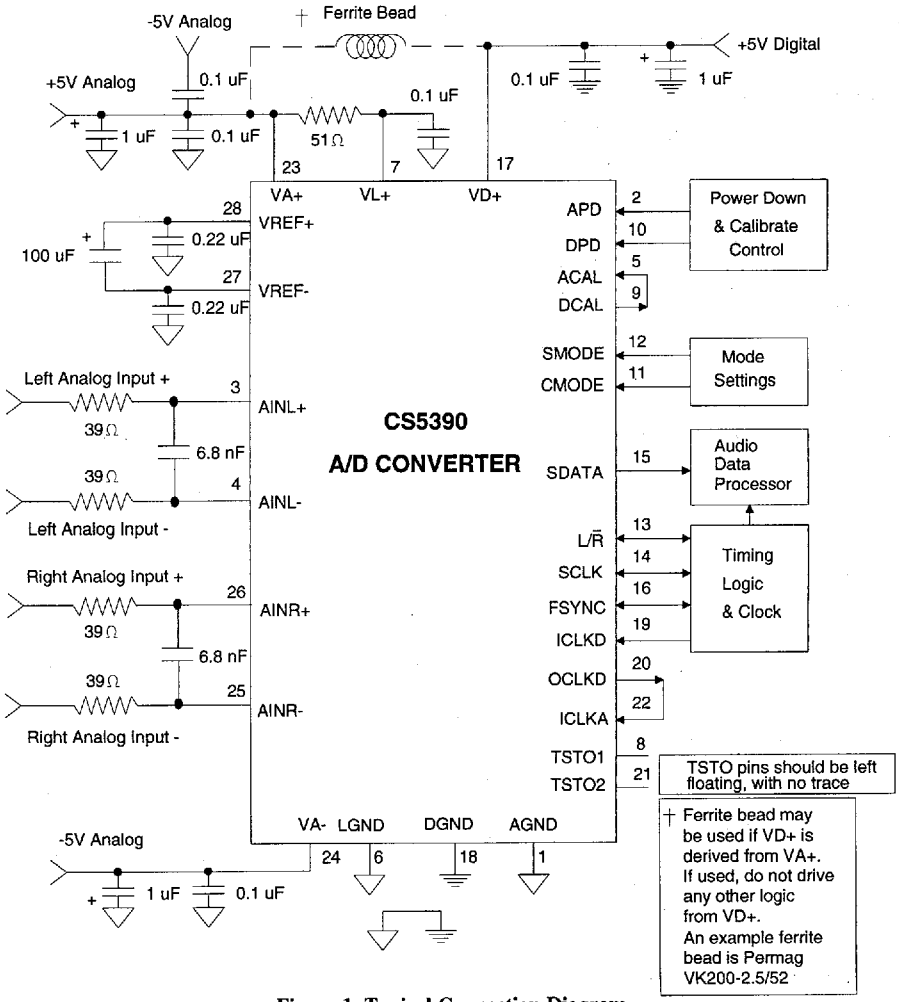


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5390 is a 20-bit, stereo A/D converter designed specifically for stereo digital audio applications. The device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 20-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters and it does not require external sample-and-hold amplifiers or voltage references.

On-chip voltage references provide for a differential input signal range of 14.72 Vpp. Any offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 20-bit numbers. Typical power consumption of only 550 mW can be further reduced by use of the power-down mode.

The CS5390 is pin compatible with the CS5389, and it offers wider dynamic range and twenty bit resolution. The pin compatibility of the CS5390 provides a simple upgrade path to systems currently using the CS5389.

For more information on delta-sigma modulation techniques see the references at the end of this data sheet.

SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

3

Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter and is used to generate the modulator sampling clock. The required ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the ICLKD frequency to 384 X OWR, while CMODE low will set the ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR. OCLKD should be connected to ICLKA, which controls the input sample rate.

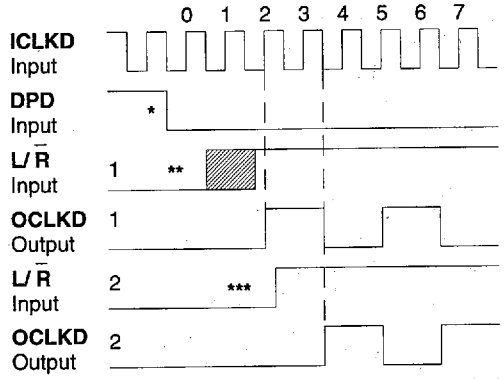
The phase alignment between ICLKD and OCLKD is determined as follows: when CMODE is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase

$L/\overline{R}$ (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and L/$\overline{R}$, shown in Figure 2.

Serial Data Interface



* DPD low is recognized on the next ICLKD rising edge (#0)
** L/$\overline{R}$ rising before ICLKD rising #2 causes OCLKD -1
*** L/$\overline{R}$ rising after ICLKD rising #2 causes OCLKD - 2

Figure 2. ICLKD to OCLKD Timing with CMODE high (384XOWR)

MASTER mode and SLAVE mode are the 2 primary modes of operation for the serial data output interface.

Master Mode

SCLK, L/$\overline{R}$ and FSYNC are outputs derived from ICLKD in Master mode, Figure 3. Notice the one SCLK cycle delay between L/$\overline{R}$ edges, SDATA and FSYNC. FSYNC brackets the 16 most significant data bits.

Slave Mode

L/$\overline{R}$, FSYNC and SCLK become inputs in SLAVE mode. L/$\overline{R}$ must be externally derived from ICLKD and be equal to the Output Word Rate. SCLK should be equal to 64 X OWR though other frequencies are possible but may degrade system performance due to interference effects. FSYNC may be high or used to control SDATA. With FSYNC high, data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The falling edge of SCLK causes the ADC to output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge, as shown in Figure 4.

SCLK is ignored with FSYNC low and only the MSB is clocked out after the L/$\overline{R}$ edge in SLAVE mode / FSYNC controlled as shown in Figure 5. Bringing FSYNC high will enable SCLK to clock data out. This feature is particularly useful to multiplex multiple channels.

Certain serial modes align well with various interface requirements. A CS5390 in MASTER mode, with an inverted L/$\overline{R}$ signal, generates I^2S (Philips) compatible timing. A CS5390 (with an inverted SCLK) in SLAVE mode emulates a CS5326 style interface and also links to a DSP56000 in network mode.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+, AINR- and AINL+, AINL- pins. Each analog input will accept a maximum of 7.36 Vpp. The + and - input signals are 180° out of phase resulting in a differential input voltage of 14.72 Vpp. Figure 6 shows the input signal levels for full scale.

The analog modulator samples the input at 3.072 MHz (64 x Fs) for an output word rate of 48 kHz. The digital filter will reject signals between 21.7 kHz and 3.072 MHz - 21.7 kHz. However, there is no rejection for input signals which are (n x 3.072 MHz) +/- 21.7 kHz, where n = 0,1,2,... A 39 Ω resistor in series with the analog input and a 6.8 nF NPO or COG capacitor between the inputs will attenuate any noise energy

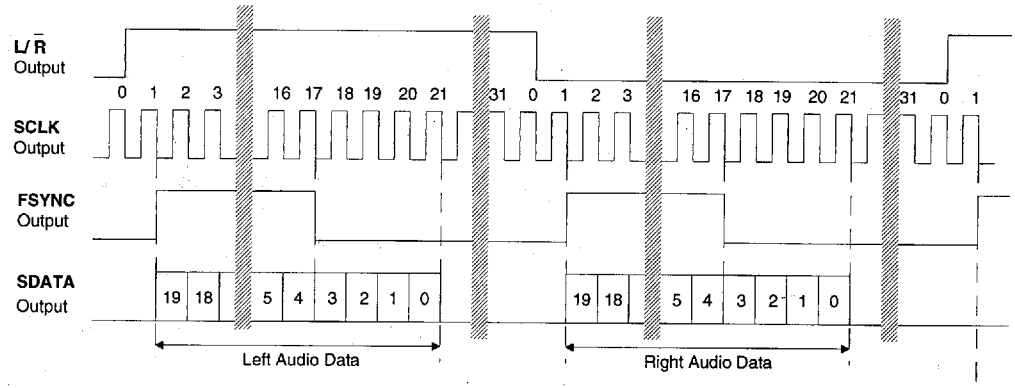


Figure 3. Data Output Timing - MASTER mode

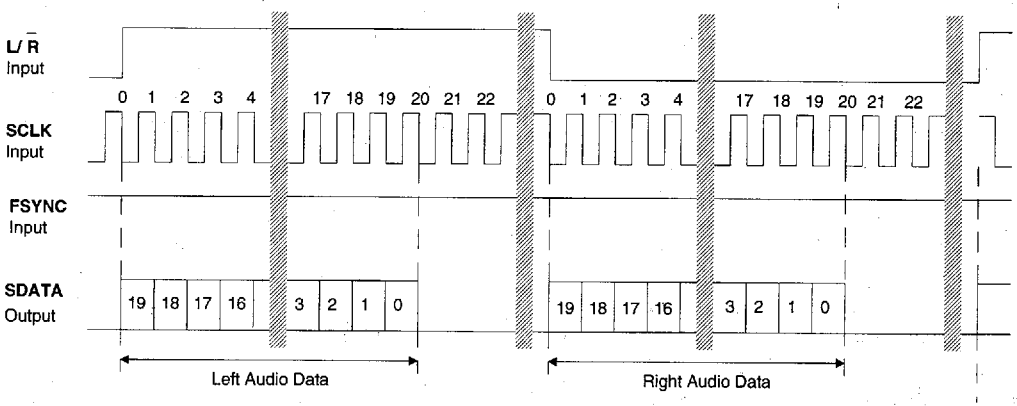
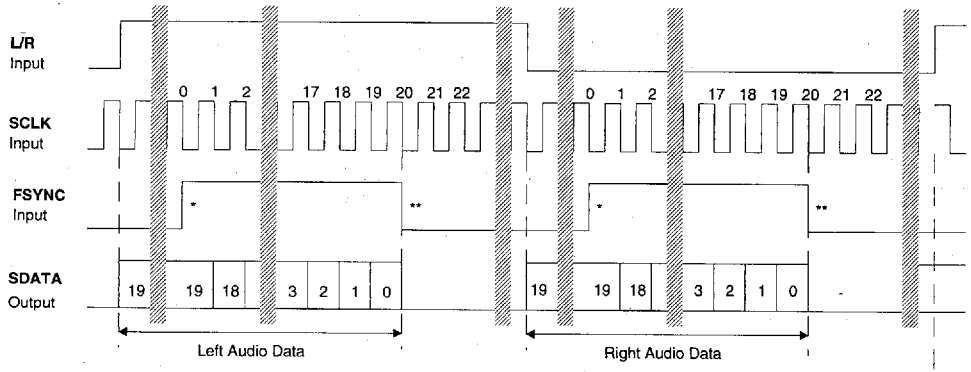


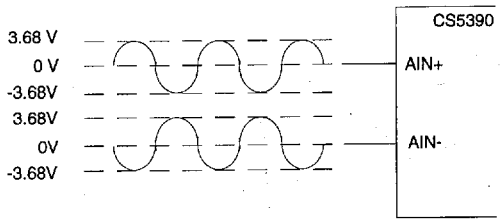
Figure 4. Data Output Timing - SLAVE Mode, FSYNC high



* Rising FSYNC enables SCLK to clock out SDATA

** Falling FSYNC stops SCLK from clocking out SDATA

Figure 5. Data Output Timing - SLAVE Mode, FSYNC controlled



Full Scale Input level= (AIN+) - (AIN-)= 14.72 Vpp

Figure 6. Full Scale Input Voltage

at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

The on-chip voltage references are available at the VREF+ and VREF- pins for the purpose of decoupling only. The circuit traces attached to these pins must be minimal in length and no load current may be taken from VREF+ or VREF-. The recommended decoupling scheme, Figure 1, is a 100 µF electrolytic capacitor across VREF+ and VREF- and two 0.22 µF ceramic capacitors connected from VREF+ to GND and VREF- to GND.

Power-Down and Offset Calibration

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode wherein typical power consumption drops to 1.5 mW.

Bringing DPD low exits power-down and initiates an offset calibration cycle. During the calibration cycle, the digital section measures the offset of each channel and stores a corresponding value in the calibration registers. This value is subtracted from future conversions to produce an offset free conversion. The calibration inputs are obtained from the analog input pins (ACAL low) or AGND (ACAL high).

The offsets generated by the input circuitry are included when calibration is performed using the analog input pins (ACAL low). DCAL should be used to control a multiplexer which grounds the user's front-end in this mode. The DCAL output will remain high for 4096 L/$\overline{R}$ clock cycles during calibration as shown in Figure 7.

A delay of approximately 50 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-

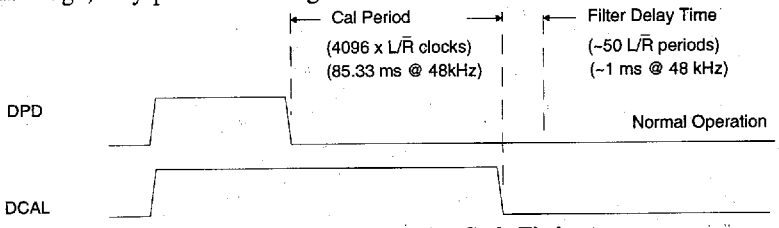


Figure 7. Initial Calibration Cycle Timing

down mode. The voltage reference will take a much longer time to reach a final value due to the presence of external capacitance on the VREF+ and VREF- pins. A time delay of approximately 10 ms/µF is required between APD going low and DPD going low to allow for VREF settling. The typical connection diagram of Figure 1 requires a 1 second delay.

APD should be tied to AGND if the analog power down feature is not required. When using the analog power down feature, DPD and APD may be tied together if the capacitor across VREF+ and VREF- is not greater than 10 µF.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+, VA- and VL+ connected to a clean ± 5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF+ and VREF- pins in order to avoid unwanted coupling into the modulators. The VREF+ and VREF- decoupling capacitors, particularly the 0.22 µF, must be positioned to minimize the electrical path from VREF+ and VREF- to Pin 1, AGND. The CDB5390 evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Additional printed circuit board design and circuit design hints are included in the application note, "Layout and Design Rules for Data Converters" and the Audio Engineering Society paper "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" which are included in the Crystal Semiconductor data book application section.

Synchronization of Multiple CS5390

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

SLAVE MODE

Synchronous sampling in the slave mode is achieved by connecting all DPD pins to a single control signal and supplying the same ICLKD and $L/\overline{R}$ to all converters.

MASTER MODE

The internal counters of the CS5390 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD pins to the same control signal and insuring that the DPD falling edge occurs outside a ±30 ns window either side of an ICLKD rising edge.

PERFORMANCE

Digital Filter

Figures 8 - 10 show the performance of the digital filter included in the ADC. All plots are normalized to the output word rate, Fs. Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with the output word rate.

Stopband rejection, figure 8, is greater than 100 dB. Figure 9 shows the passband ripple of ± 0.005 dB maximum. Figure 10 is an expanded view of the transition band.

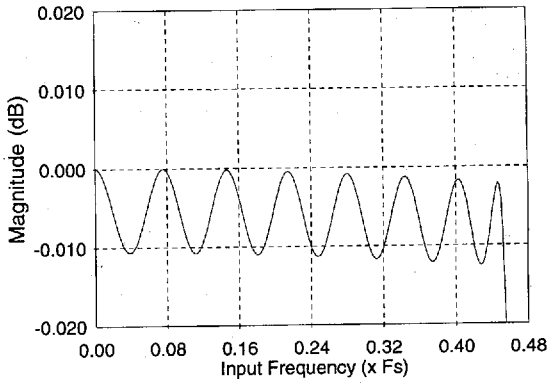


Figure 9. CS5390 Digital Filter Passband Ripple

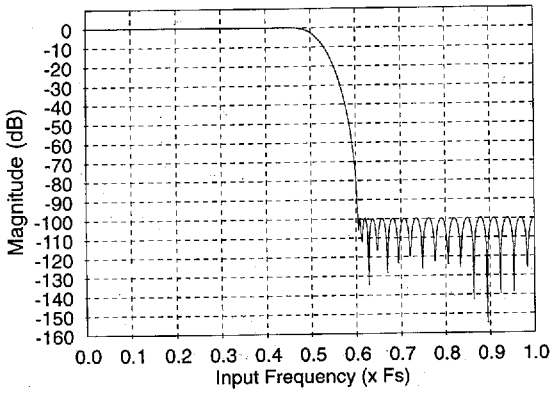


Figure 8. CS5390 Digital Filter Stopband Rejection

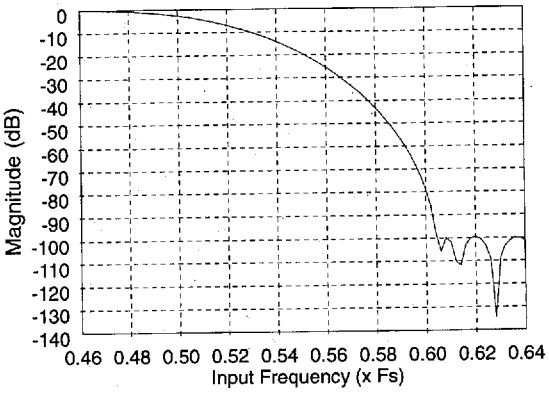
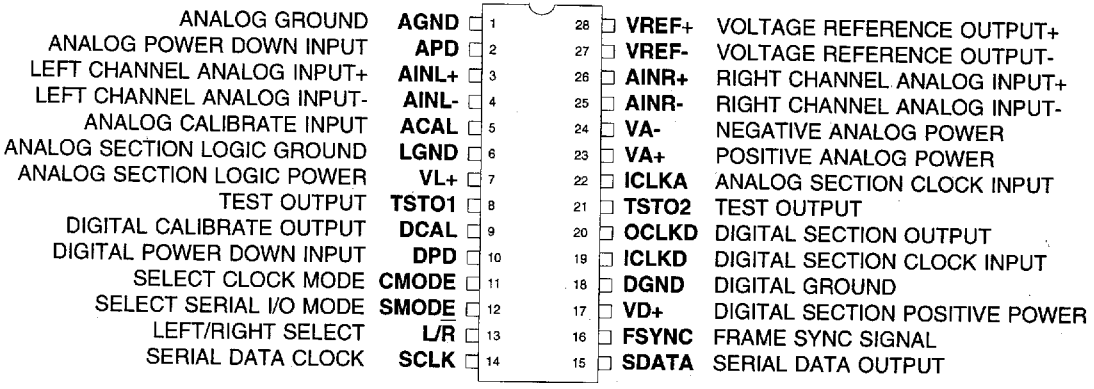


Figure 10. CS5390 Digital Filter Transition Band

PIN DESCRIPTIONS



3

Power Supply Connections

VA+ - Positive Analog Power, PIN 23.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 7.
Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 24.
Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.
Analog ground reference.

LGND - Logic Ground, PIN 6.
Ground for the logic portions of the analog section.

VD+ - Positive Digital Power, PIN 17.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 18.
Digital ground for the digital section.

Analog Inputs

AINR-, AINR+ - Differential Right Channel Analog Inputs, PINS 25, 26.
Analog input connections for the right channel differential inputs. Nominally 14.72 Vpp (differential) full scale.

AINL+, AINL- - Differential Left Channel Analog Inputs, PINS 3,4.

Analog input connections for the right channel differential inputs. Nominally 14.72 Vpp (differential) full scale.

Analog Outputs

VREF-, VREF+ - Voltage Reference Outputs, PINS 27,28.

Nominally +3.68 volts (VREF+) and -3.68 volts (VREF-) volts. Note the negative output polarity on VREF-. See Figure 1 for recommended capacitive decoupling.

Digital Inputs

ICLKA - Analog Section Input Clock, PIN 22.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

ICLKD - Digital Section Input Clock, PIN 19.

ICLKD clocks the digital filter and is the source for modulator sampling clock, OCKLD. The required ICLKD frequency is determined by the desired output word rate and the CMODE pin. If CMODE is low, ICLKD is 256 X the desired output word rate. If CMODE is high, ICLKD is 384 X the output word rate. For example, with CMODE low, ICLKD is 12.288 MHz for an output word rate of 48 kHz.

APD - Analog Power Down, PIN 2.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. APD should be connected to AGND if analog power-down is not used.

DPD - Digital Power Down, PIN 10.

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 $L/\overline{R}$ periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 5.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to AGND respectively. Should be connected to DCAL.

CMODE - Clock Mode Select, PIN 11.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 12.

SMODE should be tied high to select the serial interface master mode. SCLK, FSYNC and L/$\overline{R}$ are outputs generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/$\overline{R}$ are all inputs. In slave mode, L/$\overline{R}$, FSYNC and SCLK need to be derived from ICLKD using external dividers.

Digital Outputs

3

SDATA - Serial Data Output, PIN 15.

Audio data bits are presented MSB first, in 2's complement format.

DCAL - Digital Calibrate Output, PIN 9.

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/$\overline{R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

OCLKD - Digital Section Output Clock, PIN 20.

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

Digital Inputs or Outputs

SCLK - Serial Data Clock, PIN 14.

Data is clocked out on the falling edge of SCLK.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a continuously supplied clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/$\overline{R}$ changes.

L/$\overline{R}$ - Left/Right Select, PIN 13.

In master mode (SMODE high), L/$\overline{R}$ is an output whose frequency is at the output word rate. L/$\overline{R}$ edges occur 1 SCLK cycle before FSYNC rises. When L/$\overline{R}$ is high, left channel data is on SDATA, except for the first SCLK cycle. When L/$\overline{R}$ is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/$\overline{R}$ changes.

In slave mode (SMODE low), L/$\overline{R}$ is an input which selects the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. L/$\overline{R}$ frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

FSYNC - Frame Synchronization Signal, PIN 16.

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the sixteenth SDATA audio data bit .

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/$\overline{R}$ transitions. If it is desired to delay the data bits from the L/$\overline{R}$ edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/$\overline{R}$ edge, independent of the state of FSYNC.

Miscellaneous

TSTO1, TSTO2 - Test Output, PINS 8, 21.

These two pins are bonded out for factory test outputs. They must not be connected to any external component or any length of PC trace.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (rms) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Total Harmonic Distortion plus Noise - The ratio of the rms sum of all spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), excluding signal, to the rms value of the signal.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the gain value from the typical number given in the analog specifications table.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. (1/2 LSB below AGND). Units in LSBs.

REFERENCES - All, except 1), are reprinted in this data book.

1) "A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range" by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

3) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

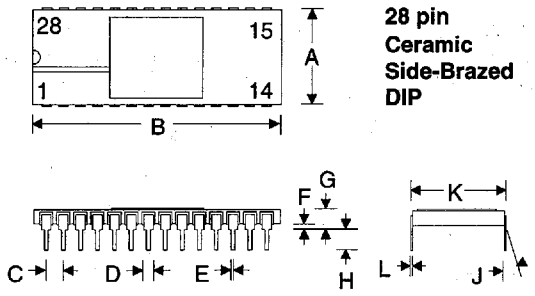
4) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

5) " 18-Bit Stereo D/A Converter with Integrated Digital and Analog Filters" by Nav Sooch ,Jeffery W. Scott, T. Tanaka, T. Sugimoto and C. Kubomura. Presented at the 91st Convention of the Audio Engineering Society, October 1991.

6) " An 18-Bit Delta-Sigma D/A Processor System Achieving Full-Scale THD+N>100dB" by Steven R. Green, Steven Harris and Brent Wilson. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

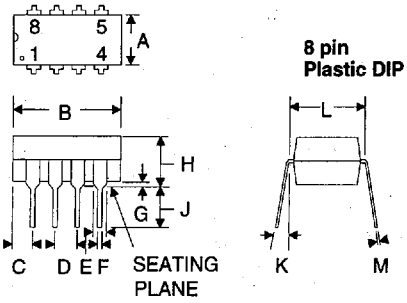
7) " How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters" by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

MECHANICAL DATA



28 pin Ceramic Side-Brazed DIP

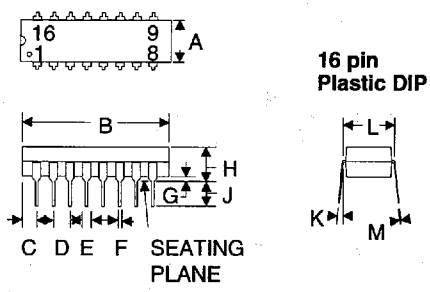
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



8 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

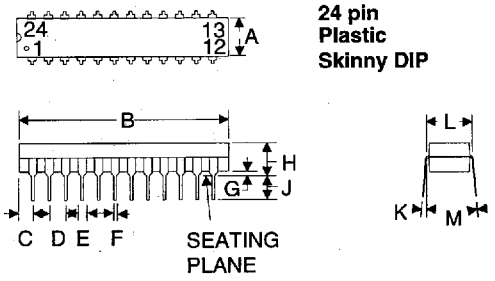
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

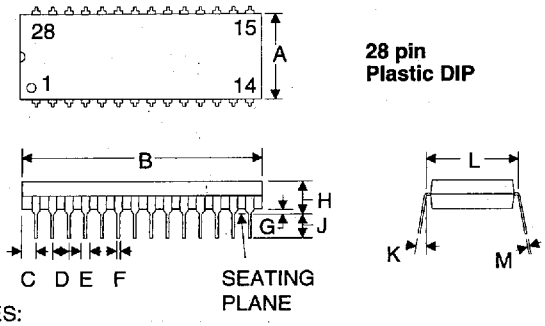
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

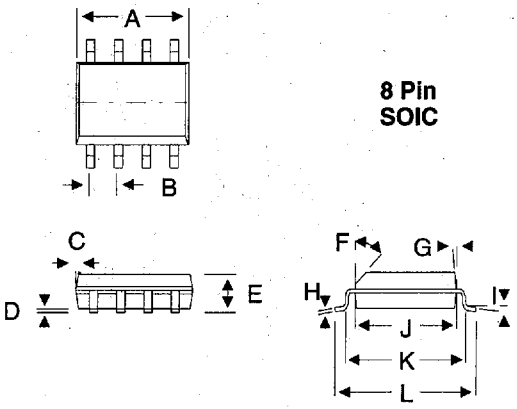
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

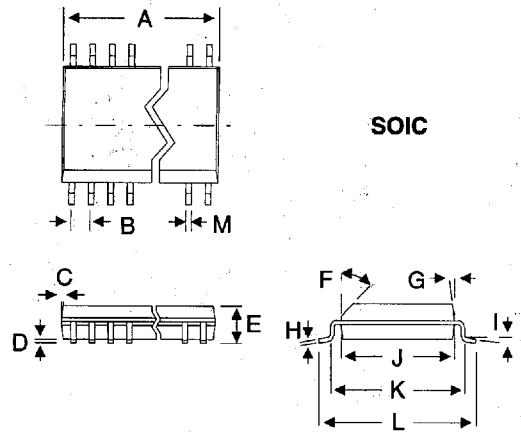
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



8 Pin
SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312

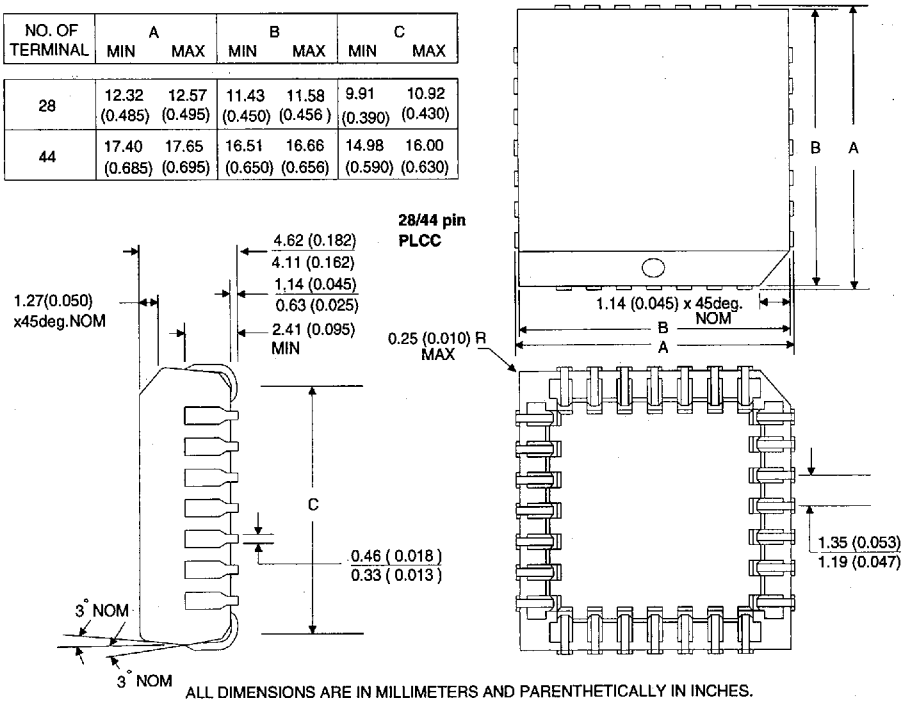


SOIC

pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

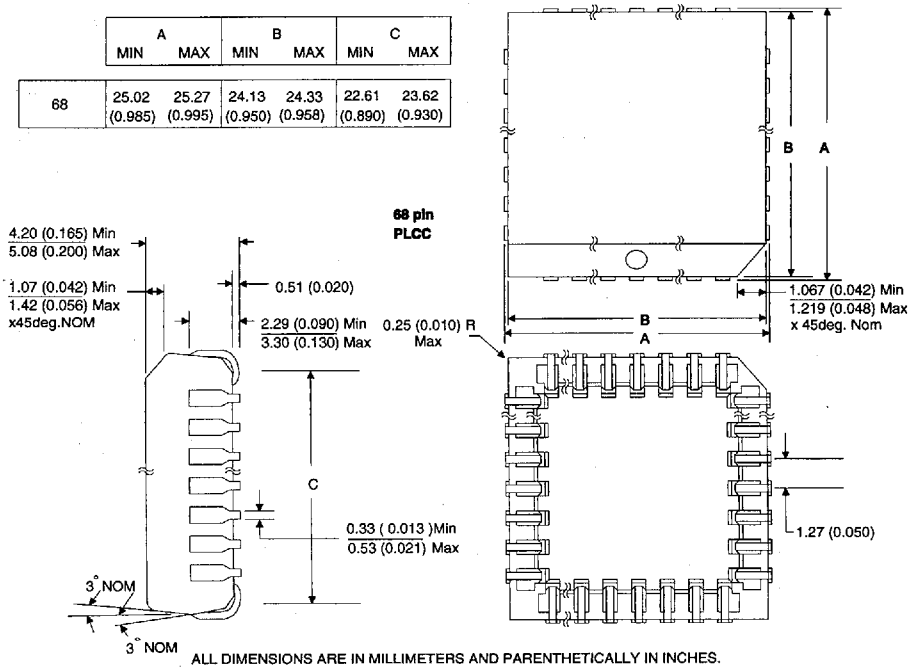
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

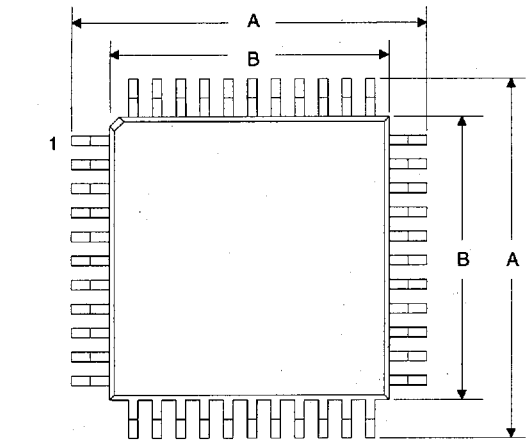
	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)



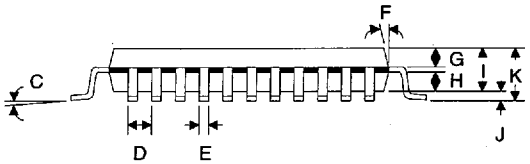
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

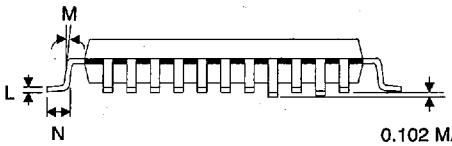
11

44 PIN QUAD FLATPACK

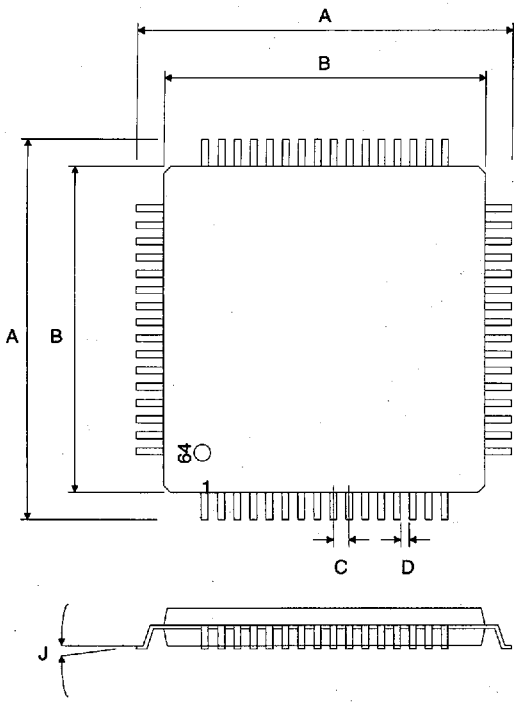


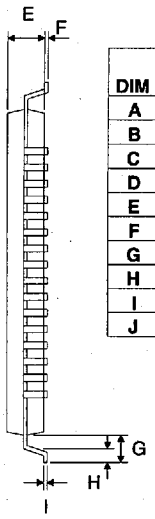
	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026





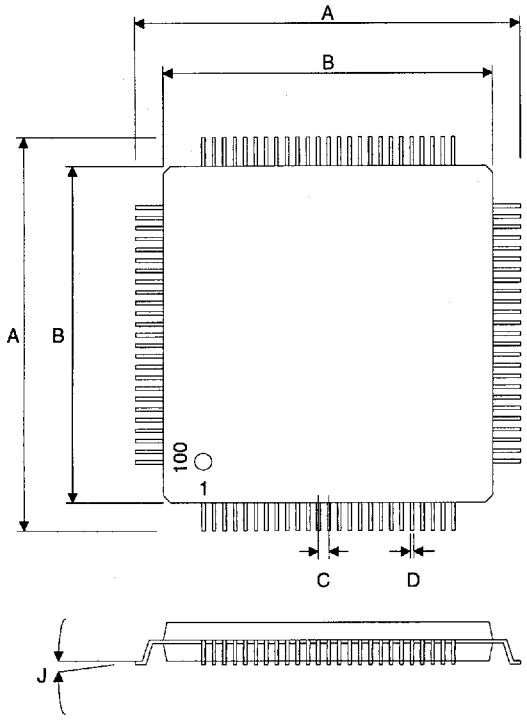
0.102 MAX
Lead Coplanarity

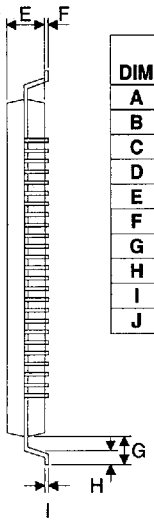




64 Pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

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