Semiconductor Corporation

CS61534

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and 2.048 MHz Applications
- Programmable Pulse-Shaping Line Driver
- Performs Data and Timing Recovery
- Transparent to AMI Polarity
- Diagnostic and Performance Monitoring Features
- Selectable Hardware or Host Processor Modes
- Jitter Attenuator
- 3 Micron CMOS for High Reliability

General Description

The CS61534 combines the analog transmit and receive line interface functions for a PCM system interface in one 28 pin device. The PCM line interface operates from a single 5 Volt supply, is transparent to the PCM framing format, and can work with ABAM and other cable types.

Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet in T1 applications. Maximum range is greater than 450 meters. The transmitter users an elastic store to remove jitter from the outgoing data prior to transmission.

3

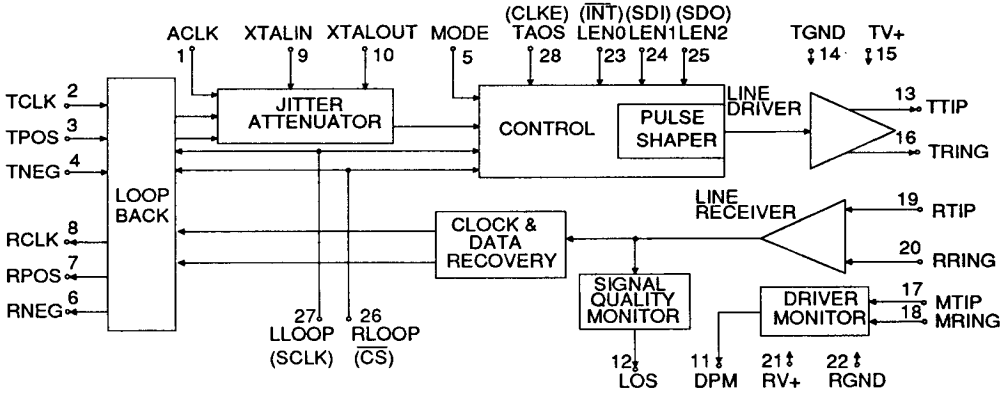
Applications

- Interfacing Network Equipment to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexers, Data PBX's and LAN Gateways to a channel Service Unit or T1 Modem.

ORDERING INFORMATION

CS61534-IP	- 28 Pin Plastic DIP	(T1 only)
CS61534-IP1	- 28 Pin Plastic DIP	(T1 & CEPT)
CS61534-IL	- 28 Pin J-lead PLCC	(T1 only)
CS61534-IL1	- 28 Pin J-lead PLCC	(T1 & CEPT)
CS61534-ID	- 28 Pin CERDIP	(T1 only)
CS61534-ID1	- 28 Pin CERDIP	(T1 & CEPT)

Block Diagram



Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 FAX: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+ TV+	- -	6.0 RV+ + 0.3	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	RV+ + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature Industrial Temperature Range	T_A=	-40	25	85	°C
Total Power Dissipation (Note 4) 100% ones density & max. line length @ 5.25V	P_D	-	-	760	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25 Ω load over operating temperature range. Includes CS61534 and load.

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 5, 6) Pins 1-5, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 5, 6) Pins 1-5, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 5, 6) I_{OUT}=-40 uA Pins 6-8, 11, 12, 23, 25	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 5, 6) I_{OUT}= 1.6 mA Pins 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA
High Impedance Leakage Current Pin 25 (Note 5)		-	-	±10	uA

Notes: 5. Functionality of pins 23 and 25 depends on the mode. See Host/Hardware mode description.
6. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Receiver Sensitivity Below DSX-1		-10	-	-	dB
Jitter Attenuation Curve Corner Frequency	(Note 7)	-	-	50	Hz
Receiver Jitter Tolerance	(Note 8)				
1.544 MHz:	8kHz - 40kHz	0.1	-	-	U.I.
	10Hz - 500Hz	5	-	-	U.I.
2.048 MHz:	18kHz - 100kHz	0.2	-	-	U.I.
	20Hz - 2.4kHz	1.5	-	-	U.I.
Input Jitter Tolerance -	Transmitter	7.0	-	-	U.I.
Loss of Signal Threshold		-	0.5	-	V
Transmitter Output Load	(Note 9)	-	25	-	ohms
AMI Output Pulse Amplitudes					
Line Length Selection LEN2/1/0 = 0/0/0 (Measured at xfmr output; 0/0/0 see Figure 7)		2.7	3.0	3.3	V
All Line Length settings except, LEN2/1/0 = 0/0/0 (Measured at the DSX; Normalization factor for Figure 6)		2.4	3.0	3.6	V
Power in 2kHz band about 772kHz	(Note 10)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544 MHz (referenced to power at 772kHz)	(Note 10)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Note 10)	-	0.2	0.5	dB

Notes:
7. Crystal pull range: ± 200 ppm. Five unit intervals of input jitter.
8. For CERDIP ICs, assumes IC is operated within -70 ° to +70 °C of reset temperature. For plastic ICs, assumes IC is operated within -25 ° to +40 °C of reset temperature (meets Bellcore central office specification: TR-EOP-000063 NEBS). For all packages, assumes IC is operated within 0.1V of reset V+. Input data pattern is quasi-random. For 1.544 MHz: (2↑20)-1 with 1-in-15. For 2.048 MHz: (2↑15)-1 as defined in CCITT 0.151. For frequencies not specified above, the jitter tolerance will be better than the AT&T 43802 line or the CCITT G.823 line shown in Figure 10.
9. Transmitter is a low impedance voltage source. Transmitter performance is typical with a 25Ω load for T1 applications, which is determined by the 2:1 turns ratio of transformer and 100 Ω line impedance.
10. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.

T1 SWITCHING CHARACTERISTICS (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V;
Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 11)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{in}	-	1.544	-	MHz
ACLK Frequency	(Note 12)	f_{out}	-	1.544	-	MHz
RCLK Pulse Width		t_{pwh}	-	324	-	ns
	(Note 13)	t_{pwl}	-	324	-	ns
Duty Cycle	(Note 14)		-	50	-	%
Rise Time, All Digital Outputs	(Note 15)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 15)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	0	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	50	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	274	-	ns
Reset Pulse Duration			0.2	-	2000	us

Notes: 11. Crystal must meet specifications described in CXT6176 data sheet.
12. ACLK provided by an external source.
13. The sum of the pulse widths must always meet the frequency specifications.
14. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
15. At max load of 1.6 mA and 50 pF.

CCITT SWITCHING CHARACTERISTICS (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; GND = 0V;
Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 16)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{in}	-	2.048	-	MHz
ACLK Frequency	(Note 17)	f_{out}	-	2.048	-	MHz
RCLK Pulse Width		t_{pwh}	-	244	-	ns
	(Note 18)	t_{pwl}	-	244	-	ns
Duty Cycle	(Note 19)		-	50	-	%
Rise Time, All Digital Outputs	(Note 20)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 20)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	0	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	50	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	194	-	ns
Reset Pulse Duration			0.2	-	2000	us

Notes: 16. Crystal must meet specifications described in CXT8192 data sheet.
17. ACLK provided by an external source.
18. The sum of the pulse widths must always meet the frequency specifications.
19. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
20. At max load of 1.6 mA and 50 pF.

SWITCHING CHARACTERISTICS - HOST MODE (T_A = T_{min} to T_{max}; V+ = 5.0V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ.	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	250	-	-	ns
SCLK High Time	t_{ch}	250	-	-	ns
SCLK Rise and Fall Time	t_r , t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 21)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns

Note: 21. Output load capacitance = 50 pF.

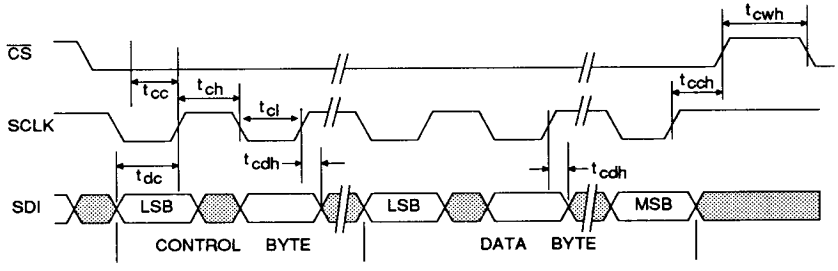


Figure 1. - Serial Port Write Timing Diagram

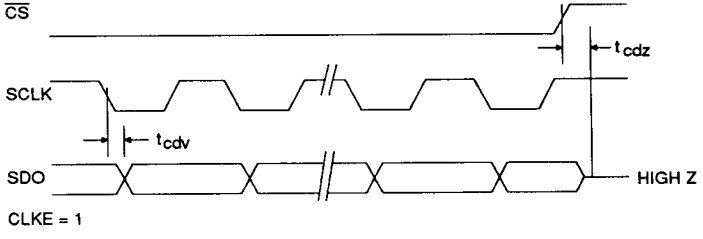


Figure 2. - Serial Port Read Timing Diagram

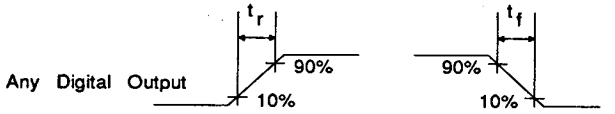


Figure 3. - Signal Rise and Fall Characteristics

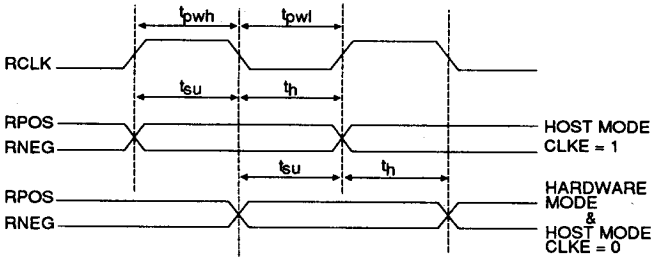


Figure 4. - Recovered Clock and Data Switching Characteristics

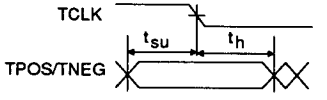


Figure 5. - Transmit Clock and Data Switching Characteristics

THEORY OF OPERATION

Transmitter

The transmitter takes binary (unipolar) data from a PCM transceiver and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

The CCITT pulse shape and T1 pulse shapes for line lengths from 0 to 655 feet (as measured from the CS61534 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver is a low-impedance voltage source designed to drive a 25 Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2, LLOOP, or RLOOP) is toggled, the transmitter stabilizes within 16 bit periods.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	CABLE TYPE
0	1	1	0-220	MAT and ICOT
0	0	1	220-440	
0	1	0	440-655	
0	1	1	0-133	ABAM (AT&T 600B or 600C)
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	0	G.703	2.048 MHz CCITT

Table 1. Line Length Selection

Transmit Line Length Selection

For T1 applications, the line length selection supports both a three partition arrangement for ICOT and MAT cable, and a five partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS61534 modifies the output pulse to meet the requirements of Compatibility Bulletin 119 and TR-TSY-000009. A typical output pulse is shown in Figure 6.

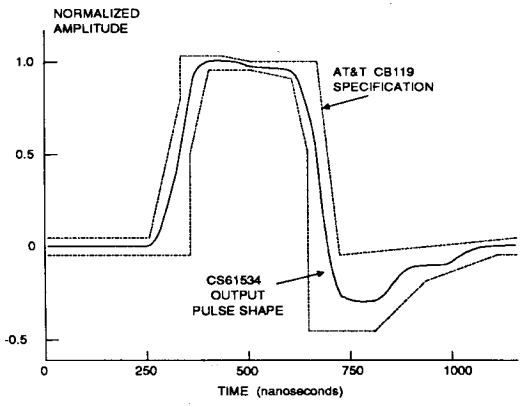


Figure 6. Typical Pulse Shape at DSX-1 Cross Connect

The remaining line length selection is for CCITT options. Transformer and resistor values depend on whether the coax or shielded cable is used, as shown in the *Applications* section at the back of this data sheet. The CCITT pulse shape meets the template shown in Figure 7, and the requirements of Table 2 for the given load conditions.

Transmit Jitter Attenuator

The CS61534 will tolerate and attenuate at least seven unit intervals of jitter (peak-to-peak) from a signal. Figure 8 shows a family of curves which show the jitter attenuation achieved by the CS61534 at T1 data rates. Each curve shows the jitter attenuation for a signal with constant jitter amplitude over a range of jitter frequencies. The

	For coaxial cable, 75 ohm load and transformer specified in Table A2.	For shielded twisted pair, 120 ohm load and transformer specified in Table A2.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

Table 2. CCITT G.703 Pulse Specifications

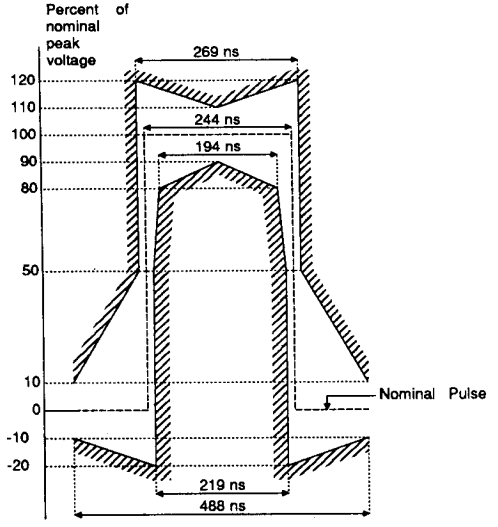


Figure 7. Mask of the Pulse at the 2048 kbps Interface

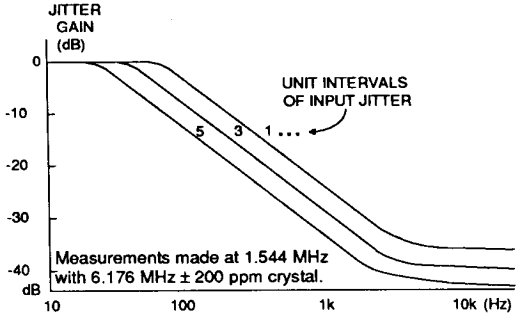


Figure 8. Jitter Attenuation Curves

more jitter a signal has, the more the jitter is attenuated. The jitter attenuator on the transmitter side meets the jitter attenuation and input tolerance specifications of AT&T Publication 43802, as shown in Figures 9 and 10.

The external reference crystal used by the jitter attenuator should have a nominal frequency of 6.176 MHz, (8.192 MHz for PCM-30 rates), and have a pull range, in the oscillator circuit, that is

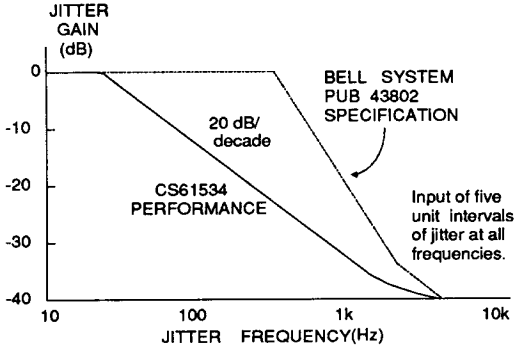


Figure 9. Jitter Attenuation Characteristics

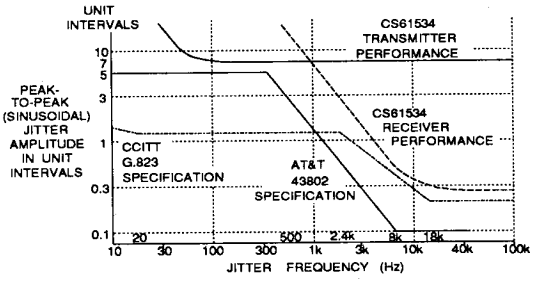


Figure 10. Typical Input Jitter Tolerance

sufficient to meet the frequency tolerance requirements specified for the system. Furthermore, the frequency tolerance must be met over all operating temperatures. The jitter attenuator can be disabled by driving XTALIN with a clock which is *exactly* four times the TCLK frequency. Remote loopback should not be used if the jitter attenuator is disabled.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of the alternate clock input, ACLK. The transmit clock can be used as the alternate clock by connecting pins 1 and 2 together. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING) using the alternate clock, ACLK. In this mode, the TPOS, TNEG and TCLK inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of DSX-1/PCM-30 cable lengths and requires no equalization. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61534 side. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publication 43802 and CCITT G. 823, (see Figure 10).

The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Clock recovery is achieved through a frequency and phase lock loop (FPLL). Upon power up and reset of the CS61534, and prior to the start of clock acquisition, the FPLL has its center frequency trained. A current controlled oscillator (ICO) is trained relative to the crystal oscillator frequency reference. The current is adjusted until the ICO is near the reference frequency. This current is then held constant. The FPLL is controlled, small signal, by the output of the phase detector and loop filter, which takes the form of a current. This is added to the fixed current to modulate the ICO about the center frequency and close the loop. The FPLL is insensitive to variations in temperature and slight variations in power supply voltage as shown in the Analog Specifications table, but fairly large changes in power supply voltage will change the control current in the FPLL, reducing its effectiveness. Resetting the CS61534 will optimize receiver performance for the operating power supply and temperature.

In the hardware mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 3.

Loss of Signal

The receiver reports loss of the received signal on the Loss of Signal pin, LOS. The threshold for loss of signal is 0.5 volts. A loss of signal will be indicated within 200 bit periods if an active signal

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW	X	RPOS	RCLK	Rising
		RNEG	RCLK	Rising
HIGH	LOW	RPOS	RCLK	Rising
		RNEG	RCLK	Rising
		SDO	SCLK	Falling
HIGH	HIGH	RPOS	RCLK	Falling
		RNEG	RCLK	Falling
		SDO	SCLK	Rising

X= Don't care

Table 3. Data Output / Clock Relationship

falls below the threshold. In the event that the input signal drops to zero volts, the loss of signal will be indicated within 31 bit periods. When a loss of signal is detected, RPOS and RNEG are not valid, but the receiver will continue to try to recover data. LOS will return to a low state when a valid signal returns to RTIP and RRING. RCLK is always output but may drift up to 6% from the nominal frequency. Note that in the host mode, LOS is simultaneously available from pin 12 and the register.

Local Loopback

The local loopback mode bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. A local loopback occurs in response to LLOOP going high. The transmit data and clock signals (TPOS, TNEG and TCLK) are sent out on the line through TTIP and TRING unless transmit all ones, TAOS, is selected, in which case AMI-coded continuous ones are transmitted on the line at the rate determined by ACLK.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the elastic store to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 4). The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset). Bipolar violations are passed unchanged through the CS61534 during remote loopback.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS61534 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring CS61534. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TPOS & TNEG	TCLK
0	1	all 1s	ACLK
1	X	RTIP & RRING	RTIP & RRING

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 4. Interaction of RLOOP and TAOS

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, the DPM pin goes high.

To provide immunity from spurious DPM reports, the following application procedure is recommended: If the controller on the line card detects that DPM has gone high, the controller should reconfirm that DPM is still high before taking actions to respond to the driver failure. The intent of the reconfirmation is to screen out events where

DPM goes high for a few bit periods, erroneously indicating a driver problem. This situation can occur only when ones density is very low.

Whenever more than one CS61534 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS61534 monitor performance of a neighboring CS61534 device, rather than having it monitor its own performance. Note that in the host mode, DPM is available from both the register and pin 11.

Reset

The CS61534 initiates internal reset procedures either on power up or in response to a reset request. After initial power up, the device will delay for approximately 10 ms before initiating the training procedure for the FPLL. It is advisable to issue a reset request after the power supply has stabilized and signals have been applied to the device to ensure that conditions on the chip are stable before the FPLL training takes place. Training the FPLL takes at most 43ms, but typically requires less than half that amount of time. These conditions should also be adhered to if temporary loss of power supply occurs.

In the Hardware Mode, a reset request is made by simultaneously setting both RLOOP and LLOOP high for a period not to exceed 2 ms. Reset will be completed within 53 ms after the falling edge of the reset request (falling edge of RLOOP and LLOOP).

In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. The device will first clear its data registers then initiate the FPLL training procedure which will be complete within 53 ms.

During the reset procedure, the loss of signal indicator, LOS, is high. Once the reset procedures are completed, the loss of signal indicator goes low signifying that normal operation of the device has begun.

Mode of Operation

The CS61534 can be operated in two modes, the hardware mode and the host mode. In the hardware mode, discrete pins are used to interface the device's control functions and status information. In the host mode, the CS61534 is connected to a host processor and a serial data bus is used for input and output of control and status information. There are six dual function pins whose functionality is determined by the mode pin, MODE. Table 5 shows the pin definitions.

PIN #	MODE	
	HARDWARE	HOST
PIN 23	LEN0	$\overline{INT}$
PIN 24	LEN1	SDI
PIN 25	LEN2	SDO
PIN 26	RLOOP	$\overline{CS}$
PIN 27	LLOOP	SCLK
PIN 28	TAOS	CLKE

Table 5. Pin Definitions

Serial Interface

In the host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to the SDI pin or read from the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 3. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no

sooner than 50 ns after the falling edge of the 16th SCLK cycle, and must go high before the rising edge of the 24th SCLK cycle.

Figure 11 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 0, data output from the serial port, SDO, is valid on the falling edge of SCLK. Data bit D7 is held until the rising edge of the 17th clock cycle.

An address/command byte, shown in Table 6, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The CS61534 responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 6. Address / Command Byte

The data register, shown in Table 7, can be read/written by the serial port. Data is input/output on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are read only. During a write to the register, the CS61534 ignores the first two bits of the data byte. SDO goes to a high-impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

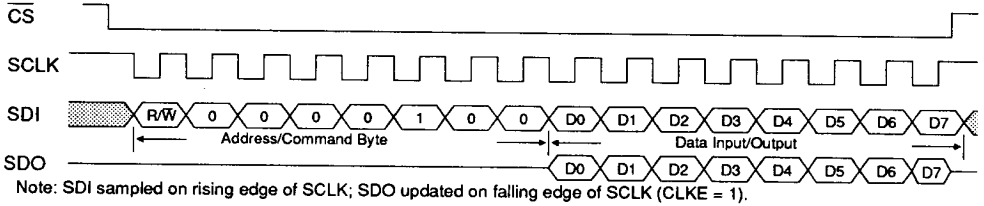
LSB: first bit in or out	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in or out	7	TAOS	Transmit All Ones Select

Table 7. Data Register

Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap breadboarding of the CS61534 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

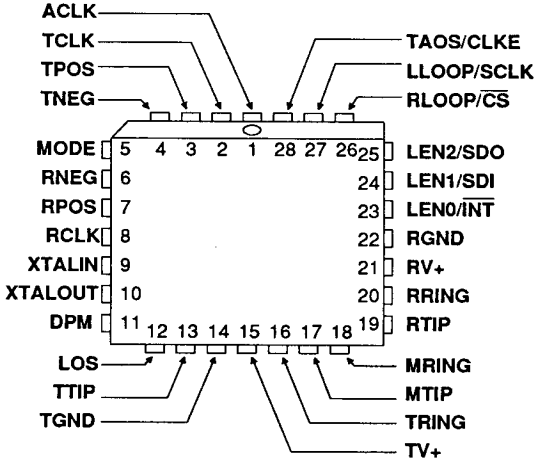


Note: SDI sampled on rising edge of SCLK; SDO updated on falling edge of SCLK (CLKE = 1).

Figure 11. Input / Output Timing

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	ACLK	1	28	TAOS/CLKE — TRANSMIT ALL ONES / CLOCK EDGE
TRANSMIT CLOCK	TCLK	2	27	LLOOP/SCLK — LOCAL LOOPBACK / SERIAL CLOCK
TRANSMIT POSITIVE PULSE	TPOS	3	26	RLOOP/$\overline{CS}$ — REMOTE LOOPBACK / CHIP SELECT
TRANSMIT NEGATIVE PULSE	TNEG	4	25	LEN2/SDO — LINE / SERIAL DATA OUT
MODE SELECTION	MODE	5	24	LEN1/SDI — LENGTH / SERIAL DATA OUT
RECEIVED NEGATIVE PULSE	RNEG	6	23	LEN0/$\overline{INT}$ — SELECT / ALARM INTERUPT
RECEIVED POSITIVE PULSE	RPOS	7	22	RGND — RECEIVE GROUND
RECOVERED CLOCK	RCLK	8	21	RV+ — RECEIVE V+ (+5VDC)
CRYSTAL CONNECTION	XTALIN	9	20	RRING — RECEIVE RING
CRYSTAL CONNECTION	XTALOUT	10	19	RTIP — RECEIVE TIP
DRIVER PERFORMANCE MONITOR	DPM	11	18	MRING — MONITORED RING
LOSS OF SIGNAL	LOS	12	17	MTIP — MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING — TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+ — TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.
Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.
Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.

Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz (8.192 MHz for CCITT applications) crystal should be connected across these pins. If desired, an externally generated 6.176 MHz (8.192 MHz for CCITT) clock signal may be input to XTALIN, pin 9; XTALOUT, pin 10, should be left floating. Overdriving the oscillator with an external source disables the jitter attenuator. This externally generated clock must be *exactly* four times the frequency of the TCLK signal.

Control

MODE - Mode Select, Pin 5.

Setting MODE to logic 1 puts the CS61534 in the host mode. In the host mode, a serial control port is used to control the CS61534 and determine its status. Setting MODE to logic 0 puts the CS61534 in the hardware mode, where configuration and status are controlled by discrete pins. MODE defines the status of pins 23 through 28.

Hardware Mode

TAOS - Transmit All Ones Select, Pin 28.

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLK.

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins, bypassing the receive circuit. TCLK and TPOS/TNEG are still transmitted unless overridden by a TAOS request.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Any TAOS request is ignored. If the oscillator is being driven with a 4x clock, the remote loopback function is not possible.

Simultaneously taking RLOOP and LLOOP high for less than 2 ms initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

Host Mode

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23.

Goes low when received signal is lost (LOS is high), or the transmitter driver has failed (DPM is high), to flag the host processor. $\overline{\text{INT}}$ will stay low until the fault condition goes away. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24.

Data for the on-chip registers and is sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25.

Status and control information from the on-chip registers. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or $\overline{\text{CS}}$ is high.

CLKE - Clock Edge, Pin 28.

Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27.

Clock used to read or write the serial port registers.

$\overline{\text{CS}}$ - Chip Select, Pin 26.

Pin must transition from high to low to read or write the serial ports.

Inputs

ACLK - Alternate External Clock, Pin 1.

This input should be tied to TCLK or some other externally generated 1.544 (or 2.048) MHz clock. The frequency of ACLK determines the rate at which TAOS is output.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. Signal jitter is attenuated and the signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1. Data and clock are recovered and output on RPOS/RNEG and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS61534. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{INT}$ pin in the host mode is used, and the monitor is not used, input a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-voltage level. This clock frequency can range from 100 kHz to the TCLK frequency.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when the received signal falls below a 0.5 volt threshold, or after 31 clock cycles without a detected one. LOS returns to logic 0 when signal returns.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, DPM goes to a logic 1 until the first detected signal.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

Data and clock are recovered from the RTIP and RRING inputs are output at these pins. A signal on RPOS corresponds to a positive pulse received on RTIP and RRING, while a signal on RNEG corresponds to the receipt of a negative pulse. RPOS and RNEG are NRZ. In the hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 3.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. This output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, approximately 4.4 Ω of resistance should be added in series with the transformer primary. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω, without additional components.

APPLICATIONS

Line Interface

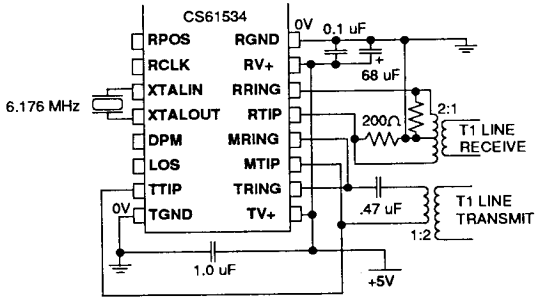


Figure A1. Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS61534 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS61534 side. These resistors provide the 100 Ω termination for the T1 line. When terminating twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

Figure A2 shows the configuration needed for transmitting data at 2.048 MHz onto a 75 Ω coax cable. The 2.2 Ω resistors serve two functions.

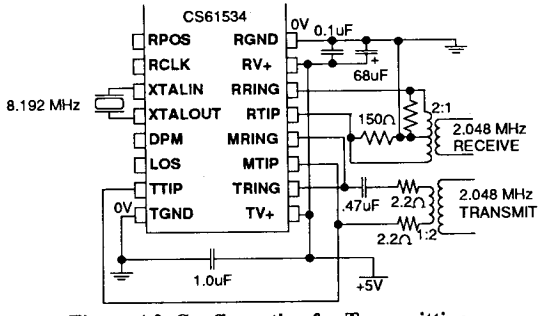


Figure A2. Configuration for Transmitting onto 75 Ω Coax

First, they provide the appropriate 25 Ω load to TTIP and TRING. Second, the resistors attenuate the signal slightly to meet the CCITT pulse amplitude requirements. Note that these 2.2 Ω resistors should not be used when interfacing to CCITT 120 Ω cable. For the receiver, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61534. It is recommended that the Crystal Semiconductor CXT6176 crystal be used for T1 applications and the CXT8192 crystal be used for PCM-30 applications.

Transformers

Transformers listed in Table A1 have been found to be suitable for use with the CS61534.

Figure A3 shows the connections for some of the recommended transformers for the transmitter. Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1) ± 5%,

Primary inductance: 600 µH min measured at 772 kHz

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted

Secondary leakage inductance: 0.4 µH max at 772 kHz

Interwinding capacitance: 23 pF max, primary to secondary

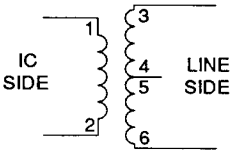
ET-Constant: 16 V-µs minimum for T1; 12 V-µs for CEPT

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer, interacting with the driver, can cause a slight voltage difference (<200 mV) between the driven zero and the non-driven zero. We recommend that this ef-

Manufacturer	Part #
Pulse Engineering	PE-64931
Pulse Engineering	PE-64951 (dual)
Schott Corp.	67115100 & 67124670
Schott Corp.	68115090 (dual)
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-0001
Midcom	671-5832

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the above Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the above Schott transformers are preferred.

Table A1. Suitable Transformers



Bell Fuse 0553-5006-IC
Schott Corp. 67115100
Pulse Engineering 5764 & PE-64931

Figure A3.Some Recommended Transmitter/Transformer Connections

fect be eliminated by inserting a 0.47uF non-polarized capacitor in series with the primary of the transmit transformer.

Receive Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the received signal. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the recovered clock and data as shown in Figure A4. In the host mode, the inverter is not needed if CLKE is high.

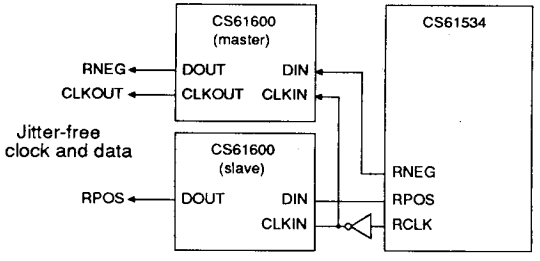


Figure A4. Receive Jitter Attenuation

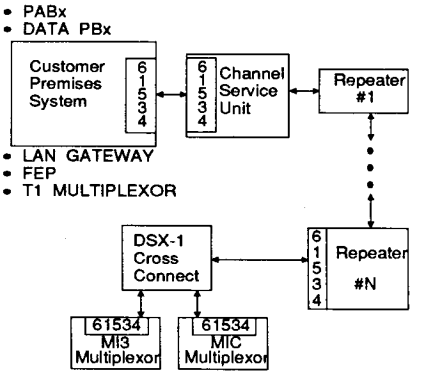


Figure A5. Application of CS61534

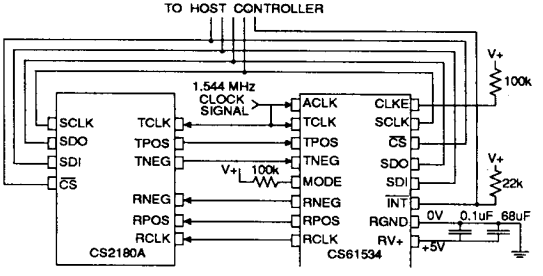


Figure A6. Interfacing the CS61534 with a CS2180A

Applicable Systems

Figure A5 shows a T1 span from a customer premises location through a TELCO DSX-1 cross connect. As shown in Figure A5, the CS61534 is applicable in customer premises systems that interconnect to a channel service unit (CSU), and in network equipment that connects to a DSX-1 cross connect.

Interfacing The CS61534 With T1 Digital Transceivers

To interface with the CS2180A, connect the devices as shown in Figure A6. In this case, the CS61534 and CS2180A are in host mode controlled by a microprocessor serial interface. If the CS61534 is used in hardware mode, then the CS61534 RCLK output must be inverted before being input to the CS2180A.