Semiconductor Corporation

CS6401

Programmable Echo Canceller

Features

- For All Echo Canceller Applications
  - Digital Cellular Network Equipment
  - Analog Cellular Hands Free
  - Digital Cellular Hands Free
  - Office Speaker Phones
  - Desktop Teleconferencing
  - Long Distance Network Equipment
- Echo Cancellation
  - 8 kHz Sampling Rate
  - 512 tap (64 ms)
  - Split Mode for Two ECs (total taps = 512)

General Description

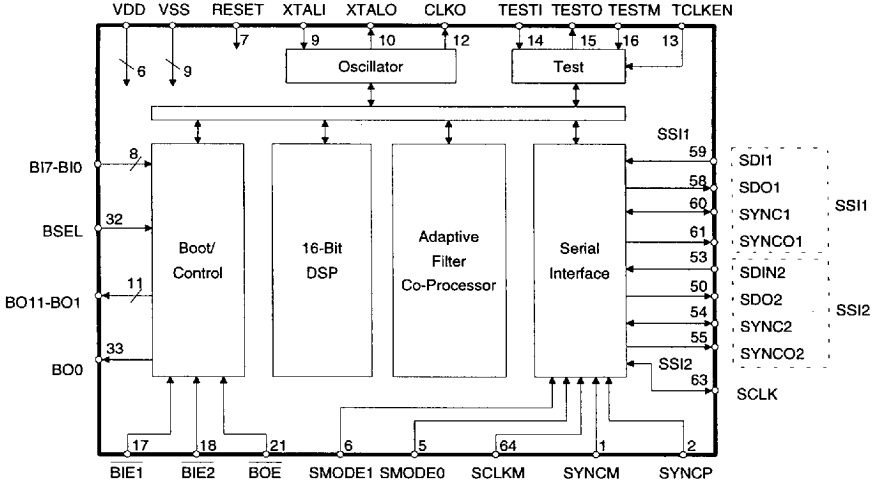
The CS6401 is a digital signal processor optimized for acoustic and/or network echo cancellation algorithms. The CS6401 implements all the adaptive filtering and control algorithms needed for high quality echo cancellation for a variety of applications. Crystal has developed the echo cancellation algorithms, and provides the DSP object code with the evaluation board. Custom algorithm development services are available from Crystal.

The CS6401 contains four main blocks:

- 16 MIPS, 16-Bit Programmable DSP
- 512-tap Adaptive FIR Filter Hardware Accelerator
- Data I-O Serial Interface
- Boot/Control Interface

ORDERING INFORMATION

CS6401-CQ	0 to 70 °C	64-pin Plastic QFP
CDB6401	Evaluation Board with object code	



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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(512) 445-7222 Fax: (512) 445-7581

ABSOLUTE MAXIMUM RATINGS (VSS = 0V, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	VDD	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	(VDD)+0.4	V
Ambient Operating Temperature (power applied)	T_{Amax}	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS = 0V; all voltages with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VDD	4.50	5.0	5.50	V
Ambient Operating Temperature	T_A	0	-	70	°C

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VDD = 5V ± 10%; measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-		V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at I_o = -2.0mA	V_{OH}	2.4	-	-	V
Low-Level Output Voltage at I_o = 2.0mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	1.0	µA.

Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Crystal Oscillator Frequency	fCLK	-	32.768	-	MHz

Serial Mode A (SMODE1=L, SMODE0=L, SCLKM=H, SYNCM=H, SYNCP=L)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	fSCK	-	2.048	-	MHz
SCLK Pulse Width Low	tSCKL	200	-	-	ns
SCLK Pulse Width High	tSCKH	200	-	-	ns
SYNC2 Frequency	fSYNC	-	8	-	kHz
SYNC2 Pulse Width Low	tSYNL	-	3906	-	ns
SCLK rising to SDO1, 2 Valid	tCD	-	-	60	ns
SCLK2 rising to SDO1, 2 Valid	tSYD	-	-	40	ns
SCLK rising to SYNC2 edge	tCSD	-	-	20	ns
SDI1, 2 data setup time	tSU	40	-	-	ns
SDI1, 2 data hold time	tHD	40	-	-	ns

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Serial Mode B (SMODE1=L, SMODE0=L, SCLKM=L, SYNCM=H, SYNCP=H)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	fSCK	-	2.048	-	MHz
SCLK Pulse Width Low	tSCKL	120	-	-	ns
SCLK Pulse Width High	tSCKH	120	-	-	ns
SYNC2 Frequency	fSYNC	-	8	-	kHz
SYNC2 Pulse Width Low	tSYNL	-	488	-	ns
SCLK rising to SDO1, 2 Valid	tCD	-	-	120	ns
SCLK2 rising to SDO1, 2 Valid	tSYD	-	-	60	ns
SCLK rising to SYNC2 edge	tCSD	-	-	60	ns
SDI1, 2 data setup time	tSU	20	-	-	ns
SDI1, 2 data hold time	tHD	20	-	-	ns

Serial Mode C CS4216 Application (SMODE1=L, SMODE0=H, SCLKM=H, SYNCM=H, SYNCP=H)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	FSCK	-	2.048	-	MHz
SCLK Pulse Width Low	tSCKL	220	-	-	ns
SCLK Pulse Width High	tSCKH	220	-	-	ns
SYNC2 Frequency	fSYNC	-	8	-	kHz
SYNC2 Pulse Width Low	tSYNL	-	488	-	ns
SCLK rising to SDO 2 Valid	tCD	-	-	70	ns
SYNC2 falling to SDO 2 Valid	tSYD	-	-	50	ns
SCLK rising to SYNC2 edge	tCSD	-	-	20	ns
SDI2 data setup time	tSU	30	-	-	ns
SDI2 data hold time	tHD	30	-	-	ns

Serial Mode D (SMODE1=H, SMODE0=L, SCLKM=H, SYNCM=H, SYNCP=L)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	FSCK	-	512	-	kHz
SCLK Pulse Width Low	tSCKL	960	-	-	ns
SCLK Pulse Width High	tSCKH	960	-	-	ns
SYNC1 Frequency	fSYN1	-	2.048	-	MHz
SYNC1 Pulse Width Low	tSY1L	-	244	-	ns
SYNC1 Pulse Width High	tSY1H	-	244	-	ns
SYNC2 Frequency	fSYN2	-	8	-	kHz
SYNC2 Pulse Width Low	tSY2L	-	62.5	-	us
SYNC2 Pulse Width High	tSY2H	-	62.5	-	us
SCLK falling to SDO2 Valid	tCD	-	-	60	ns
SCLK falling to SYNC2 edge	tCSD	-	-	30	ns
SYNC rising to SCLK edge	tSYSD	-	-	10	ns
SDI2, data setup time	tSU	40	-	-	ns
SDI2, data hold time	tHD	40	-	-	ns

Serial Mode E Network Application (SMODE1=H, SMODE0=H, SCLKM=L, SYNCM=L, SYNCP=L)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	FSCK	-	2.048	-	MHz
SCLK Pulse Width Low	tSCKL	120	-	-	ns
SCLK Pulse Width High	tSCKH	120	-	-	ns
SYNC1, 2 Frequency	fSYNC	-	8	-	kHz
SYNC1, 2 Pulse Width High	tSYNH	-	3906	-	ns
SYNCO1, 2 Frequency	fSYO	-	8	-	kHz
SYNCO1, 2 Pulse Width High	tSYOH	-	3906	-	us
SCLK rising to SDO1, 2 Valid	tCD	-	-	120	ns
SCLK rising to SYNC1, 2 edge	tCSD	-	-	60	ns
SYNC rising to SYNCOUT1, 2 edge	tCSOD	-	-	60	ns
SDI1, 2 data setup time	tSU	20	-	-	ns
SDI1, 2 data hold time	tHD	20	-	-	ns

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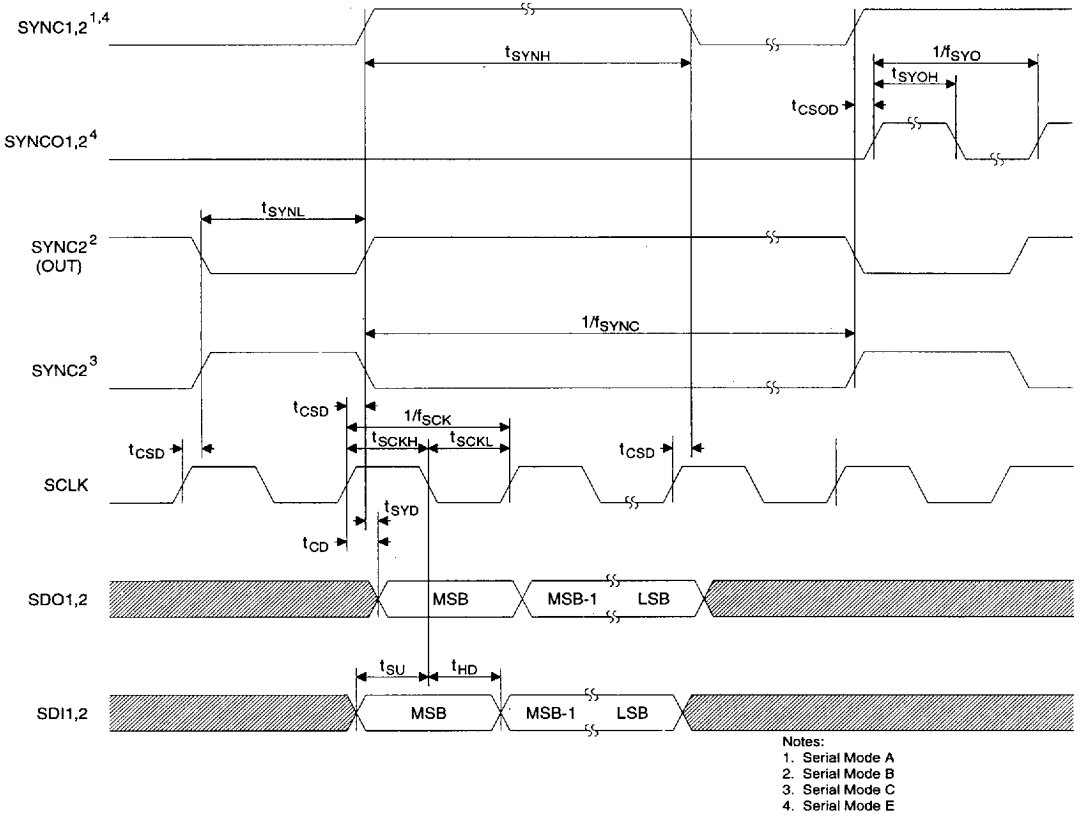

Figure 1. Serial Mode A, B, C, and E Timing.

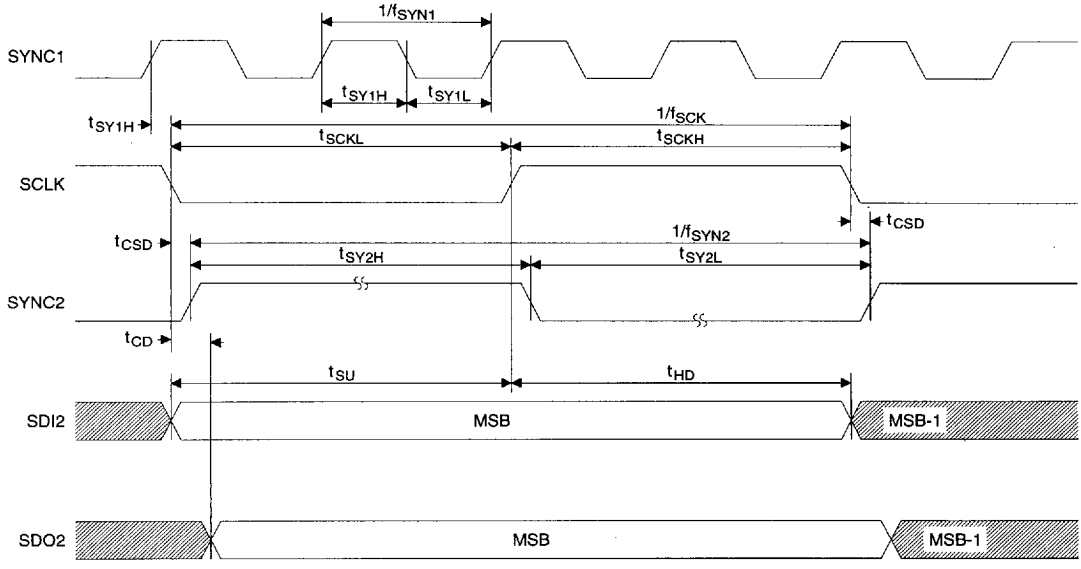

Figure 2. Serial Mode D Timing

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Boot Mode 1: Boot with Parallel EPROM (CS6401 is boot master. BSEL=L, $\overline{BIE1}$=L, $\overline{BIE2}$=L, $\overline{BOE}$=L)

Parameter	Symbol	Min	Typ	Max	Units
RESET Pulse Width High	tRSTH	300	-	-	ns
RESET Falling to $\overline{BIEX}$ Latch	tRBI	-	76/fCLK	-	s
RESET Falling to BSEL Latch	tRBS	-	80/fCLK	-	s
RESET Falling to BO [11:0] become [000]	tRBO	-	130/fCLK	-	s
BO0 Pulse width Low (for upper byte)	tBOTL1	-	112/fCLK	-	s
BO0 Pulse Width High (for upper byte)	tBOTH1	-	68/fCLK	-	s
BO0 Pulse width Low (for lower byte)	tBOL2	-	106/fCLK	-	s
BO0 Pulse Width High (for lower byte)	tBOTH2	-	86/fCLK	-	s
BO0 Falling to BIN [7:0] Latch	tBOBI	-	30/fCLK	-	s
BI [7:0] setup time	tBISU	60		-	ns
BI [7:0] hold time	tBIHD	60		-	ns
Boot Procedure Period	tBOOT	-	285084/ fCLK	-	s

Boot Mode 2: Boot with Serial PROM (CS6401 is boot master. BSEL=H, $\overline{BIE1}$=L, $\overline{BIE2}$=L, $\overline{BOE}$=L)

Parameter	Symbol	Min	Typ	Max	Units
RESET Pulse Width High	tRSTH	300	-	-	ns
RESET Falling to $\overline{BIEX}$ Latch	tRBI	-	76/fCLK	-	s
RESET Falling to BSEL Latch	tRBS	-	80/fCLK	-	s
RESET Falling to BO0 Falling	tRBO	-	100/fCLK	-	s
BO0 Pulse width Low	tBOTL1	-	36/fCLK	-	s
BO0 Pulse Width High (for bit15 bit1)	tBOTH1	-	32/fCLK	-	s
BO0 Pulse Width High (for bit0)	tBOTH2	-	60/fCLK	-	s
BO0 Falling to BI7 Latch	tBOBI	-	24/fCLK	-	s
BI7 setup time	tBISU	60	-	-	ns
BI7 hold time	tBIHD	60	-	-	ns
Boot Procedure Period	tBOOT	-	854958/ fCLK	-	s

Boot Mode 3: Boot with Parallel uP or DSP (CS6401 is boot slave. BSEL=L, BIEX=H at RESET, Controlled by Boot Master)

Parameter	Symbol	Min	Typ	Max	Units
RESET Pulse Width High	tRSTH	300	-	-	ns
RESET Falling to $\overline{BIEX}$ Latch	tRBI	-	76/fCLK	-	s
RESET Falling to BSEL Latch	tRBS	-	78/fCLK	-	s
RESET Falling to $\overline{BIEX}$ Falling	tRBI2	132/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width Low (for upper byte)	tBINEL1	106/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width High (for upper byte)	tBINEH1	62/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width Low (for lower byte)	tBINEL2	100/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width High (for lower byte)	tBINEH2	80/fCLK	-	-	s
BIEX Falling to BI [7:0] Latch	tBINB	-	10/fCLK	-	s
BI [7:0] setup time	tBISU	200	-	-	ns
BI [7:0] hold time	tBIHD	200	-	-	ns

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Boot Mode 4: Boot with Serial uP or DSP (CS6401 is boot slave. BSEL=H, BIEX=H at RESET, Controlled by Boot Master)

Parameter	Symbol	Min	Typ	Max	Units
RESET Pulse Width High	tRSTH	300	-	-	ns
RESET Falling to $\overline{BIEX}$ Latch	tRBI	-	76/fCLK	-	s
RESET Falling to BSEL Latch	tRBS	-	78/fCLK	-	s
RESET Falling to $\overline{BIEX}$ Falling	tRBI2	100/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width Low	tBINEL	30/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width High (for bit15 bit1)	tBINEH1	32/fCLK	-	-	s
$\overline{BIEX}$ Pulse Width High (for bit0)	tBINEH2	54/fCLK	-	-	s
BIEX Falling to BI7 Latch	tBINEB	-	10/fCLK	-	s
BI7 setup time	tBISU	200	-	-	ns
BI7 hold time	tBIHD	200	-	-	ns

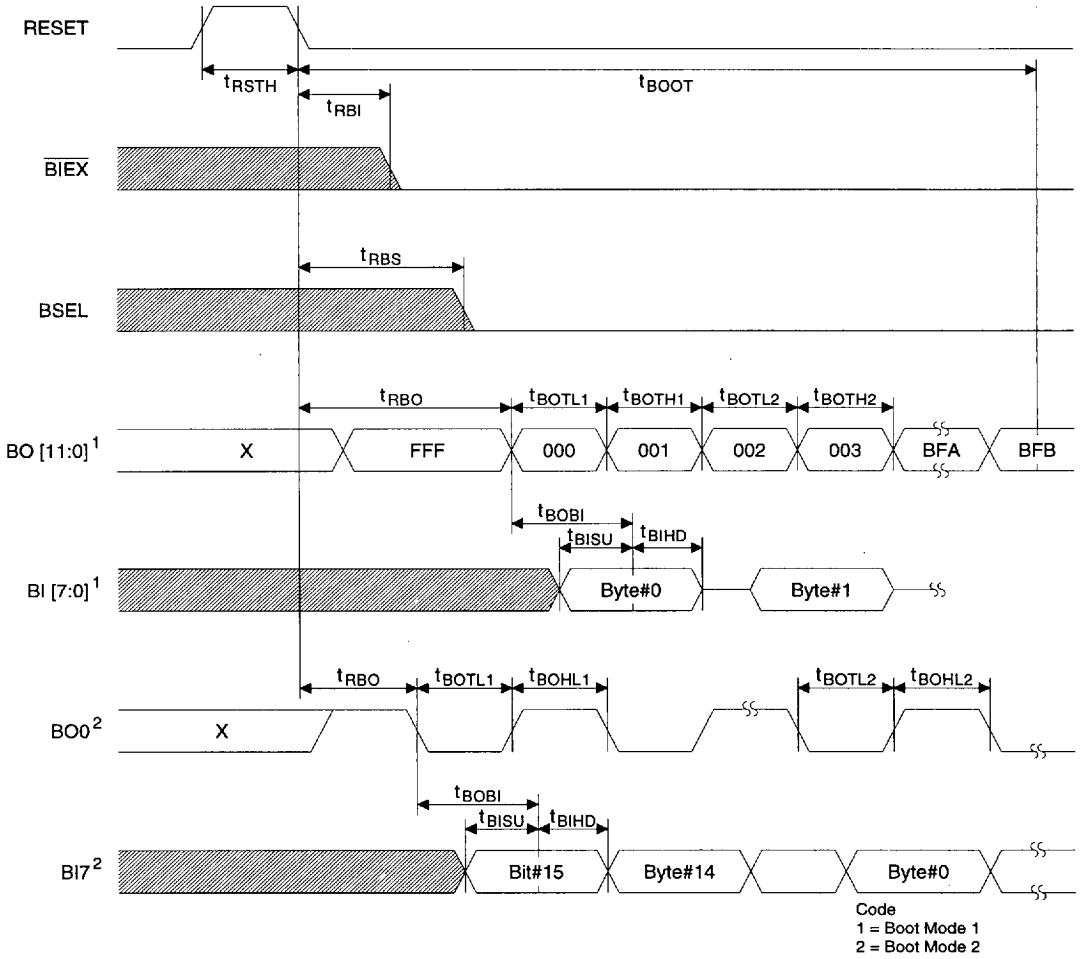

Figure 3. Boot Mode 1 and Mode 2

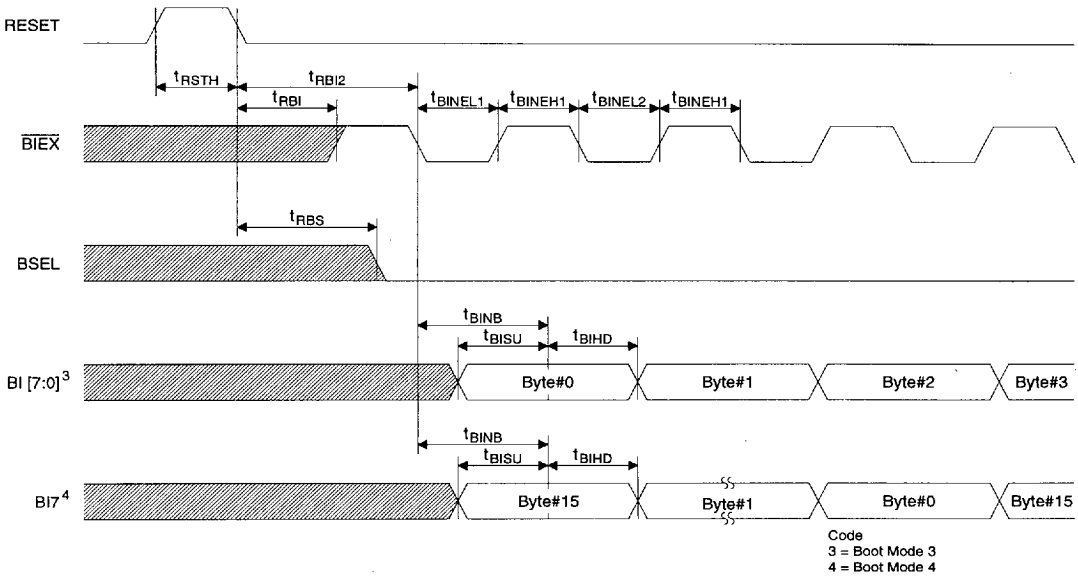

Figure 4. Boot Mode 3 and Mode 4

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GENERAL DESCRIPTION

OVERVIEW

The CS6401 is a programmable custom DSP optimized for echo cancellation in telephony applications.

Internally, the CS6401 is divided into a programmable DSP section and an adaptive filter coprocessor (AFP) unit. Boot interface and two serial ports are provided. Because the CS6401 is an application specific DSP designed to perform the echo-cancellation function, many of the features found in general purpose DSPs are not implemented in favor of performing the desired function as efficiently as possible. This efficiency is the reason that the CS6401 can provide high quality echo-cancellation at a much lower price than comparable general-purpose DSPs.

In the CS6401, digital audio data received via the serial port is processed by the AFP using the Normalized Least Mean Squared (NLMS) update algorithm to produce an echo estimate which is digitally subtracted by the DSP. This echo-cancelled data is sent back through the serial port back to a codec or supervisory DSP.

The programmable DSP executes 16.384 million instruction cycles every second when using a 32.768 MHz clock source. The DSP features 128 words of 16-bit Data RAM, 256 words of 16-bit Program ROM, and 768 words of 16-bit Program RAM. The Program ROM contains code for Linear/μ-Law conversions, multiply, divide, multiply/accumulates, and software initiated booting. The DSP usually runs the update control algorithms as well as supplementary suppression and other code.

The AFP implements 512 taps of adaptive FIR filtering using the NLMS algorithm, which provides 64 ms of echo cancellation at an 8 kHz sample rate. The AFP features 512 taps of 18-bit Coefficient RAM, 512 taps of 14-bit Buffer RAM, and the NLMS update and convolution engine. The AFP can also implement a split mode to create two distinct echo chancellors. This is especially useful in speakerphone applications that need both acoustic echo-cancellation and network echo-cancellation.

The Program RAM in the DSP is loaded with program code via the boot interface. The program code is provided by Crystal Semiconductor. For more details, see the CWECAXB data sheet. The boot interface loads the CS6401 program into the Program RAM from an external code source such as an EPROM, DSP, or microcontroller. The boot interface is capable of booting either serially or in parallel and can be either master of the boot process or slave. After the boot is complete, the boot interface is available as general purpose inputs and outputs to the CS6401. There are eight inputs and twelve outputs in the boot interface.

The serial interface provides two channels of data for the CS6401. The serial interface has four modes with master/slave options. It can directly interface to popular single-channel or dual channel codecs, as well as most general-purpose DSPs.

Echo Cancellation Overview

A block diagram of a situation that requires an echo-canceller is shown below in Figure 5. A training signal is applied at FE_IN and the desired signal at FE_OUT is S(t). With no echo-canceller in the system, the signal at FE_OUT is S(t)+H*FE_IN, which has the unwanted component of FE_IN. The echo canceller filter must adapt itself to appear equivalent to the path response, H. Then, when the echo canceller is active, the signal at FE_OUT will be S(t) + H*FE_IN - H*FE_IN, or just S(t).

A hands-free phone is a good practical example of a situation that would benefit from an echo-canceller. H would represent the room response from speaker to microphone and S(t) would be the talker on the hands-free phone. The talker at FE_IN does not want to hear his own voice at FE_OUT, he should only hear S(t). When converged, or fully adapted, the echo canceller's path estimate EC should be the same as the path response between the microphone and speaker, H. Ideally, none of FE_IN will be perceived at FE_OUT, and so full-duplex hands-free communication is possible.

SYSTEM OVERVIEW

The CS6401 is meant to be used as part of a larger audio-processing system. There are several possible permutations of system configurations that depend to a large degree on the application. Typical applications include: network echo-cancellation of time-division multiplexed PCM data, analog speakerphone, digital speakerphone, and audio for video-conferencing.

A typical connection diagram for the majority of applications is shown in Figure 6. Note that the system requirements will dictate what is connected to the serial ports and boot interface. For example, a telephone network echo-canceller would typically connect the serial port to a network backplane. An analog speakerphone would likely connect the serial port to either two single-channel codecs or one dual-channel codec and it would boot from a ROM. The video-conferencing application may have one serial port connected to a single channel codec, the other serial port connected to a host processor, and boot from the host processor. The configuration depends on the application.

CS6401 SERIAL INTERFACE OVERVIEW

The CS6401 has two serial ports, Synchronous Serial Interface #1 (SSI1) and Synchronous Serial Interface #2 (SSI2), which can be used to interface to a variety of peripherals including popular codecs and DSPs. Each serial port has its own Serial Data Output (SDO), Serial Data Input (SDI), Synchronize Signal (SYNC), and Delayed Synchronize Signal (SYNCO), but both share the common serial bit clock SCLK.

SDO is changed on the rising edge of SCLK while SDI is sampled on the falling edge of SCLK. The SYNC signal may be either a pulse or a frame type depending on the state of the SYNCP pin. This will be explained in greater detail in the discussion of serial modes below. The SYNCO pins are provided for use in Time-Slot Allocation Circuit (TSAC) applications (see serial mode E for details). The SYNCO pin outputs a copy of the SYNC signal received by the CS6401 delayed by 8 SCLK periods. The CS6401 can thus be daisy chained for subsequent time slots on the serial bus given only one external SYNC.

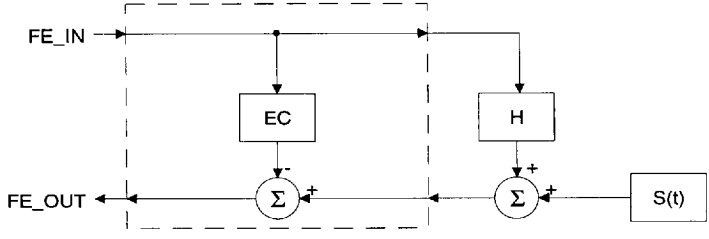

Figure 5. Echo Canceller Path

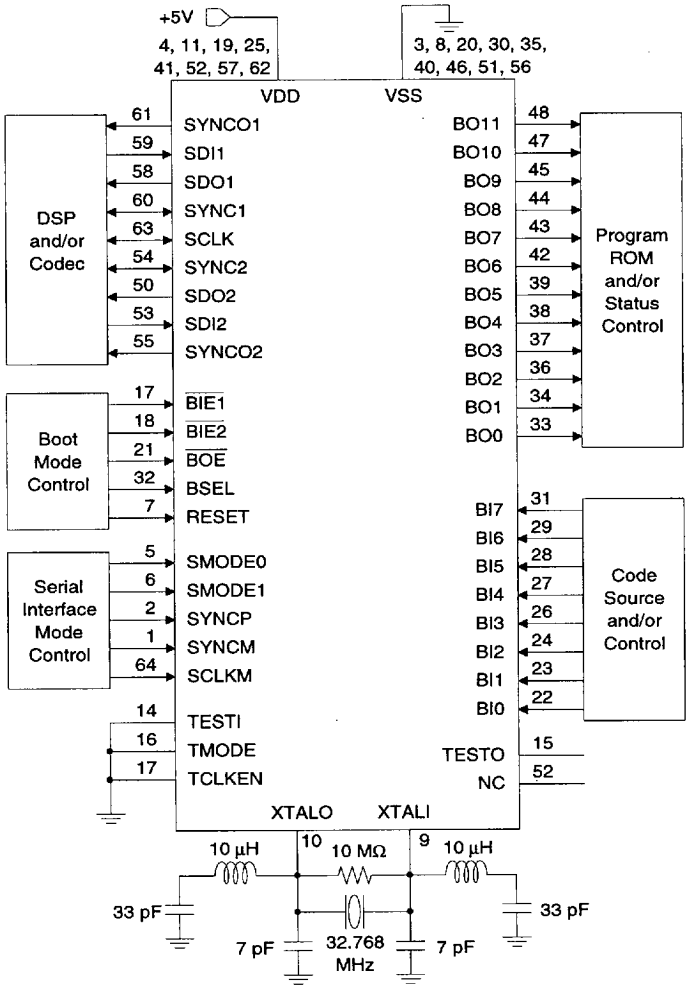

Figure 6. Typical Connection Diagram

The SCLKM pin determines whether or not the CS6401 is the SCLK source. If SCLKM is high, the CS6401 is the SCLK master. Similarly, if SYNCM is high, the CS6401 is the SYNC master. SYNCP determines whether the SYNC signal is a frame-type or a pulse type. If SYNCP is low, the SYNC signal will be a frame-type, high for the valid data bits and low for the remaining bits. If SYNCP is high, the SYNC signal will be a pulse-type. The serial mode determines the polarity of the pulse: SYNC is pulsed low in SM0 and high in SM1. The pulse duration is one SCLK period and the pulse occurs just prior to the start of a frame of serial data (depends on the serial mode, see below).

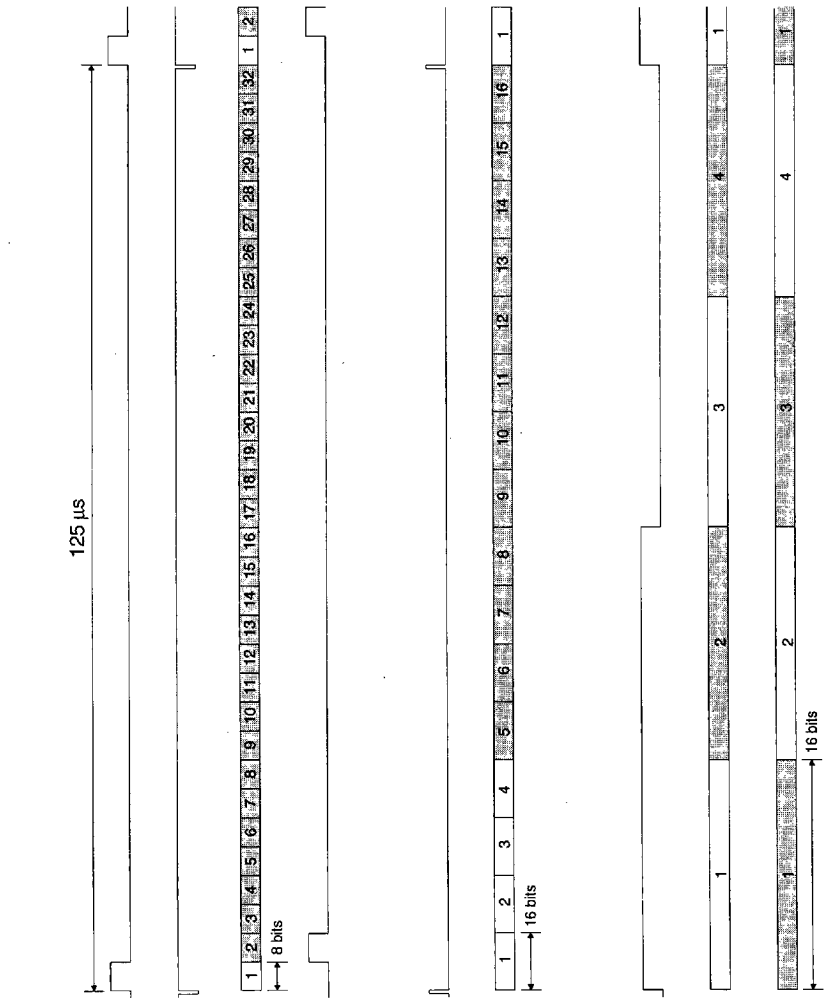

Figure 7. Serial Modes Overview

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CS6401 SERIAL INTERFACE MODES

The CS6401 supports 5 serial port modes. The different serial modes allow connectivity to many popular codecs and DSPs. Serial mode A and serial mode B are 8-bit modes which interface to popular codecs and DSPs. Serial mode C uses SSI2 to interface to Crystal's popular CS4216 dual-channel codec. Serial mode D interfaces to a 16-bit dual-channel codec. Serial mode E is used for 8-bit TSAC interfaces.

Serial Mode:	A	B	C	D	E
SMODE0	0	0	1	0	1
SMODE1	0	0	0	1	1
SCLKM	1	0	1	1	0
SYNCM	1	1/0	1	1	0
SYNCP	0	1	1	0	0
Bits	8	8	16	16	8
Ports	1,2	1,2	2	2	1,2
SYNCO	no	no	no	no	yes

In Serial Mode A, both SSI1 and SSI2 are active. SCLK outputs at 2.048 MHz and SYNC1 and SYNC2 are frame-type synchronization signals (high while the 8-bit data is valid (8 SCLK periods)). The timing relationships for this mode are shown in Figure 8.

Serial Mode B is detailed in Figure 9. SCLK is an input at 2.048 MHz and SYNC1 and SYNC2 are either both inputs or both outputs. The synchronization signals in this mode are the pulse-type: they are always high except for the SCLK period just prior to the 8-bit data being valid.

Serial Mode C, whose timings are shown in Figure 10, is meant to connect to a CS4216 in SM3 in slave mode with 256 bits per frame, sampling at 8 kHz through SSI2. SCLK again outputs a 2.048 MHz clock and can be used as the master clock of the codec. SYNC2 goes high for one SCLK period just prior to the 16-bit stereo data being valid. Note that there is status and control

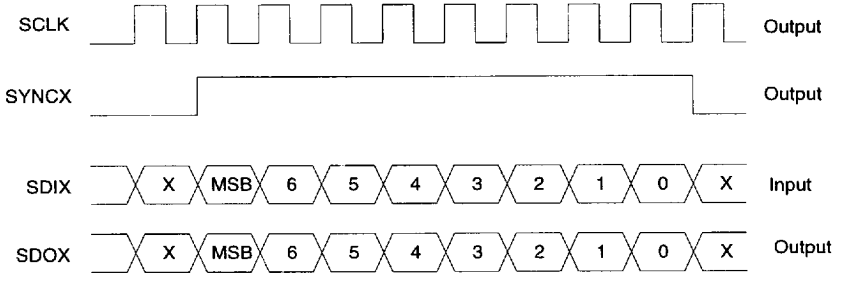


Figure 8. Serial Mode A

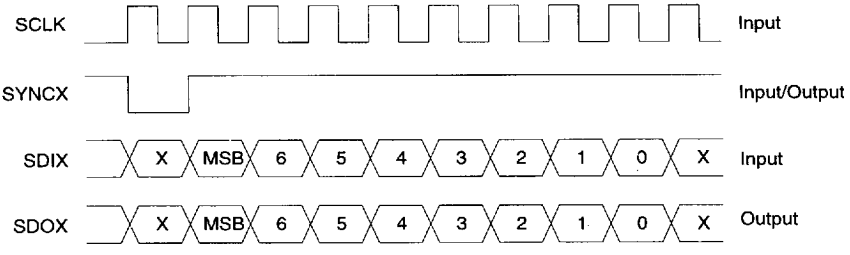


Figure 9. Serial Mode B

data for the CS4216 passed through the serial port as well in this mode. For more information on this Serial Mode, consult the CS4216 data sheet. This mode can be used to implement 64 bit data transfers as long as the timing relationships are maintained (so the CS6401 can communicate with the CS4215 as well).

Figure 11 gives timing relationships for Serial Mode D where SCLK now changes to 512 kHz. SYNC1 provides a 2.048 MHz output that may be used as a master clock. SDI1 and SDO1 are inactive. SYNC2 is an 8 kHz, 50% duty cycle square wave that is high for 16-bit data valid on one channel of a stereo ADC and DAC, and low for the other channel. Note that the first 16 bits of data (after a SYNC2 edge) at SDI2 are valid and the next 16 are ignored. Similarly the first 16 bits of SDO2 should be ignored while the later 16 bits are valid. This mode can be used to interface the CS6401 to the CS5336 ADC and CS4328 DAC.

Serial Mode E is to be used for TSAC applications. In this mode, SCLK and SYNC1 and SYNC2 are all inputs. SCLK should receive a 2.048 MHz clock and SYNC1 and SYNC2 should be frame-type synchronization signals that are high while the data is valid. SYNCO1 and SYNCO2 output the framing signal for the next 8-bit timeslot. This mode is very similar to serial mode A, with the exception of the SYNCO signals and the directions of SCLK and the SYNC signals. The operation of this mode can be seen in Figure 12.

Currently the CS6401 only supports the five modes with SMODE0, SMODE1, SCLKM,

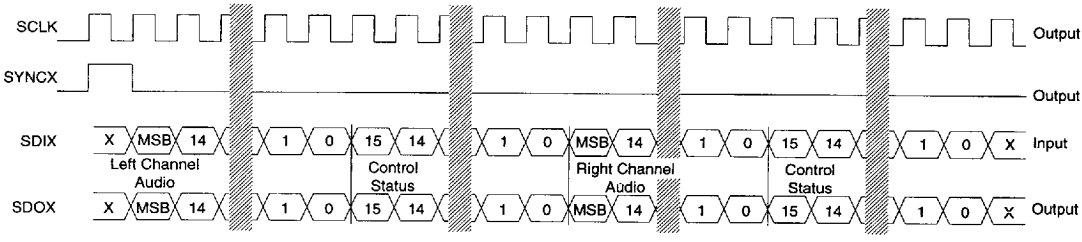


Figure 10. Serial Mode C: CS4216 SM3 Interface

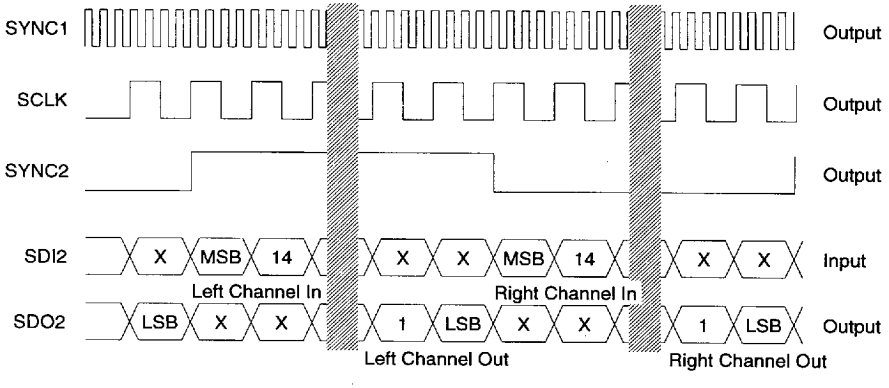


Figure 11. Serial Mode D: 16-bit codec interface

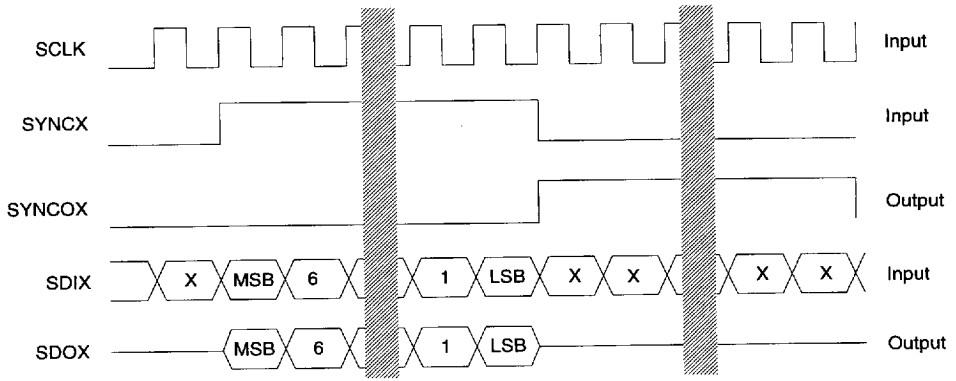


Figure 12. Serial Mode E: 8 bit codec interface

SYNCM, and SYNCP set as indicated. Note that since the CS6401 is programmable, the way it interprets what it reads from or writes to the serial ports is also programmable. If further flexibility is desired, please contact Crystal.

CS6401 BOOT INTERFACE OVERVIEW

The CS6401 has a very flexible boot interface which loads user code into its Program RAM. The CS6401 may be booted in either parallel mode, with 8 bits of instruction presented to BI0-7, or serial mode with serial data presented to BI7. The boot interface is configured using the BSEL, $\overline{\text{BIE1}}$, $\overline{\text{BIE2}}$, and $\overline{\text{BOE}}$ pins. The state of the BIE pins determine whether or not the CS6401 is master of the boot process. If either $\overline{\text{BIE1}}$ and $\overline{\text{BIE2}}$ are high after reset, the CS6401 boot interface is slaved to an external memory source such as a DSP or microcontroller. In this case, the data presented to the BI0-7 pins (parallel boot) or BI7 (serial boot) is latched on the falling edge of $\overline{\text{BIE1}}$ or $\overline{\text{BIE2}}$.

In the stand alone parallel boot mode (chosen when BSEL, $\overline{\text{BIE1}}$, and $\overline{\text{BIE2}}$ are low), the CS6401 clears all the BO pins after reset. The BO pins register the address in the parallel EPROM that the CS6401 is to boot from. The outputs from the EPROM should present their data to BI0-7. It is recommended that BO0 be used as an active-low chip select for the EPROM. In this manner the CS6401 can load 766 words of 16-bit instructions into its Program RAM one byte at a time by incrementing the address presented at BO1-11 and sampling the data at BI0-7 on the falling edge of BO0.

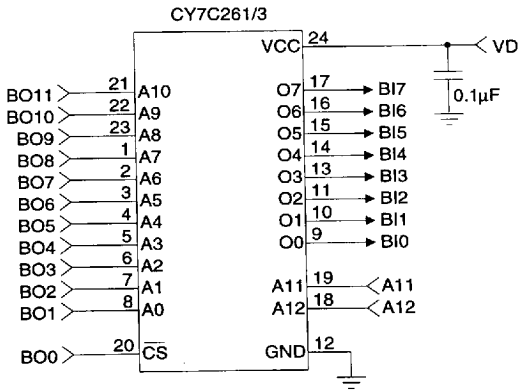


Figure 13. Standalone parallel boot from 8k EPROM

In the stand alone serial boot mode (differentiated from the previous mode by setting BSEL high), the CS6401 latches the data presented at BI7 on the falling edge of BO0. BO0 is connected to the clock input of the serial EPROM and BI7 is connected to the data output. The reset signal for the serial EPROM should be common with the CS6401 reset signal. The first rising edge of BO0 causes the first bit from the EPROM to be present at BI7. This bit is latched on the falling edge of BO0 and becomes the most significant bit of the first 16-bit word. After 16 bits are loaded, that word is loaded into the Program RAM, and the next 16 bits are loaded.

The boot modes where the CS6401 is the slave are very similar to the standalone modes except that the data is latched on the falling edge of either $\overline{\text{BIE}}$ pin. The BOx pins still drive out the addresses for a ROM, but these are generally ignored by the boot master. It is important to make sure that a ROM is not selected at this time, though, in order to avoid bus-contention problems. Note that the CS6401 begins executing as soon as it receives 1532 bytes of instructions.

Two $\overline{\text{BIE}}$ pins are provided to allow simultaneous booting of multiple CS6401s. In this case, one CS6401 is selected as the boot master and the rest as boot slaves. The BO0 of the master is fed to the $\overline{\text{BIE2}}$ of the slaves and the BIs are all ganged together. The master controls the EPROM accesses and all data is accessed at the same time via BO0/$\overline{\text{BIE2}}$. Simultaneous booting is possible in both serial and parallel modes. If the code source is a DSP or microcontroller, there will only be slave CS6401s.

Setting the $\overline{\text{BOE}}$ pin causes the BO pins to become high impedance. This pin can be used to

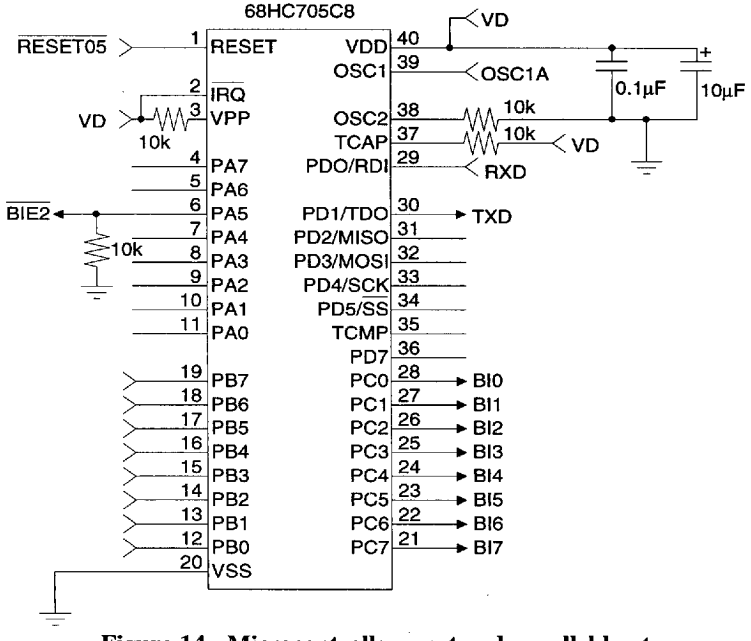
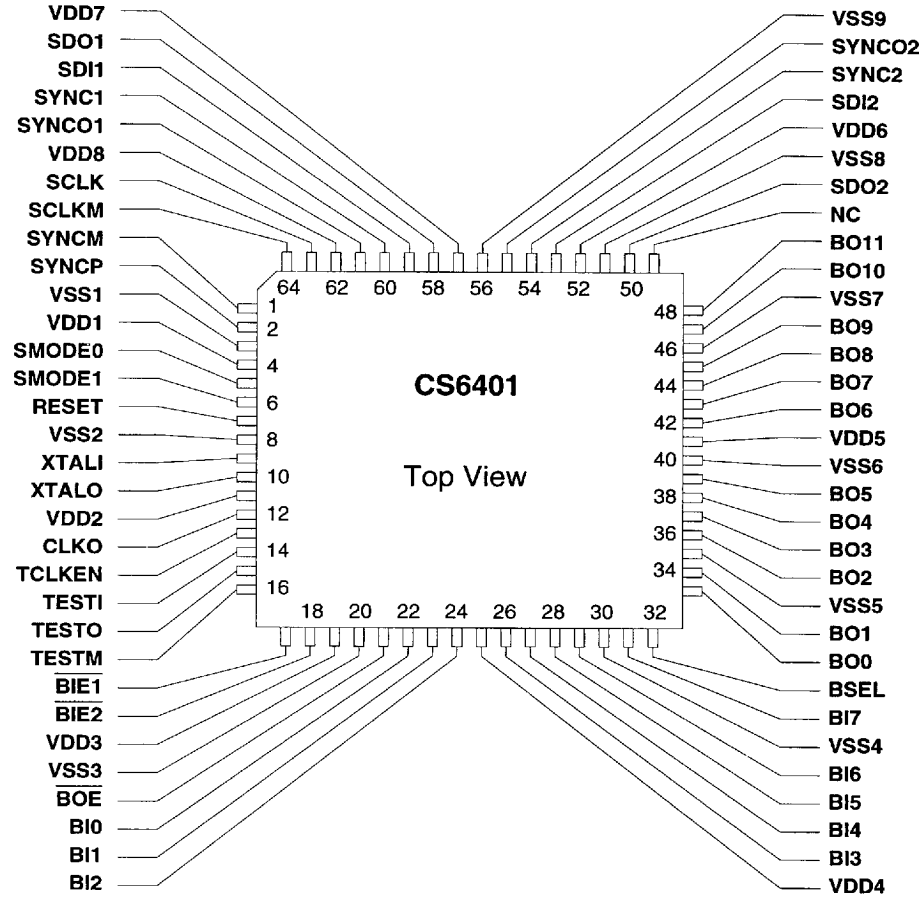


Figure 14. Microcontroller mastered parallel boot (See CDB6401 for more details).

allow a CS6401 to share a bus with another chip. When $\overline{BOE}$ is low, the BO pins are enabled and will act as outputs.

The boot sequence can be initiated either by re-setting the CS6401 or by a software call. The software call option is useful if the user wishes to boot different sets of code.

PIN DESCRIPTIONS



Power Supply Connections

VDD1 - VDD8 – Pins 4, 11, 19, 25, 41, 52, 57 and 62
+5V power supply pins

VSS1 - VSS9 – Pins 3, 8, 20, 30, 35, 40, 46, 51 and 56
0V ground pins

RESET - Active High Reset Input, Pin 7
Resets the AFP and serial ports when high. All RAM is unaffected. Fall of RESET initiates the boot process.

XTALI, XTALO - Crystal Input and Output, Pins 9 and 10

Input and output connections for 32.768 MHz crystal. Alternately, an external clock fed into XTALI may clock the CS6401.

CLKO - Master Clock Output, Pin 12

CLKO is Master Clock output, whose freqency is half that of the signal at XTALI. CLKO is always active while the chip is powered and clocked.

Serial Interface Pins

SDO1, SDO2 - Port 1 and Port 2 Serial Data Output, Pins 58 and 50

Data is output from serial port 1 and serial port 2 of the CS6401 via these pins.

SDI1, SDI2 - Port 1 and Port 2 Serial Data Input, Pins 59 and 53

Data is input to serial port 1 and serial port 2 of the CS6401 via these pins.

SYNC1, SYNC2 - Port 1 and Port 2 Synchronization Signal, Pins 60 and 54

Used to indicate the start of a word of serial data on serial port 1 and serial port 2.

SYNCO1, SYNCO2 - Port 1 and Port 2 Delayed Synchronization Output, Pins 61 and 55

Provides a SYNC signal delayed by 8 SCLK periods for TSAC applications. Active in serial mode 3.

SCLK - Serial Port Bit Clock, Pin 63

SCLK controls the digital data on SDO1 and SDO2 and latches the data on SDI1 and SDI2. SCLK is low while RESET is high.

SCLKM - Serial Clock Mode Select, Pin 64

SCLKM high makes the CS6401 output SCLK. SCLKM low makes the CS6401 slave to a supplied SCLK.

SYNCM - Synchronization Mode Select, Pin 1

SYNCM high makes the CS6401 output SYNC1 and SYNC2. SYNCM low makes the CS6401 accept external SYNC signals as inputs.

SYNCP - Synchronization Pulse Mode Select, Pin 2

SYNCP high makes the CS6401 produce a SYNC pulse of one SCLK period duration just prior to the start of a new word of data. SYNCP low makes the CS6401 frame each word with SYNC high while data is valid.

SMODE0, SMODE1 - Serial Mode Selects, Pins 5 and 6

Select the serial mode format of the data input to and output from the serial ports.

Boot/Control/Status Interface Pins

$\overline{\text{BIE1}}$, $\overline{\text{BIE2}}$ - Boot Interface Enables, Pins 17 and 18
After reset if either $\overline{\text{BIEx}}$ pin is low the Boot Interface is self-clocking, else it is slaved (to $\overline{\text{BIE1}}$ or $\overline{\text{BIE2}}$).

$\overline{\text{BOE}}$ - Boot Output Enable, Pin 21
Boot outputs are low impedance when low.

BI0-BI7 - Boot Inputs, Pins 22, 23, 24, 26, 27, 28, 29 and 31
Parallel or serial boot data input from EPROM and general purpose input after boot.

BO0-BO11 - Boot Outputs, Pins 33, 34, 36, 37, 38, 39, 42, 43, 44, 45, 47 and 48
Parallel boot address word for parallel EPROM, serial boot clock or output enable, and general purpose output after boot.

BSEL - Boot Mode Select, Pin 32
When BSEL is high, a serial boot is selected. When BSEL is low, a parallel boot is selected.

Test Interface Pins

TESTI - Scan Test Input, Pin 14
Keep grounded.

TESTO - Scan Test Output, Pin 15
Keep unconnected.

TESTM - Test Mode Select, Pin 16
Keep grounded.

TCLKEN - Test Clock Enable, Pin 13
Keep grounded.