

S G S-THOMSON

T-52-13-45

L6212

# HIGH CURRENT SOLENOID DRIVER

■ HIGH VOLTAGE OPERATION (UP TO 50 V)

- HIGH OUTPUT CURRENT CAPABILITY (UP TO 6 A)
- LOW SATURATION VOLTAGE
- TTL-COMPATIBLE INPUT
- OUTPUT SHORT CIRCUIT PROTECTION (TO GROUND, TO SUPPLY AND ACROSS THE LOAD)
- THERMAL SHUTDOWN
- OVERDRIVING PROTECTION
- LATCHED DIAGNOSTIC OUTPUT

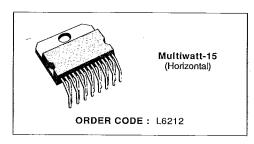
### DESCRIPTION

The L6212 is a monolithic switch-mode solenoid driver designed for fast, high-current applications such as hammer driving in printers and electronic typewriters. Power dissipation is reduced by efficient

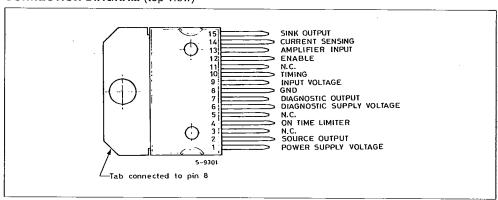
# PRELIMINARY DATA

switch-mode operation. An extra feature of the L6212 is a latched diagnostic output which indicates when the output is short circuit.

The L6212 is supplied in an 15-lead Multiwatt plastic power package.



## **CONNECTION DIAGRAM** (top view)

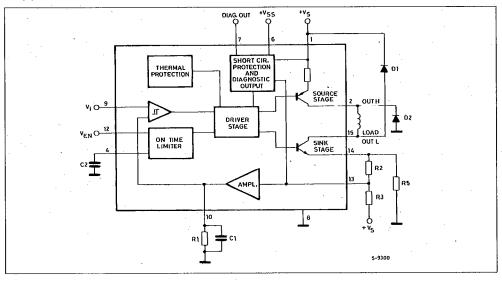


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## **BLOCK DIAGRAM**



# **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit	
Vs	Power Supply Voltage	50	V	
Vss	Logic Supply Voltage	7	V	
V <sub>EN</sub>	Enable Voltage	7	V	
VI	Input Voltage	7	V	
l <sub>p</sub>	Peak Output Current (repetitive)	6.5	А	
Ptot	Total Power Dissipation (at T <sub>case</sub> = 75 °C)	25	W	
T <sub>sta</sub> , T <sub>i</sub>	Storage and Junction Temperature	- 40 to + 150	°€	

### **THERMAL DATA**

R <sub>th i-case</sub>	Thermal Resistance Junction-case	Max	3	°C/W
R <sub>th i-amb.</sub>	Themal Resistance Junction-ambient	Max	35	°C/W

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**ELECTRICAL CHARACTERISTICS** (refer to the test circuit,  $V_s = 37$  V,  $V_{ss} = 5$  V,  $T_{amb} = 25$  °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Vs	Power Supply Voltage (pin 1)		12		46	٧
ld	Quiescent Drain Current	V <sub>EN</sub> = H	-	20	30	mA
		V <sub>i</sub> ≥ 0.6 V V <sub>EN</sub> = L		70		mA
V <sub>ss</sub>	Logic Supply Voltage (pin 6)		4.5		7	٧
Iss	Quiescent Logic Supply Current	V <sub>DIAG</sub> = L		5	8	mA
	•	DIAG Output at High Impedance		10	100	μΑ
Vi	Input Voltage (pin 9)	Operating Output	0.6			٧
		Non-operative Output		:	0.45	٧
l <sub>ī</sub>	Input Current (pin 9)	$V_i \ge 0.6 \text{ V} \\ V_i \le 0.45 \text{ V}$			–2 –5	μA μA
VENABLE	Enable Input Current (pin 12)	Low Level High Level	-0.3 2.4		0.8	٧
JENABLE	Enable Input Current	$V_{EN} = L$ $V_i = 0.8 \text{ V}$ $V_{EN} = H$ $V_e = 2.4 \text{ V}$			-100 100	μ <b>A</b>
V <sub>sat H</sub>	Source Output Saturation Volt.	I <sub>P</sub> = 5.5 A			2.5	٧
V <sub>sat L</sub>	Sink Output Saturation Volt.	l <sub>out</sub> = 5.5 A			2.5	٧
V <sub>sat H</sub> + V <sub>sat L</sub>	Total Saturation Voltage	l <sub>out</sub> = 5.5 A			4.5	V
l <sub>leakage</sub>	Output Leakage Current Source PNP	$V_s = 45 \text{ V} $ $V_i \le 0.45 \text{ V}$			2	mA
l <sub>ieakage</sub>	Output Leakage Current Sink NPN	$V_s = 45 \text{ V} $ $V_i \le 0.45 \text{ V}$			2	mA
K	On Time Limiter Constant (*)	V <sub>EN</sub> = L		120		
V <sub>DIAG</sub>	Diagnostic Saturation Voltage (pin 7)	I <sub>DIAG</sub> = 10 mA			0.4	٧
IDIAG	Diagnostic Leakage Current (pin 7)	V <sub>DIAG</sub> = 40 V			10	μА
V <sub>pin 10</sub>	OP AMP DC Voltage Gain	V <sub>pin 13</sub> = 100 to 800 mV		5		
V <sub>pin 13</sub>						
V <sub>pin 10</sub>		I <sub>pin 10</sub> = 1 mA	4.5			V
lpin 10		$\begin{array}{c} V_{pin \ 10} = 4 \ V \ V_{9} = V_{13} = 0 \\ V_{pin \ 10} = 2 \ V \ V_{13} = 0.9 \ V \end{array}$	1		10 1.5	μA mA
I <sub>sense</sub>	Input Bias Current (pin 13)			-1		μA
V <sub>sense</sub>	Sensing Voltage (pin 14) (**)				0.9	V

After a time interval t<sub>max</sub> = KC<sub>2</sub>, the output stages are disabled.

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<sup>(\*)</sup> After a time interval  $t_{max}$  =  $KC_2$ , the output stages are disauled. (\*\*) Allowed range of  $V_{\text{ente}}$  without the intervention of the short circuit protection.



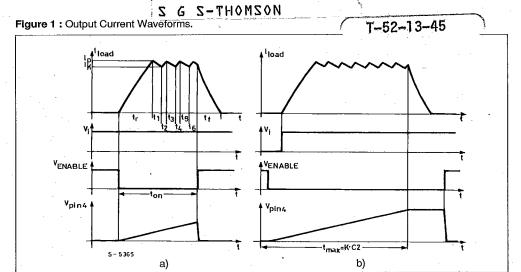
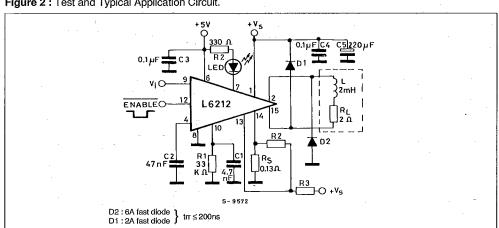


Figure 2: Test and Typical Application Circuit.



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#### CIRCUIT OPERATION

The L6212 works as a transconductance amplifier: it can supply an output current directly proportional to an input voltage level (Vi). Furthermore, it allows complete switching control of the output current waveform (see Fig. 1).

The following explanation refers to the Block Diagram, to Fig. 1 and to the typical application circuit of Fig. 2.

The t<sub>on</sub> time is fixed by the width of the Enable input signal (TTL compatible): it is active low and enables the output stages "source" and "sink". At the end of t<sub>on</sub>, the load current I<sub>load</sub> recirculates through D1 and D2, allowing fast current turn-off.

The rise time t<sub>r</sub> depends on the load characteristics, on V<sub>1</sub> and on the supply voltage value (V<sub>s</sub>, pin 1).

During the  $t_{on}$  time  $l_{load}$  is converter into a voltage signal by means of the external sensing resistance  $R_s$  connected to pin 13. This signal, amplified by the op amp charges the external RC network at pin 10 (R1, C1). The voltage at this pin is sensed by the inverting input of a comparator. The voltage on the non-inverting input of this one is fixed by the external voltage  $V_l$  (pin 9).

After,  $t_r$ , the comparator switches and the output stage "source" is switched off. The comparator output is confirmed by the voltage on the non-inverting input, which decreases of a constant fraction of  $V_i$  (1/10), allowing hysteresis operation. The current in the load now flows through D2.

Two cases are possible: the time constant of the recirculation phase is higher than R1, C1; the time constant is lower than R1, C1. In the first case, the voltage sended on the non-inverting input of the comparator is just the value proportional to  $l_{load}$ . In the second case, when the current decreases too quickly, the comparator senses the voltage signal stored in the R1, C1 network.

In the first case  $t_1$  depends on the load characteristics, while in the second case it depends only on the value of R1, C1.

In the other word, R1, C1 fixed the minimum value of  $t_1$  ( $t_1 \ge 1/10$  R1 x C1. Note that C1 should be chosen in the range 2.7 to 10 nF for stability reasons of the op amp).

After  $t_1$ , the comparator switches again : the output is confirmed by the voltage on the non-inverting input, which reaches  $V_i$  again (hysteresis).

Now the cycle starts again:  $t_2$ ,  $t_4$  and  $t_6$  have the same characteristics as  $t_r$ , while  $t_3$  and  $t_5$  are similar

to  $t_1$ . The peak current  $I_p$  depends on  $V_i$  as shown in the typical transfer function of Fig. 3.

It can be seen that for  $V_i$  lower than 450 mV the device is not operating.

For  $V_{i}$  included between 450 and 600 mV, the operation is not guaranteed.

The other parts of the device have protection and diagnostic functions. At pin 4 is connected an external capacitor C2, charged at constant current when the Enable is low.

After time interval equal to K  $\cdot$  C1 (K is defined in the table of Electrical Characteristics and has the dimensions of  $\Omega$ ) the output stages are switched off independently by the Input signal.

This avoids the load being driven in construction for an excessive period of time (overdriving protection).

The action of this protection is shown in Fig. 1b. Note that the voltage ramp at pin 4 starts whenever the Enable signal becomes active (low state), regardless of the Input signal. To reset pin 4 and to restore the normal conditions, pin 12 must return high. This protection can be disabled by grounding pin 4.

In order to keep constant the energy delivered to the load, when the supply voltage changes, it's possible to modify the output maximum peak current ( $I_p$ ) by means the external voltage divider R2 and R3 which "senses" the supply voltage.

 $I_p$  is given by :

$$I_{p} = \frac{V_{i} (R_{s} + R2 + R3) - 5 V_{s} (R2 + R_{s})}{5 R3 R_{s}}$$

so the variation of  $l_p$  versus  $V_s$  is :

$$\Delta I_p = -\frac{R2 + R_s}{R3 R_s}$$

The thermal protection included in the L6212 has hysteresis.

It switches off the output stages whenever the junction temperature increases too much. After a fall of about 20°C, the circuit starts again.

Finally, the device is protected against any type of short circuit at the outputs: to ground, to supply and across the load.

When the source stage current is higher than 7A and/or when the pin 13 voltage is higher then 1 V (i.e. for a sink current greater than 1 V/R<sub>s</sub>) the output stages are switched off and the device is inhibited.

This condition is indicated at the open-collector output DIAG (pin 7); internal flip-flop F/F changes and forces the output transistor into saturation. The F/F

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After that, two cases are possible : the reason for the "bad operation" is till present and the protection acts again; the reason has been removed and the device starts to work properly.

Figure 3: Peak Output Current vs. Input Voltage.

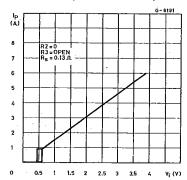


Figure 4: Peak Output Current vs. Input Voltage.

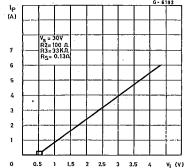
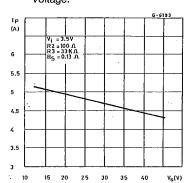


Figure 5: Peak Output Current vs. Supply Voltage.



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