L64016
L64017
16-Bit HCMOS Multipliers
Preliminary

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Description

The L64016 and L64017 are high speed 16×16-bit multipliers with on-chip scan testing. The L64016 has independent clocks for the X, Y, MSP and LSP registers. The L64017 has a single master clock and three register enables for the X, Y, and full product register, facilitating use in microprogrammed systems. The 1.5-micron drawn gate length HCMOS (0.9-effective) results in very high speed operation with low power dissipation.

These devices are useful in Digital Signal Processing (DSP) applications such as Fast Fourier Transforms (FFTs), digital filtering, correlations and power expansions. They are also useful for general computational tasks such as graphics processing, image processing and vector processing operations.

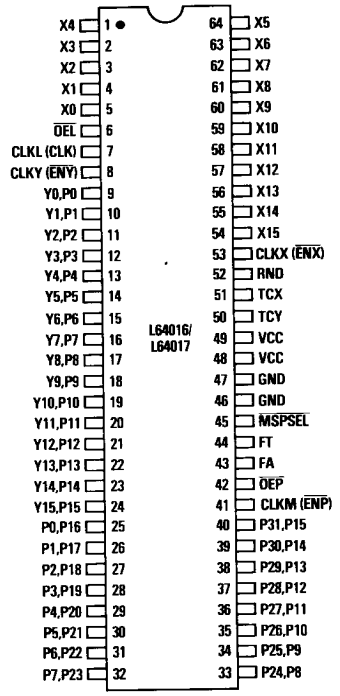
In the 68-pin versions, the L64016 and L64017 contain on-chip scan testing. Normally non-connected pins are used for scan input, scan output and scan enable. Serial scan is useful for board and system level testing and maintenance schemes. During scan mode, test data can be serially shifted into the on-chip registers, the chip exercised and the resulting data serially shifted out. Upon evaluation of the data, a faulty chip can be easily isolated and replaced. Serial scan is used on all LSI Logic L64000 series devices as well as most ASIC megacells and memories. This allows consistent testing across all devices on a board.

Features

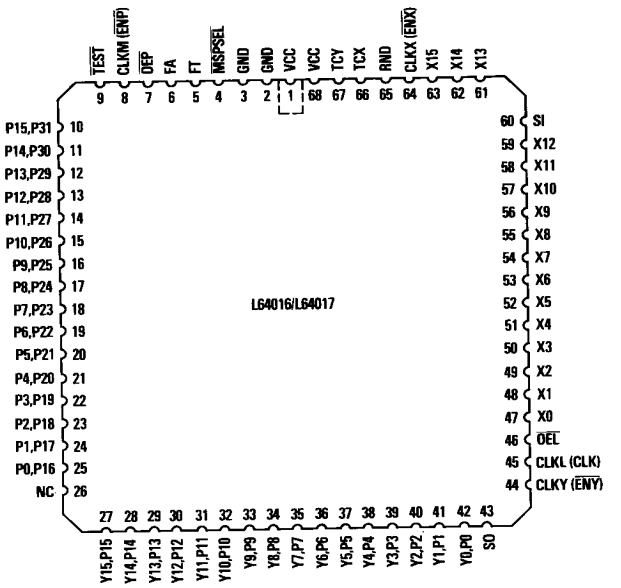
- 16 × 16-bit parallel multiplication with full precision 32-bit product output.
- Fast clock cycle times
  - L64016/17: 40 ns commercial, 50 ns military
  - L64016A/17A: 30 ns commercial, 40 ns military
- Two's complement, unsigned or mixed mode operations
- Pin compatible with AM29516/17, Cypress CY7C516 and TRW MPY016K
- Serial scan capability for X, Y and product registers on 68-pin packages
- Over 2001 V ESD protection, over 200 mA latchup protection
- Available in 64-pin CDIP, 68-pin PLDCC, 68-pin CLCC and 68-pin CPGA packages

Pin Diagrams (Top View)

64-Pin CDIP



68-Pin LCC



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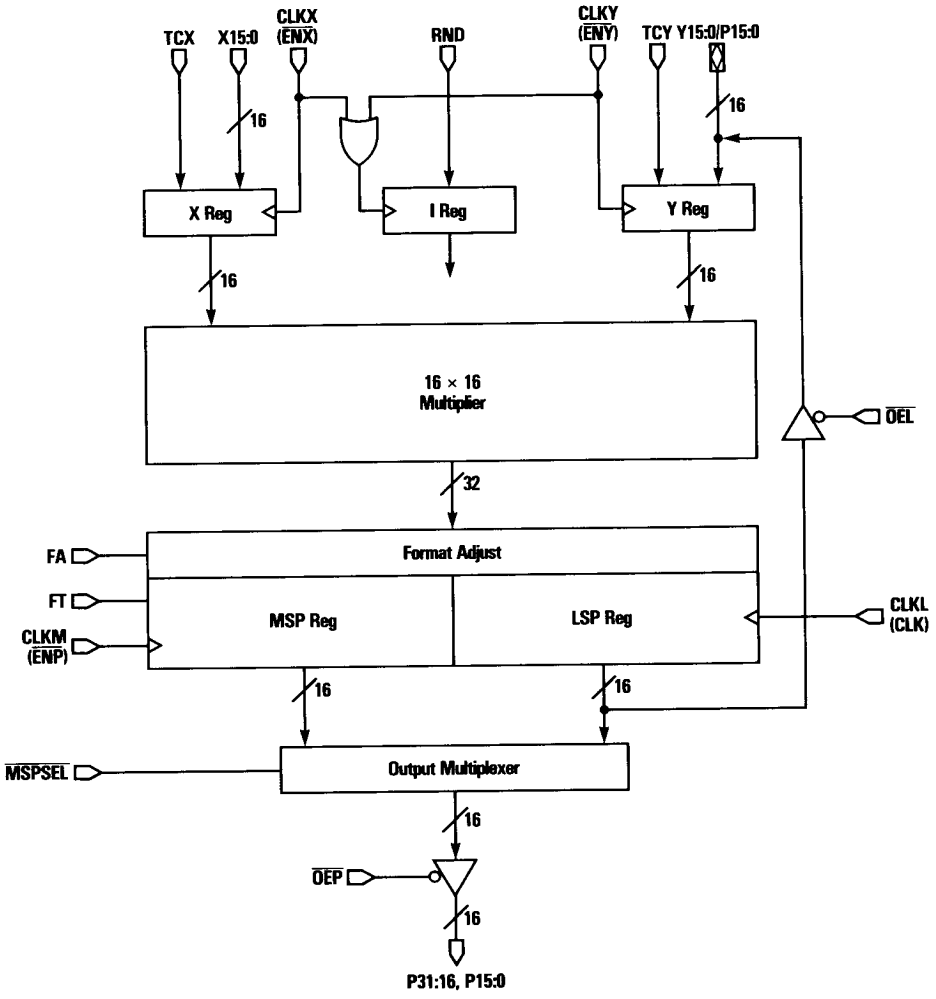
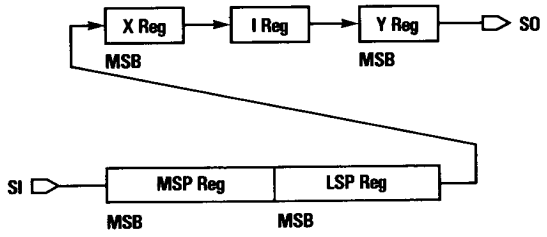
Order Number L64016

Logic Block Diagram
Normal Operation
($\overline{TEST}$ = HIGH for
68-Pin Package)



Note: Pin designations for L64017 are shown in parentheses.

Logic Diagram—Scan Chain
($\overline{TEST}$ = LOW, FT = LOW)
68-Pin Packages Only



Notes:
1. I register is the RND input.
2. Register clocks act as scan clocks.
3. For L64016, apply CLKY at or before CLKX. Apply CLKX at or before CLKL and CLKL at or before CLKM.
4. For L64017 enable all registers. CLK acts as single clock for all scan registers.
5. Scan data in the MSP and LSP registers can only be observed on the outputs if FT = LOW.

X and Y Data Input Formats

Unsigned Integer (TCX or TCY=0)

15	14	13	•••	2	1	0
2^{15}	2^{14}	2^{13}	•••	2^{2}	2^{1}	2^{0}

Two's Complement Integer (TCX or TCY=1)

15	14	13	•••	2	1	0
-2^{15}	2^{14}	2^{13}	•••	2^{2}	2^{1}	2^{0}
(Sign)						

Unsigned Fractional (TCX or TCY=0)

15	14	13	•••	2	1	0
2^{-1}	2^{-2}	2^{-3}	•••	2^{-14}	2^{-15}	2^{-16}

Two's Complement Fractional (TCX or TCY=1)

15	14	13	•••	2	1	0
-2^{0}	2^{-1}	2^{-2}	•••	2^{-13}	2^{-14}	2^{-15}
(Sign)						

Two's Complement and Unsigned numbers can be multiplied together in mixed mode operations.

Numerical Output Formats

Unsigned Integer Output (FA=1)

MSP															LSP														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Two's Complement Integer Output (FA=1)

MSP															LSP														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(Sign)																															

Unsigned Fractional Output (FA=1)

MSP															LSP														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Two's Complement Fractional Output (FA=1)

MSP															LSP														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
(Sign)																															

Fractional Two's Complement (FA=0) (Shifted*)

MSP															LSP														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	-2^{0}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
																(Sign)															

*In shifted fractional two's complement format an overflow results when 1.000 ••• is multiplied by 1.000 ••• (-1 times -1). The product of this operation is 1.000 ••• (-1).

Pin Listing and Description

L64016/L64017

X15:0
16-bit data input. Data are loaded into the X register on the rising edge of CLKX for the L64016 or on the rising edge of CLK when $\overline{ENX}$ is LOW for the L64017.

X15:0/P15:0
16-bit data input/output. When $\overline{OEL}$ is HIGH, this port acts as the Y data input. Data are loaded on this input on the rising edge of CLKY for the L64016 or on the rising edge of CLK when $\overline{ENY}$ is LOW for the L64017.

When $\overline{OEL}$ is LOW this port acts as a data output for the LSP (P15:0).

P31:16/P15:0
16-bit multiplexed data output. When $\overline{MSPSEL}$ is LOW, the MSP (P31:16) is available on this output. When $\overline{MSPSEL}$ is HIGH, the LSP (P15:0) is available on this output. In both cases $\overline{OEP}$ must be HIGH.

FT
Feedthrough. Both the MSP and LSP registers become transparent when FT is HIGH.

FA
Format Adjust. When FA is HIGH, a proper 32-bit product is output. When FA is LOW, a left shifted product is output with the sign bit replicated in the MSB of the LSP. FA must be HIGH for two's complement integer, unsigned magnitude and mixed mode multiplication.

$\overline{MSPSEL}$
MSP Select Multiplexer Control. When $\overline{MSPSEL}$ is LOW, the MSP (P31:16) is available at the P31:16/P15:0 output port and the LSP is available at the Y15:0/P15:0 port. When $\overline{MSPSEL}$ is HIGH, the MSP is unavailable while the LSP is available at both the P31:16/P15:0 and the Y15:0/P15:0 ports.

RND
When RND is HIGH a "1" is added to the MSB of the LSP. This position is located at P15 when FA = HIGH and P14 when FA = LOW.

TCX
Two's Complement X. X input data are interpreted as two's complement when TCX is HIGH and as unsigned magnitude when TCX is LOW.

TCY
Two's Complement Y. Y input data are interpreted as two's complement when TCY is HIGH and as unsigned magnitude when TCY is LOW.

$\overline{OEP}$
P31:16/P15:0 Output Enable. The P31:15/P15:0 output port is enabled when $\overline{OEP}$ is LOW, otherwise the output is placed in high impedance.

$\overline{OEL}$
Y15:0/P15:0 Output Enable. When $\overline{OEL}$ is LOW, Y15:0/P15:0 is enabled for P15:0 output data. When $\overline{OEL}$ is HIGH Y15:0/P15:0 function as the input port for Y15:0 data.

L64016 Only

CLKX
X register clock. X15:0 and TCX are loaded at the rising edge of CLKX.

CLKY
Y register clock. Y15:0 and TCY are loaded at the rising edge of CLKY.

CLKM
MSP register clock. MSP (Most Significant Product) data are loaded into the MSP register at the rising edge of CLKM.

CLKL
LSP register clock. LSP (Least Significant Product) data are loaded into the LSP register at the rising edge of CLKL.

L64017 Only

CLK
Clock. All enabled register data are loaded at the rising edge of CLK.

$\overline{ENX}$
X-Register Enable. When $\overline{ENX}$ is LOW, X15:0 and TCX will be loaded at the rising edge of CLK. When $\overline{ENX}$ is HIGH, the X registers are disabled.

$\overline{ENY}$
Y-Register Enable. When $\overline{ENY}$ is LOW Y15:0 and TCY will be loaded at the rising edge of CLK. When $\overline{ENY}$ is HIGH, the Y registers are disabled.

$\overline{ENP}$
Product Register Enable. When $\overline{ENP}$ is LOW both the MSP and LSP can be loaded at the rising edge of CLK. When $\overline{ENP}$ is HIGH, the product register is disabled.

Pin Listing and Description (Continued)

68-Pin Package Only
(both L64016 and L64017)

$\overline{\text{TEST}}$
TEST mode enable. When $\overline{\text{TEST}}$ is LOW, the MSP, LSP, RND, X, I, and Y registers all operate as a single large serial shift register for the shifting of test data into the device. Scan registers are clocked via the normal input clocks for each set of registers.

SI, SO
Scan Input and Scan Output for the scan chain during test mode.

AC Switching Characteristics: Commercial Temperature Range (TA = 0°C to 70°C, VDD = 4.75V to 5.25V) $\overline{TEST}$ = HIGH for 68-pin packages

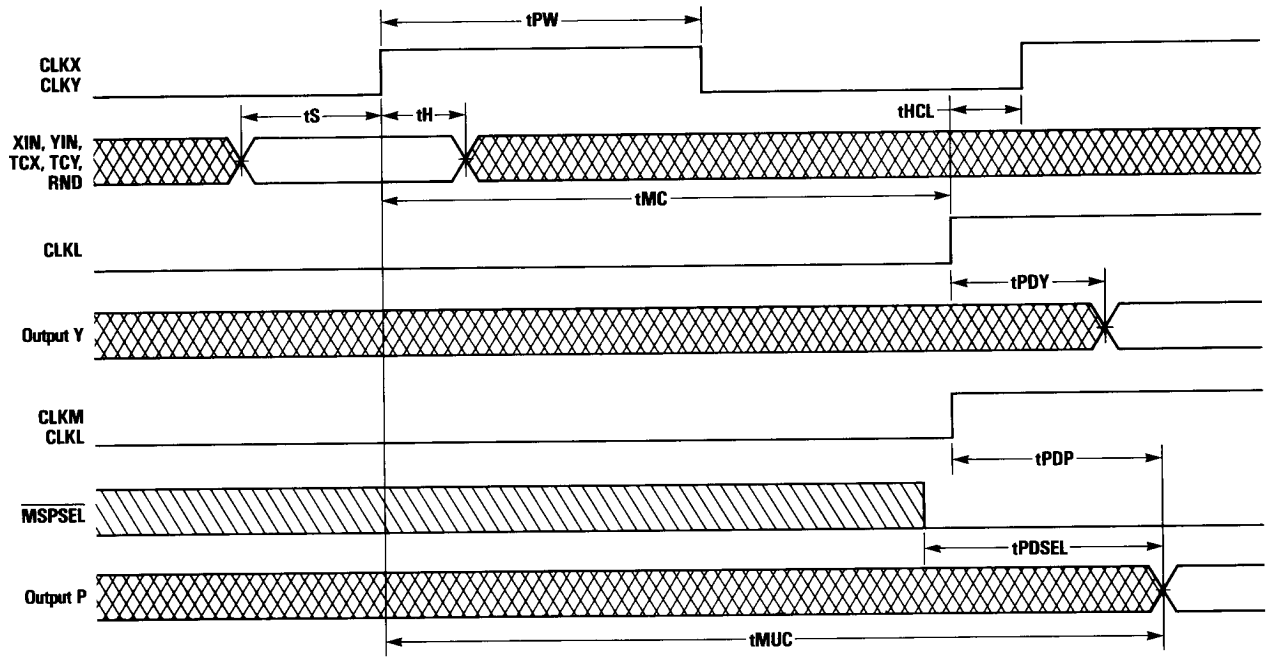
Symbol	Parameter	L64016A/17A		L64016/17		Units
		Min	Max	Min	Max	
tMUC	Unclocked Multiply Time		45		60	ns
tMC	Clocked Multiply Time		30		40	ns
tS	X, Y, RND, TCX, TCY Set-Up Time	7		10		ns
tH	X, Y, RND, TCX, TCY Hold Time	3		3		ns
tSE	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Set-Up Time (L64017 Only)	7		10		ns
tHE	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Hold Time (L64017 Only)	3		3		ns
tPW	Clock Pulse Width	15		20		ns
tPDSEL	$\overline{MSPSEL}$ to Product Out		15		20	ns
tPDP	Output Clock to P		20		25	ns
tPDY	Output Clock to Y		20		25	ns
tOZ	Output Disable Time		15		20	ns
tOE	Output Enable Time		15		20	ns
tHCL	Clock Low Hold Time CLKXY Relative to CLKML[1]	0		0		ns

AC Switching Characteristics: Military Temperature Range (TC = −55°C to 125°C, VDD = 4.5V to 5.5V) $\overline{TEST}$ = HIGH for 68-pin packages

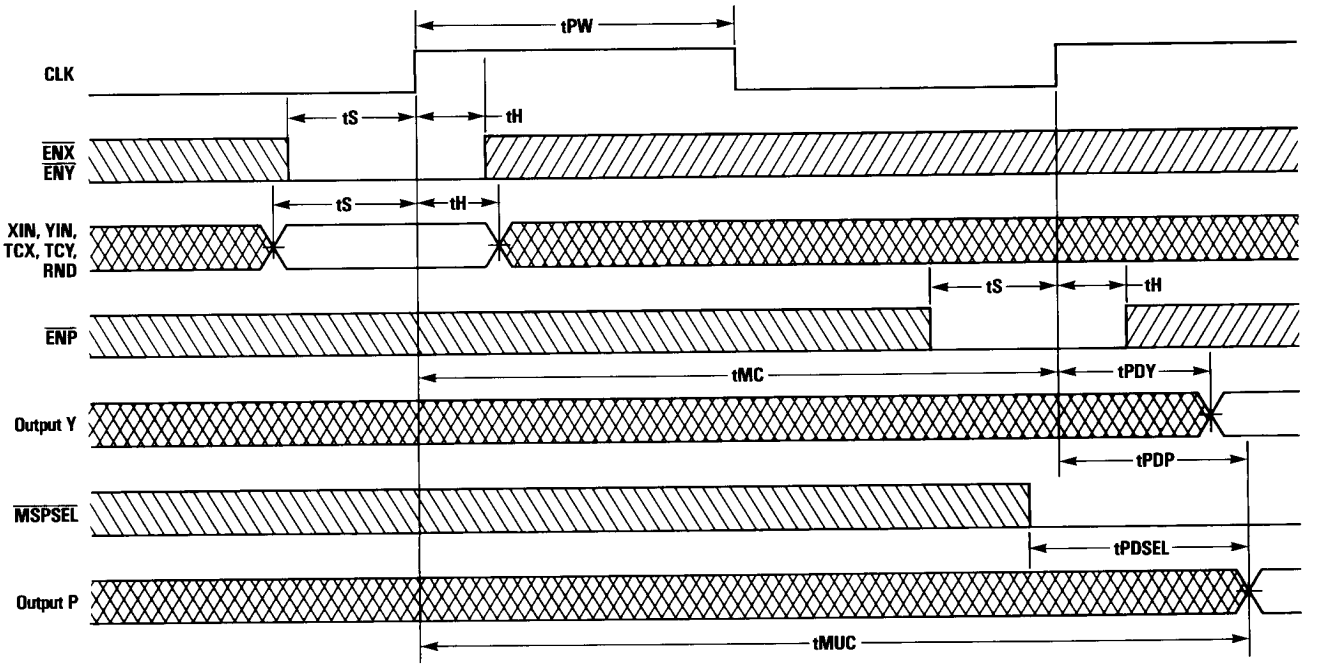
Symbol	Parameter	L64016A/17A		L64016/17		Units
		Min	Max	Min	Max	
tMUC	Unclocked Multiply Time		60		70	ns
tMC	Clocked Multiply Time		40		50	ns
tS	X, Y, RND, TCX, TCY Set-Up Time	10		15		ns
tH	X, Y, RND, TCX, TCY Hold Time	5		5		ns
tSE	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Set-Up Time (L64017 Only)	10		15		ns
tHE	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Hold Time (L64017 Only)	5		5		ns
tPW	Clock Pulse Width	20		25		ns
tPDSEL	$\overline{MSPSEL}$ to Product Out		20		25	ns
tPDP	Output Clock to P		25		30	ns
tPDY	Output Clock to Y		25		30	ns
tOZ	Output Disable Time		20		25	ns
tOE	Output Enable Time		20		25	ns
tHCL	Clock Low Hold Time CLKX, CLKY Relative to CLKM, CLKL[1]	0		0		ns

Note:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

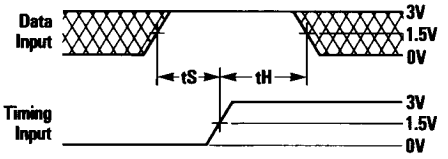
Timing Diagram
L64016



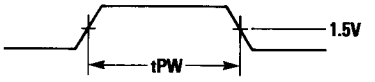
Timing Diagram
L64017



Set-Up and Hold Time (All Devices)

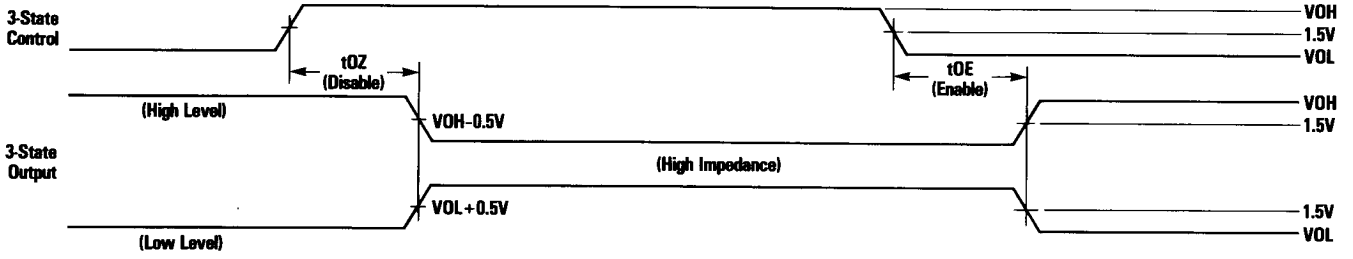


Pulse Width (All Devices)
LOW → HIGH → LOW



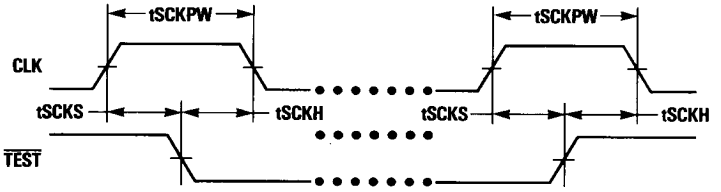
Notes:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

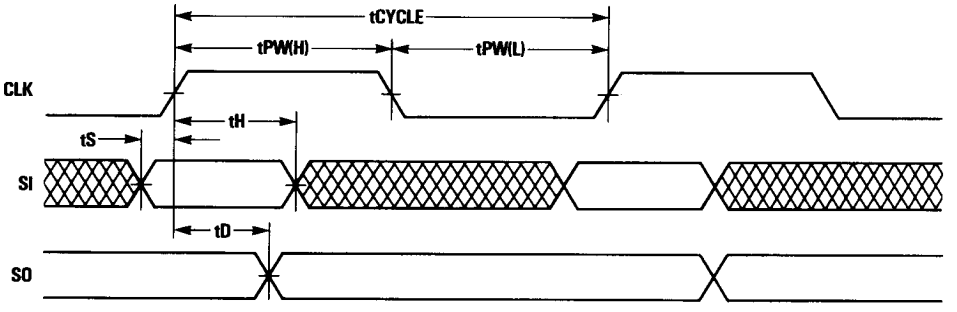
Three-State Timing Diagram



Scan Test Timing Waveforms

68-Pin Packages Only ($\overline{TEST}$ = LOW)





Notes:
1. During scan, all clocks must be tied together.
2. All clocks should be HIGH while entering and leaving TEST mode.
3. tCYCLE is 75 ns commercial, 100 ns mil.

Operating Characteristics

Absolute Maximum Ratings (Referenced to GND)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	−0.3 to +7	V
Input Voltage	VIN	−0.3 to VDD +0.3	V
DC Input Current	IIN	±10	mA
Storage Temperature Range	TSTG	−65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+3 to +6	V
Operating Ambient Temperature Range Military	TA	−55 to +125	°C
Industrial Range	TA	−40 to +85	°C
Commercial Range	TA	0 to +70	°C

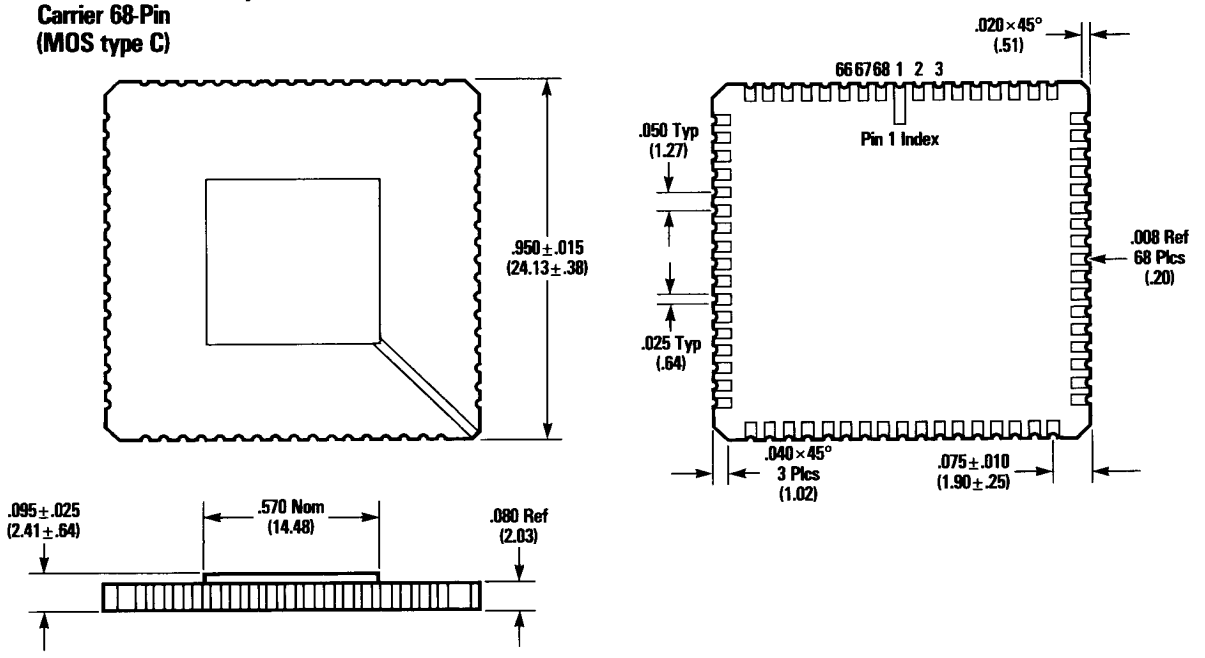
DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges[1].

Symbol	Parameter	Condition			Min	Typ	Max	Units
VIL	Low Level Input Voltage						0.8	V
VIH	High Level Input Voltage Commercial Temperature Range Military and Industrial Temperature Range				2.0 2.25			V V
IIN	Input Current	VIN = VDD			−100	−30	−8	µA
VOH	High Level Output Voltage		Comm	Mil				
		IOH =	−4 mA	−3.2 mA	2.4	4.5		V
VOL	Low Level Output Voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOZ	3-State Output Leakage Current	VOH = VSS or VDD			−10	±1	10	µA
IOS	Output Short Circuit Current[2]	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = 0V			−5		−100	mA
IDDQ	Quiescent Supply Current	VIN = VDD or VSS					10	mA
IDD	Operating Supply Current	tMC = tCYCLE = 50 ns				160		mA
CIN	Input Capacitance	Any Input				5		pF
COUT	Output Capacitance	Any Output				10		pF

Notes:
1. Military temperature range is −55°C to +125°C, ±10% power supply; industrial temperature range is −40°C to +85°C, ±5% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. All input pads have internal pull-up resistors.

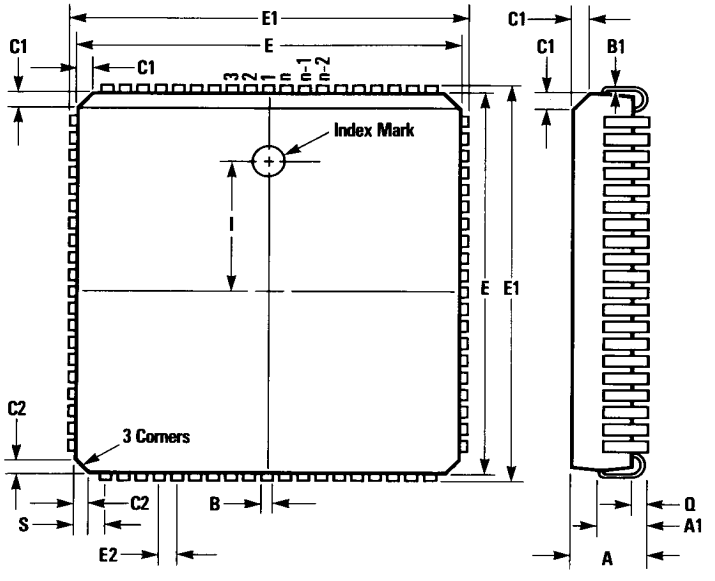
Package Drawings

Ceramic Leadless Chip Carrier 68-Pin (MOS type C)



Notes:
1. All exposed metallized area shall be gold plated 60 micro-inches Min. thickness over 50 microinches Min-350 microinches Max Nickel over refractory metallization.
2. Cap is gold plated kovar or ceramic.
3. Base is Al2O3.
4. Package dimensions fit within JEDEC outline for 50 mil center line pkgs.

68-Pin Plastic Leaded Chip Carrier



A	Min	.165 (4.19)
	Max	.185 (4.70)
A1	Min	.100 (2.54)
	Max	–
B	Min	.026 (.66)
	Max	.032 (.81)
B1	Ref	.020 (.51)
E	Min	.950 (24.13)
	Max	.958 (24.33)
E1	Min	.985 (25.02)
	Max	.995 (25.27)

E2	Ref	.050 (1.27)
Q	Min	.020 (.51)
	Max	–
S	Ref	.075 (1.90)
C1	Min	.042 (1.07)
	Max	.048 (1.22)
C2	Min	–
	Max	.010 (.25)
I	Ref	.350 (8.89)
Notes		1,2,3,4

Notes:
1. Pins are tin plated or hot solder dipped (increase B1 MAX by .003" (.08)) copper or Alloy 42.
2. Pin foot print matches that of ceramic chip carrier JEDEC Type A.
3. Package can be surface mounted or socketed.
4. Package dimensions fit within the JEDEC outline.

Ordering Information

L64016 / L64017 A L M B

- Screening Option
  - Blank = Standard Processing
  - C = Burn-In
  - B = Full 883C
- Temperature Range
  - C = Commercial (0°C to 70°C)
  - M = Military (−55°C to +125°C)
- Package Code
  - D = 64-Pin Ceramic DIP
  - L = 68-Pin Ceramic Leadless Chip Carrier
  - J = 68-Pin Plastic Leaded Chip Carrier
  - G = 68-Pin Ceramic Pin Grid Array
- Speed Range
  - Blank = Standard Speed
  - A = High Speed
- Device Type

Package Drawings

64 Lead (900 MIL) Cerdip