DS3200-1.1 November 1991

CT1555-3/CT1820

DATA TERMINAL BIT PROCESSOR FOR MIL-STD-1553 A & B

GENERAL DESCRIPTION

The CT1555-3/CT1820 Bit Processor Unit (BPU) is an advanced Hybrid Microcircuit that provides the interface between a MIL-STD-1553 Transceiver such as CT3231M or CT3232M, and the subsystem internal parallel data bus. The unit can be employed as the mux bus interface for Remote Subsystems or Master Terminal Bus Controllers, thus providing a common interface for all systems communicating over the bus.

The unit places no restrictions on Command, Response or polling operations as it transfers all Command, Status and Data words from the bus to parallel output lines, together with error information, bus status and handshaking signals. It also contains 5 Bit Address Recognition, Broadcast and Mode Code Decode, Terminal Fail Safe Signal and Self Test.

In the transmit mode, it accepts parallel data from the user and transmits Command, Status and Data words, under subsystem control, to the data bus. Positive handshaking signals provide logic control synchronisation between the unit and the subsystem for direct data flow.

The hybrid is completely compatible with all the electrical and functional spec requirements of MIL-STD-1553 A & B.

FEATURES

- Performs Encoder, Decoder, Logic and Control functions of a Data Bus Terminal to MIL-STD-1553 specifications, including Address, Mode Code and Broadcast Decoding and Terminal Fail Safe
- Flexibility - all control lines accessible
- Parallel tri-state subsystem I/O bus compatible with both 16 bit and 8 bit systems
- Dual rank I/O registers for versatile subsystem timing
- Operates from +5VDC @ 40mA typical (25mA CT1820)
- Self-contained oscillator and clock driver
- Look-ahead serial receive data output
- Self-test, on-line wraparound, plust off-line capability
- Interfaces directly with CT3231M or CT3232M Driver/ Receiver

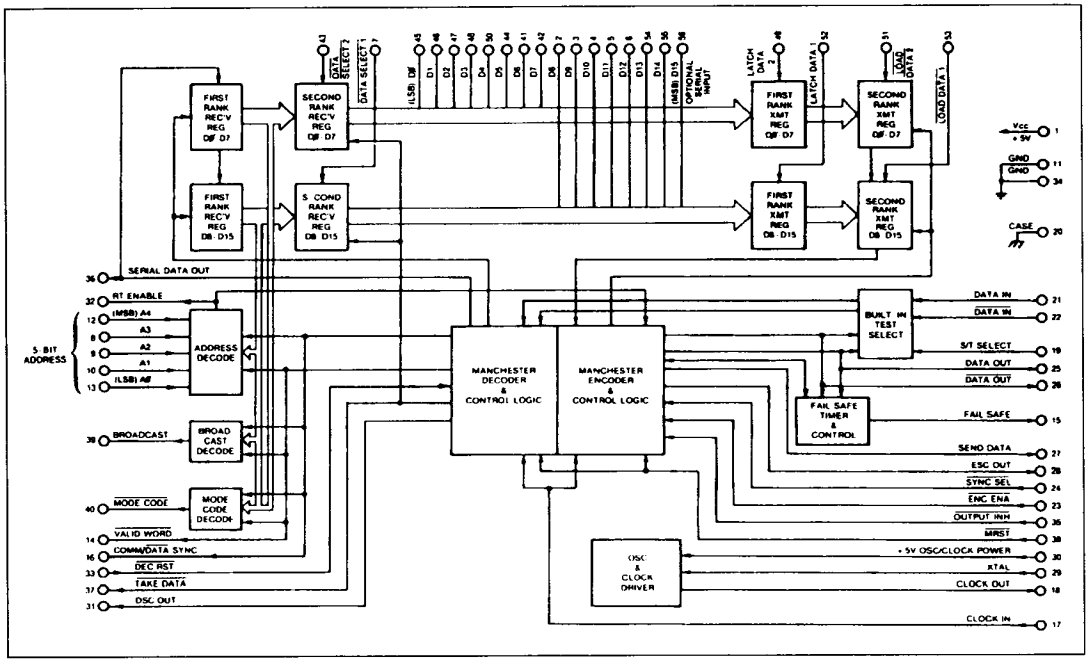


Figure 1: Functional Diagram

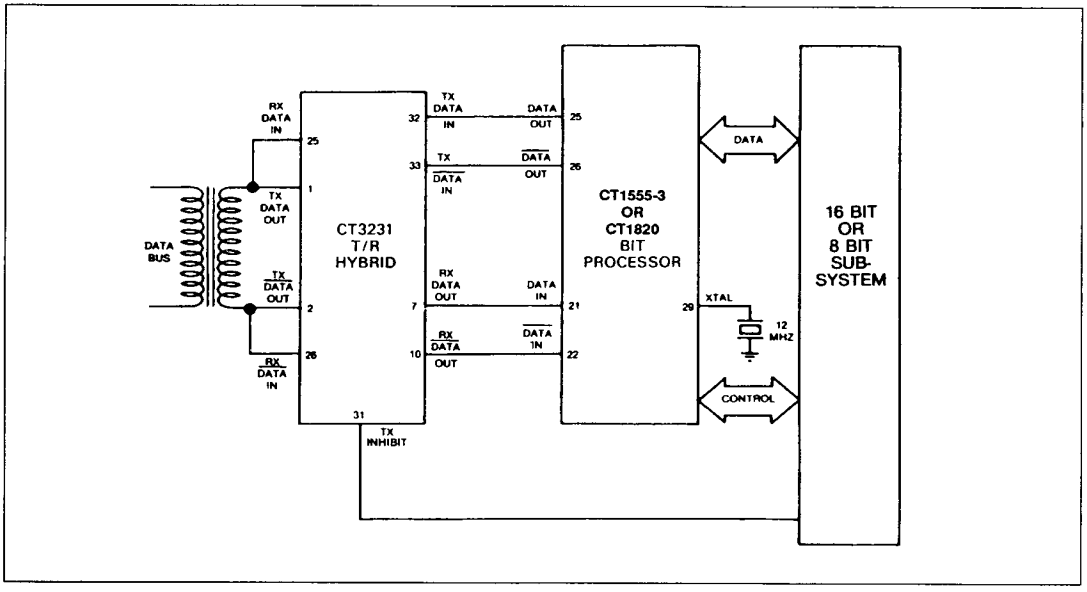


Figure 2: Typical MIL-STD-1553 Data Terminal

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Logic Input Voltage	-0.3 to +5.5V
Logic Input Current	-20 to +4mA
Clock Output Current (PIN 18)	15 mA
Clock In (PIN 17)	-0.3 to V_{CC} +0.3V
Storage Temperature Range	-65 to +150°C
Operating Case Temperature Range	-55 to +125°C

ELECTRICAL CHARACTERISTICS, V_{CC} = 5.0V ±5%

Symbol	Parameter / Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage	2.0			V
V_{IL}	Logic "0" Input Voltage			0.7	V
V_{OH}	Logic "1" Output Voltage	See Pin assignments and Loading			
V_{OL}	Logic "0" Output Voltage	See Pin assignments and Loading			
V_{IHC}	Logic "1" Input Voltage (CLOCK)	V_{CC}-0.5			V
V_{ILC}	Logic "0" Input Voltage (CLOCK)			GND+0.5	V
V_{OHC}	Logic "1" Output Voltage (CLOCK)	V_{CC}-0.3			V
V_{OLC}	Logic "0" Output Voltage (CLOCK)			GND+0.3	V
I_{OC}	Logic Supply Current		40		mA
I_{OSC}	Oscillator / Clock Supply Current		8	13	mA

PIN ASSIGNMENTS AND LOADING

In the following table, the symbols are defined as follows:
I_{IH} = maximum input HIGH current with V_{IN} = 2.5 volts
I_{IL} = maximum input LOW current with V_{IN} = 0.4 volts
I_{OH} = maximum output HIGH current for V_{OUT} = 2.5 volts minimum
I_{OL} = maximum output LOW current for V_{OUT} = 0.4 volts maximum

* indicates use of an internal pull-up resistor

Pin No.	Name	CT1555-3 I_{IH} (µA)	CT1555-3 I_{IL} (µA)	CT1555-3 I_{OH} (µA)	CT1555-3 I_{OL} (mA)	CT1820 I_{IH} (µA)	CT1820 I_{IL} (µA)	CT1820 I_{OH} (µA)	CT1820 I_{OL} (mA)	CT1820-2 I_{OL} (mA)	Description
1	V_{CC}										+5V Power Input
2	D8	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
3	D9	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕ ↕
4	D10										
5	D11										
6	D12	40	-0.4	-1000	2.4			-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
7	DATA SELECT 1	20	-0.4								A LOW on this input applies the contents of the SECOND RANK REC'V REG to the D8-D15 I/O pins
8	A3*	-1500	-3.2								Part of 5 Bit ADDRESS INPUT
9	A2*										↕ ↕
10	A1*	-1500	3.2			20	-0.4				Part of 5 Bit ADDRESS INPUT
11	GROUND										Logic and power return
12	A4*	-1500	-3.2			20	-0.4				MSB of 5 Bit ADDRESS INPUT
13	A0*	-1500	-3.2			20	-0.4				LSB of 5 Bit ADDRESS INPUT
14	VALID WORD			-400	2.4			-400	4.0	4.0	A LOW on this output indicates receipt of a valid word
15	FAIL SAFE			-400	2.4			-400	4.0	4.0	A HIGH on this output indicates termination of a transmitted message that exceeds 768µs.
16	COMM / DATA SYNC			- 380	2.4			-400	4.0	4.0	A HIGH on this output indicates COMMAND (or STATUS) word reception. A LOW indicates DATA word reception.
17	CLOCK IN	±30	±0.003			100	0.1				Input for 12MHz clock (20pf load). See text for clock requirements.
18	CLOCK OUT			-1000	1.0			-1000	1.0	1.0	Output of OSCILLATOR AND CLOCK DRIVER (see text for description).
19	S / T SELECT	40	-0.8			20	-0.4				A HIGH on this input sets the unit in the self test mode.
20	CASE										CASE CONNECTION
21	DATA IN	20	-0.4			20	-0.4				A HIGH on this input represents a positive state on the bus.
22	DATA IN	20	-0.4			20	-0.4				A HIGH on this input represents a negative state on the bus. (Pins 21 and 22 must both be high when the bus is inactive.)
23	ENC ENA	20	-0.4			20	-0.4				A LOW on this input initiates a transmit cycle.
24	SYNC SEL	20	-0.4			20	-0.4				Actuates COMMAND (or STATUS) sync for an input LOW and DATA sync for an input HIGH.
25	DATA OUT			360	2.4			-400	4.0	4.0	A HIGH on this output produces a positive state on the bus.
26	DATA OUT			360	2.4			-400	4.0	4.0	A HIGH on this output produces a negative state on the bus.
27	SEND DATA			380	2.4			-400	4.0	4.0	A HIGH on this output indicates data shifting during the transmit cycle.
28	ESC OUT			1000	1.2			-1000	1.2	1.2	LOW to HIGH transitions on this output during HIGH SEND DATA cause the transmit cycle data shifting to occur.
29	XTAL										A 12MHz (parallel resonant) crystal is connected between this pin and ground.
30	+5V OSC / CLOCK POWER										+5V power for OSCILLATOR AND CLOCK DRIVER.
31	DSC OUT			-1000	1.2			-1000	1.2	1.2	LOW to HIGH transitions on this output during LOW TAKE DATA cause receive cycle data shifting to occur.
32	RT ENABLE			-400	2.4			-400	4.0	4.0	A HIGH on this output indicates reception of a valid COMMAND (or STATUS) word containing the terminal's address. It also resets the FAIL SAFE.

Pin No.	Name	CT1555-3				CT1820				CT1820-2	Description
		I_{IH} (µA)	I_{IL} (µA)	I_{OH} (µA)	I_{OL} (mA)	I_{IH} (µA)	I_{IL} (µA)	I_{OH} (µA)	I_{OL} (mA)	I_{OL} (mA)	
33	$\overline{\text{DEC RST}}$	20	-0.4			20	-0.4				A LOW on this input (for 1µs minimum) resets the decoder to a condition ready for a new word, resets the COMM / $\overline{\text{DATA}}$ SYNC output LOW, and resets the $\overline{\text{VALID WORD}}$ output HIGH.
34	GROUND										Logic and power return.
35	$\overline{\text{OUTPUT INH}}$	20	-0.4			20	-0.4				A LOW on this input holds output pins 25 and 26 LOW.
36	SERIAL DATA OUT			-400	1.6			-400	4.0	4.0	The received serial data in NRZ format is available at this pin during LOW $\overline{\text{TAKE DATA}}$.
37	$\overline{\text{TAKE DATA}}$			-360	2.4			-400	4.0	4.0	A LOW on this output indicates data shifting during the receive cycle. A LOW to HIGH transition on this pin always transfers the current contents of the FIRST RANK REC'V REG to the SECOND RANK REC'V REG.
38	$\overline{\text{MRST}}$	60	-1.2			20	-0.4				A LOW on this input (for 1µs minimum) interrupts and clears the transmit cycle, resets the FAIL SAFE, and also performs the same functions as $\overline{\text{DEC RST}}$.
39	BROADCAST*			-300	1.6			-400	4.0	4.0	A HIGH on this output indicates reception of a valid COMMAND (or STATUS) word containing all ONES in the address field.
40	$\overline{\text{MODE CODE}}$*			-600	2.4			-600	6.0	6.0	A LOW on this output indicates reception of a valid COMMAND (or STATUS) word containing all ONES or all ZEROS in the sub-address field.
41	D6	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
42	D7	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
43	$\overline{\text{DATA SELECT 2}}$	20	-0.4			20	-0.4				A LOW on this input applies the contents of the SECOND RANK REC'V REG to the D0 -D7 I/O pins.
44	D5	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
45	D0										LSB of 16 Bit TRI-STATE I/O
46	D1										Part of 16 Bit TRI-STATE I/O
47	D2										Part of 16 Bit TRI-STATE I/O
48	D3	40	-0.4	-1000	2.4			-1000	6.0		Part of 16 Bit TRI-STATE I/O
49	LATCH DATA 2	20	-0.4								A HIGH on this input allows the I/O data on D0-D7 to appear at the output of the FIRST RANK XMT REG. A LOW on this input holds the register outputs in their last state.
50	D4	40	-0.4	-1000	2.4			-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
51	$\overline{\text{LOAD DATA 2}}$	60	-1.2								A LOW on this input loads the D0-D7 data into the SECOND RANK XMT REG. A HIGH on this input then locks out the data inputs to permit serial shifting.
52	LATCH DATA 1	20	-0.4			20	-0.4				A HIGH on this input allows the I/O data on D8-D15 to appear at the output of the FIRST RANK XMT REG. A LOW on this input holds the register outputs in their last state.
53	$\overline{\text{LOAD DATA 1}}$	60	-1.2			20	-0.4				A LOW on this input loads the D8-D15 data into the SECOND RANK XMT REG. A HIGH on this input then locks out the data inputs to permit serial shifting.
54	D13	40	-0.4	-1000	2.4			-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
55	D14	40	-0.4	-1000	2.4			-1000	6.0	10.0	Part of 16 Bit TRI-STATE I/O
56	D15	40	-0.4	-1000	2.4	20	-0.4	-1000	6.0	10.0	MSB of 16 Bit TRI-STATE I/O and OPTIONAL SERIAL INPUT.

TRANSMIT CYCLE OPERATION

ENCODER SHIFT CLOCK (ESC) (see Figure 3) operates at the data rate (1MHz). A low at ENCODER ENABLE (ENC ENA) during a falling edge of ESC ① starts the Transmit cycle, which lasts for twenty ESC clock periods. The SYNC SELECT (SYNC SEL) input is valid at the next low-to-high transition of ESC ②. A high at SYNC SEL will produce a data sync, or a low will produce a command sync for that word.

Parallel data must be stable at the second rank transmit register before SEND DATA goes high ③. Since ENC ENA is not synchronous with ESC, the minimum time to ③ is 3µsec from ENC ENA leading edge.

The first-rank transmit register may be operated transparently (LATCH DATA always high), or may be used to hold data ready for transmission, independent of the activity on the 16-line subsystem I/O bus. As long as LATCH DATA is held high, data present on the subsystem I/O bus appears at the output of the first rank transmit register. Stable data may be latched and held at the first rank register output by bringing LATCH DATA low. Data to be transmitted may be latched any time before the low-to high transition of SEND DATA (SEND DATA, when appled to the LOAD DATA inputs, locks out the data inputs to the second rank transmit register.) For multiple word transmissions, the next word may be inputted and latched any time after ③, but before the next low to-high transition of SEND DATA.

SEND DATA remains high for 16 ESC periods, during which the parallel transmit data is clocked to the MANCHESTER ENCODER ③ to ④. After the sync and Manchester coded data are transmitted through the DATA OUT and DATA OUT outputs, the ENCODER adds on the parity bit for that word ⑤.

If the transmitted word is to be the last word of the transmission, ENC ENA must go high by ⑤ to prevent initiation of another transmit cycle.

At any time, a low applied to OUTPUT INHIBIT will force both DATA OUT and DATA OUT to a low state without affecting any other operations.

The entire transmit cycle may be interrupted and cleared by applying a minimum of 1µsec negative pulse to the MASTER RESET (MRST) input.

For 8-BIT I/O subsystems, D0 is tied to D8, D1 to D9, etc., through D7 tied to D15, and data is inputted in 8-BIT bytes by using LATCH DATA 1 and LATCH DATA 2 and / or LOAD DATA 1 and LOAD DATA 2 independently.

For serial data applications, D15 input serves as the serial transmit input. With LOAD DATA 1 held low and LATCH DATA 1 held high, D15 input is applied to the ENCODER's serial data input. Inputted data must be at the ESC rate with the MSB starting at the low-to-high transition of SEND DATA.

If a message length ever exceeds 768µsec, the 768µsec TIME OUT (FAIL SAFE) flag goes high, and DATA OUT and DATA OUT are both forced to a low state. This condition will remain until a valid command word (containing the terminal's address) is received or until MRST goes low.

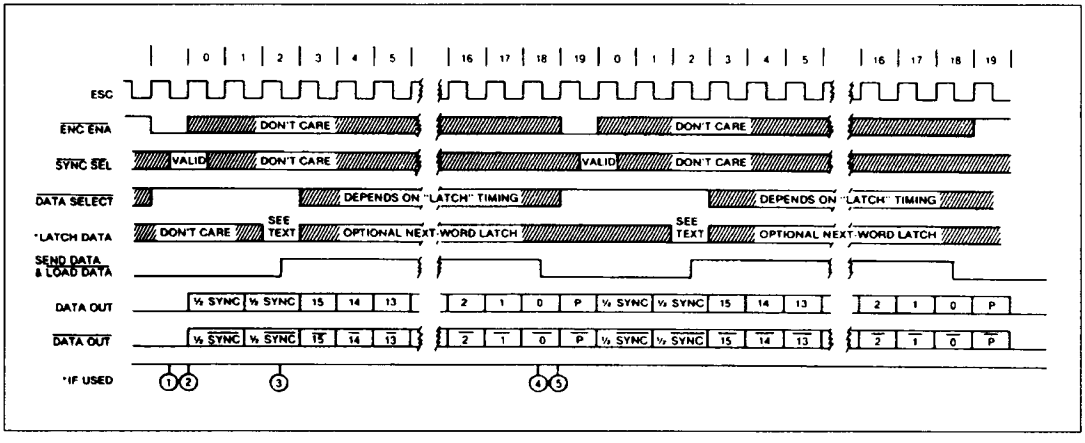
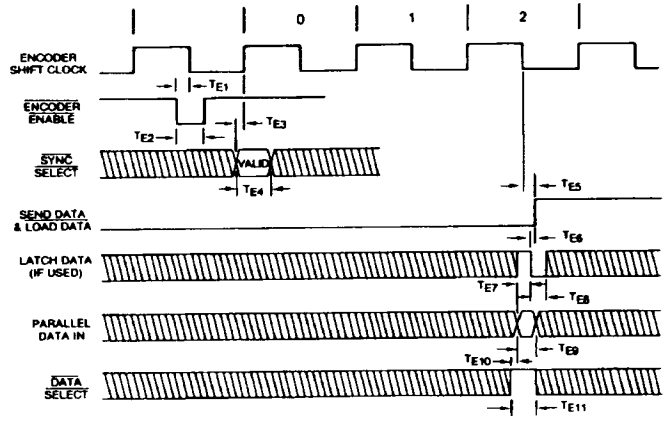


Figure 3: Transmit Cycle Timing



Symbol	Description	Min	Max	Units
T_{E1}	$\overline{\text{ENCODER ENABLE}}$ SET-UP TIME	100		ns
T_{E2}	$\overline{\text{ENCODER ENABLE}}$ PULSE WIDTH	180		ns
T_{E3}	$\overline{\text{SYNC SELECT}}$ SET-UP TIME	190		ns
T_{E4}	$\overline{\text{SYNC SELECT}}$ 'VALID' PULSE WIDTH	150		ns
T_{E5}	SEND DATA DELAY		70	ns
T_{E6}	LATCH DATA HOLD TIME	25		ns
T_{E7}	LATCH DATA SET UP TIME	50		ns
T_{E8}	LATCH DATA PULSE WIDTH LOW	50		ns
T_{E9}	PARALLEL DATA 'VALID' WIDTH	75		ns
T_{E10}	$\overline{\text{DATA SELECT}}$ DISABLE TIME	25		ns
T_{E11}	$\overline{\text{DATA SELECT}}$ PULSE WIDTH HIGH	100		ns

Figure 4: Encoder Timing Detail

RECEIVE CYCLE OPERATION

DECODER SHIFT CLOCK (DSC) (see Figure 5) operates at the data rate (1MHz). When the DECODER recognises a valid sync and two valid Manchester data bits ①, a receive cycle is initiated. The new sync is indicated at the COMMAND/$\overline{\text{DATA}}$ SYNC (C/$\overline{\text{D}}$ SYNC) output and the $\overline{\text{TAKE DATA}}$ output goes low ②. The C/$\overline{\text{D}}$ sync output will remain in its valid state until a new sync is detected on a subsequent word or until $\overline{\text{DECODER RESET}}$ ($\overline{\text{DEC RST}}$) or $\overline{\text{MRST}}$ goes low. A low at $\overline{\text{DEC RST}}$ or $\overline{\text{MRST}}$ causes C/$\overline{\text{D}}$ SYNC to go low.

$\overline{\text{TAKE DATA}}$ remains low for 16 DSC periods during which time the 16 serial data bits appear at the SERIAL DATA OUTPUT (SDO). This data is simultaneously loaded into the first-rank receive register. The low-to-high transition of $\overline{\text{TAKE DATA}}$ ③ makes the new data available at the output of the second-rank receive register. This data remains available until the next low-to-high transitions of $\overline{\text{TAKE DATA}}$. It is not reset or cleared by any other signals. This data is applied to the D0 to D15 I/O bus by setting $\overline{\text{DATA SELECT}}$ lines low.

After all data has been loaded into the receive registers, the data is checked for odd parity. A low on $\overline{\text{VALID WORD}}$ ($\overline{\text{VW}}$) output ④, indicates successful reception of a word without any Manchester or parity errors. For consecutive word receptions, $\overline{\text{VW}}$ will go high again in 3 to 3.5µs. In the absence of succeeding valid syncs, $\overline{\text{VW}}$ will return high in 20µs. A $\overline{\text{DEC RST}}$ (low) at any time will reset $\overline{\text{VW}}$ high.

All decoded commands, including RT ENABLE (address recognition), BROADCAST and $\overline{\text{MODE CODE}}$ are enabled internally by $\overline{\text{VW}}$ and remain valid only as long as $\overline{\text{VW}}$ is low.

For 8-BIT I/O subsystems (D0 tied to D8, through D7 tied to D15), data may be extracted in 8 BIT bytes by selectively activating $\overline{\text{DATA SELECT}}$ 1 and $\overline{\text{DATA SELECT}}$ 2.

For serial data systems, SERIAL DATA OUTPUT is available at the DSC rate from ② to ③.

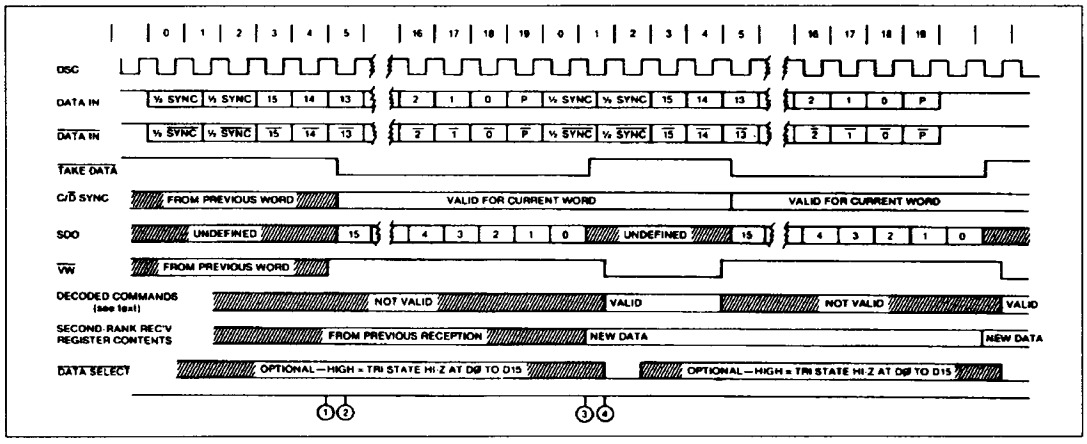
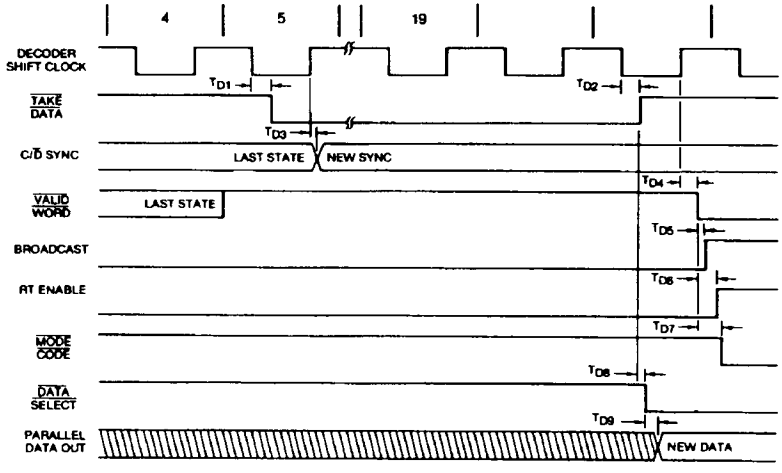


Figure 5: Receive Cycle Timing



Symbol	Description	Min	Max	Units
T_{D1}	$\overline{\text{TAKE DATA}}$ RELAY ON		125	ns
T_{D2}	$\overline{\text{TAKE DATA}}$ DELAY OFF		125	ns
T_{D3}	SYNC DELAY		50	ns
T_{D4}	$\overline{\text{VALID WORD}}$ DELAY		125	ns
T_{D5}	BROADCAST DELAY		70	ns
T_{D6}	RT ENABLE DELAY		100	ns
T_{D7}	$\overline{\text{MODE CODE}}$ DELAY		100	ns
T_{D8}	$\overline{\text{DATA SELECT}}$ INPUT DELAY	0 (Note 1)		ns
T_{D9}	PARALLEL DATA OUTPUT DELAY		50 (Note 2)	ns

Notes: 1. $\overline{\text{DATA SELECT}}$ may be applied at any time that the 16 line I/O is otherwise free. The parallel DATA OUT, however, is not 'NEWDATA' until 50ns after $\overline{\text{TAKE DATA}}$ goes high.
2. 180ns max for CT1555-3

Figure 6: Decoder Timing Detail

SELF TEST FUNCTION

A high on the S/T SELECT input sets the hybrid in the SELF TEST mode. In this mode, the DATA and $\overline{\text{DATA}}$ output lines are connected to the Decoder inputs so that the unit may operate in the "wraparound" mode without actually going through the data bus transceiver. Note that the DATA and $\overline{\text{DATA}}$ output lines are active in this mode and the S/T SELECT command must also be used to inhibit the data bus transmitter to prevent arbitrary transmission on the data bus.

TERMINAL FAIL SAFE

In order to satisfy the Terminal Fail Safe requirements of MIL-STD-1553B, the DATA and $\overline{\text{DATA}}$ output lines are continuously monitored for length of message. A transmitted message in excess of 768µs sets the FAIL SAFE output high and terminates the transmission by setting both DATA and $\overline{\text{DATA}}$ output lines low. As a redundant safety factor, the FAILSAFE output may be applied to the INHIBIT input of the data bus transmitter (if so equipped). Further transmissions are prevented until the FAIL SAFE flag is reset either by reception of a valid command word containing the terminal address or by a negative pulse on the $\overline{\text{MRST}}$ input. Note: Transmissions containing gaps of 3µs or less are considered continuous, even if the gap is caused by a $\overline{\text{MRST}}$ pulse.

TERMINAL ADDRESS LINES

The five-bit terminal address is set by hard wiring the 5-BIT ADDRESS lines. The hybrid contains internal pull-up resistors so that logic "1" lines may be left open circuited. Logic "0" lines must be grounded.

In operation, RT ENABLE goes high when a valid command word containing the hard-wired address is received. See "RECEIVE CYCLE OPERATION" for timing.

OSCILLATOR AND CLOCK DRIVER

The hybrid may be operated with either the internal clock or an external clock source.

For internal clock operation, a 12MHz parallel-resonant fundamental-mode crystal must be connected from XTAL to ground. Power (+5V) must be applied to +5V OSC/CLOCK POWER and CLOCK OUT must be connected to CLOCK IN.

For external clock operation, no power is applied to +5V OSC/CLOCK POWER and the external clock is applied to CLOCK IN (CLOCK OUT not connected). The external clock must be capable of driving a 20 picofarad load to within 0.5 volts of V_{CC} and within 0.5 volts of ground with rise and fall times of less than 10 nanoseconds. Standard TTL levels are not satisfactory. For a normal 1MHz data rate, the clock frequency must be 12MHz.

FALSE RT ENABLE

Terminals that continuously monitor their own transmissions are subject to "END-AROUND" operation due to a false RT ENABLE. The terminal can erroneously interpret its own status word as a new command word. If no measures are taken to prevent or re-set RT ENABLE, it will remain high for 20µs or until the DECODER recognises a new valid sync (whichever time is shorter).

RT ENABLE may be inhibited by interrupting the RECEIVE CYCLE during a status word transmission. Inverted SEND DATA applied to DEC RST will prevent reception of the status word.

If continuous monitoring is required, RT ENABLE may be reset immediately after it goes high by a 1µs (minimum) low at DEC RST. The status word will then be available at the second-rank receive register.

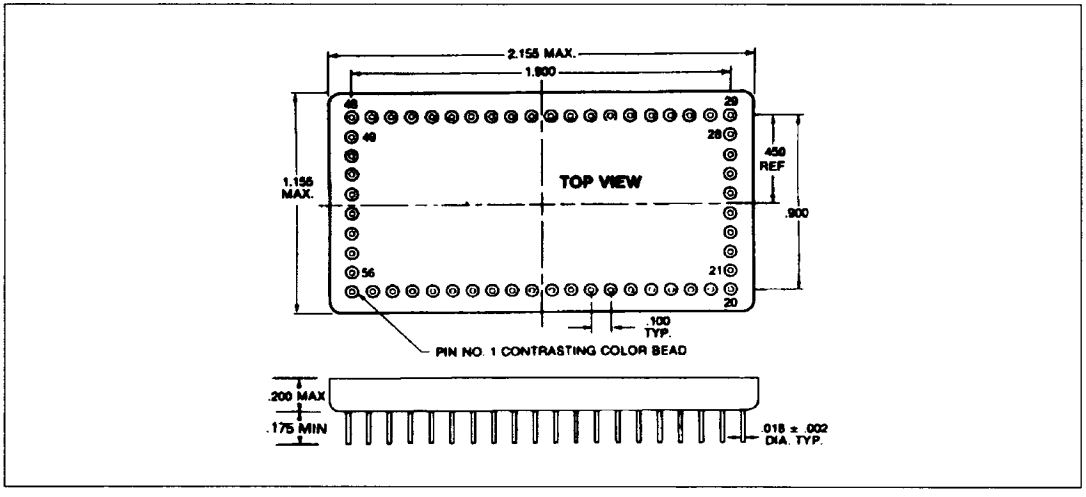


Figure 7: Package Outline