CT3231M/CT3231MFP

Low Power Driver/Receiver

for MIL-STD-1553

Note: "M" designates monolithic devices used internally. Specifications also apply to the CT3231 and CT3231FP except as noted.

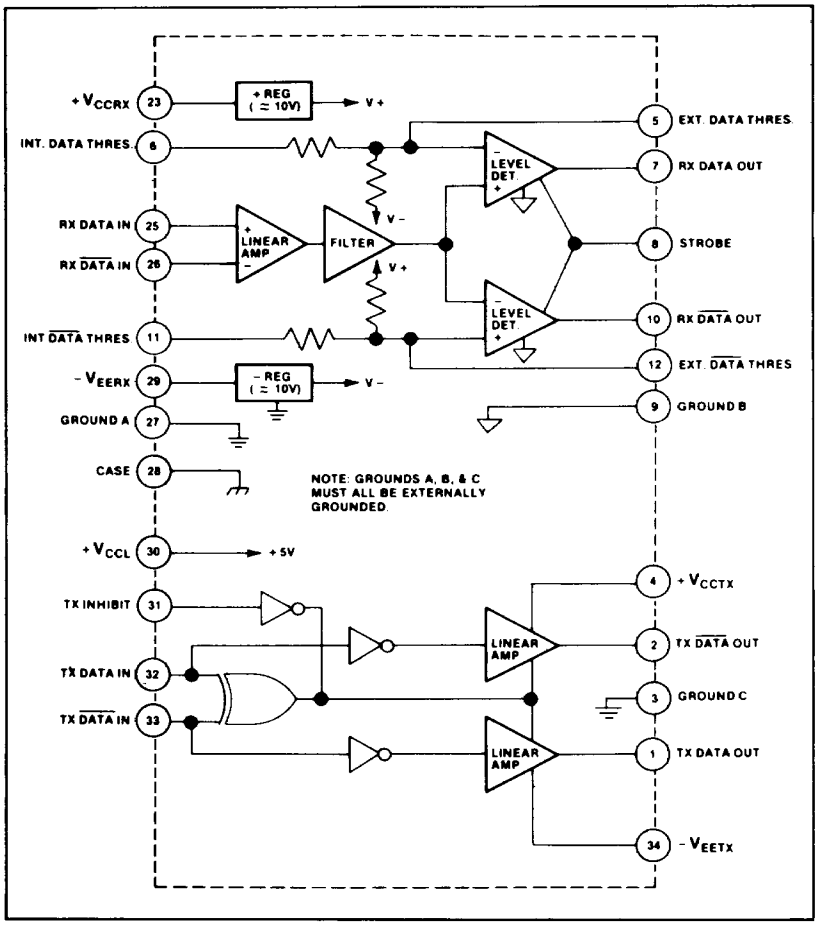
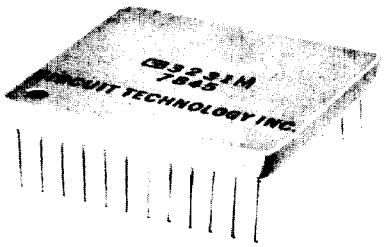


FIGURE 1.
FUNCTIONAL DIAGRAM AND PINOUTS

FEATURES

- **1.5 Watt Total Hybrid Dissipation at 25% Transmitting Duty Cycle**
- **Meets MIL-STD-1553B**
- **TTL Compatible**
- **Meets MIL-STD-883 & MIL-M-38510**
- **Thick Film Hybrid Technology**
- **Driver/Receiver in a single Package for Space & Weight Savings**
- **Plug-In or Flat Pack Configuration**
- **Filtering on Receiver to Improve S/N Ratio of System**
- **Interfaces directly with CT1555 Bit Processor**



See Figure 6 for outline drawings of available packages.

DRIVER DESCRIPTION

The CT3231M Driver section accepts complementary TTL Data at the input, and produces a 30 volt-nominal peak-to-peak differential signal across a 140Ω load at the output. When coupled to the Data Bus with a 1:1 transformer, isolated on the Data Bus side with two 55.0 ohm fault isolation resistors, and loaded by two 70 ohm terminations plus additional receivers, the Data Bus signal produced is 7.2 volts-nominal peak-to-peak.

When both "DATA" and "$\overline{\text{DATA}}$" inputs are held low or both are held high, the driver output becomes a high impedance and is "removed" from the line. In addition, an overriding "INHIBIT" input provides for removal of the Driver output from the line. A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the Driver. See Driver Logic Waveforms, Figure 3.

DATA and $\overline{\text{DATA}}$ inputs must be complementary waveforms, of 50% duty cycle average, with no gate delays between them. It is recommended that those inputs be driven from a "D" type flip-flop.

RECEIVER DESCRIPTION

The CT3231M Receiver section accepts Bi-Phase Differential data at the input and produces two TTL signals at the output. The outputs are "DATA" and "$\overline{\text{DATA}}$", and represent positive and negative excursions (respectively) of the input beyond a predetermined threshold. See Receiver Logic Waveforms, Figure 2.

The positive and negative thresholds may be internally set by grounding the appropriate pins, or externally set with resistors. The pre-set internal thresholds will detect Data Bus signals exceeding 1 volt p-p and ignore signals less than 0.5 volt p-p when used with a 1:1 transformer. (See Figure 4 for a suitable transformer and typical connection.)

A low level at the STROBE input inhibits the DATA and $\overline{\text{DATA}}$ outputs. If unused, a 2K ohm pull-up to +5V is recommended.

CT3231M SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Pin 4 or 23	−0.3 to +18.0 V
Supply Voltage, Pin 29 or 34	+0.3 to −18.0 V
Supply Voltage, Pin 30	−0.3 to +7.0 V
Logic Input Voltage, Pin 8, 31, 32, or 33	−0.3 to +5.5 V
Receiver Differential Input, Pin 25 to Pin 26	±20 V (40 V p-p)
Receiver Input Voltage, Pin 25 or Pin 26	±15 V
Driver Peak Output Current, Pin 1 or Pin 2	±300 mA
Total Package Power Dissipation at (Ambient) T_A = +25°C (Derate above T_A = +25°C at 40 mW/°C)	4.0 watts (Note 1)
Power Dissipation at Specified Case Temperatures	See Figure 5.
Operating Case Temperature Range (T_C) (See Figure 5 for limitations)	−55 to +125°C

ELECTRICAL CHARACTERISTICS, RECEIVER SECTION

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage Ranges		V_{CCRX}	+11.75		+15.75	V
		V_{EERX}	−11.75		−15.75	V
(V_{CCL} is common to both Driver and Receiver)		V_{CCL}	+4.75		+5.25	V
Supply Current		I_{CCRX}		25	Note 2	mA
		I_{EERX}		30	Note 2	mA
(I_{CCL} includes Driver and Receiver Together)		I_{CCL}		35	Note 2	mA
Differential Input Impedance	D.C.	R_{IN}	6K			ohms
	f = 1MHz	Z_{IN}	4K			ohms
Differential Voltage Range		V_{IDR}	±20			V peak
Input Common Mode Voltage Range		V_{ICR}	±10			V peak
Common Mode Rejection Ratio (From Point A, Fig. 4)		CMRR	40			dB
Strobe Characteristics (Logic "0" inhibits Output)						
"0" Input Current (V strobe = 0.5 V)		I_{IL}			−4	mA
"1" Input Current (V strobe = 2.7 V)		I_{IH}			400	μA
"0" Input Voltage		V_{IL}			0.7	V
"1" Input Voltage		V_{IH}	2.0			V
Strobe Delay (turn-on or turn-off)		t_{SD}		6		nS
Threshold Characteristics (Sinewave input, 100KHz to 1MHz)						
Note: Threshold voltages are referred to the Input.						
Internal (Pin 6 & 11 grounded)		V_{TH_1}	0.6		0.9	V p-p
External (Pin 6 & 11 open; threshold setting resistors from Pin 5 to ground & from Pin 12 to ground; R_{TH} Max = 10K ohms.)		R_{TH}/V_{TH_1}		4000		ohms/V p-p
Filter Characteristics (Pin 6 & 11 Grounded)	f = 2MHz	V_{TH_2}	0.8		1.5	V p-p
(Sinewave input)	f = 4MHz	V_{TH_4}	4.2		8.5	V p-p
Output Characteristics, RX Data & $\overline{\text{Data}}$						
"1" State (I_{SOURCE} = −0.4 ma) Note 2		V_{OH}	2.5	3.3		V
"0" State (I_{SINK} = 4 ma) Note 2		V_{OL}			0.5	V
Note: With Receiver input below threshold, both RX Data & RX $\overline{\text{Data}}$ outputs remain in "1" state.						
Delay (average) from differential input zero crossings to RX Data and RX $\overline{\text{Data}}$ output 50% points.		t_{DRX}		190		nS

Note 1: Assumes unit in free air (natural convection cooling).

Note 2: For CT3231/CT3231FP ONLY
"1" STATE (I_{SOURCE} = −1 ma)
"0" STATE (I_{SINK} = 10 ma)

ELECTRICAL CHARACTERISTICS, DRIVER SECTION

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage Ranges		V_{CCTX}	+11.75		+15.75	V
(See Receiver Section for V_{CCL})		V_{EETX}	−11.75		−15.75	V
Supply Current, "Standby" mode (see Receiver Section for I_{CCL})		I_{CCTXS}		12	Note 2	mA
(TX Inhibit high; or TX Data & TX $\overline{\text{Data}}$ both high or both low)		I_{EETXS}		0	1	mA
Supply Current transmitting at 1MHz into a 35 ohm load at point A in Figure 4.	DUTY CYCLE					
	25%	I_{CCX25}	Note 4	45	Note 2	mA
		I_{EEX25}	Note 3	35	Note 2	mA
(I_{CCL} limits do not change with mode of operation or duty cycle)	100%	I_{CCTX}	Note 4	150	Note 2	mA
		I_{EETX}	Note 3	135	Note 2	mA
Input Characteristics, TX Data in or TX $\overline{\text{Data}}$ in						
"0" Input Current (V_{IN} = 0.4 V)		I_{ILD}			−1.2	mA
"1" Input Current (V_{IN} = 2.7 V)		I_{IHD}			100	μA
"0" Input Voltage		V_{ILD}			0.7	V
"1" Input Voltage		V_{IHD}	2.0			V
Inhibit Characteristic						
"0" Input Current (V_{IN} = 0.4 V)		I_{ILI}			−0.8	mA
"1" Input Current (V_{IN} = 2.7 V)		I_{IHI}			50	μA
"0" Input Voltage		V_{ILI}			0.7	V
"1" Input Voltage		V_{IHI}	2.0			V
Delay from TX $\overline{\text{Inhibit}}$ (0→1) to inhibited output impedance		t_{DXOFF}		300		nS
Delay from TX $\overline{\text{Inhibit}}$ (1→0) to active output impedance		t_{DXON}		100		nS
Differential output noise, inhibit mode		V_{NOI}			10	mVp-p
Differential output impedance (inhibited) at 1MHz		Z_{OI}	10K			ohms
Output Characteristics (Figure 3)						
Differential output level (140 ohm load)		V_O	26	30	35	V p-p
Differential Active output impedance at 1MHz		Z_{OA}		4		ohms
Rise and Fall times (10% to 90% of p-p output)		t_r	100	150	300	nS
Output offset at point A in Fig. 4 (35 ohm load) 2.5 μS after mid-bit crossing of the parity bit of the last word of a 660 μS message		V_{OS}		±20	±75	mV peak
Delay from 50% point of TX Data or TX $\overline{\text{Data}}$ input to zero crossing of differential output		t_{DTX}		100		nS

Note 2: *Maximum supply currents for driver and receiver combined are included in power and thermal data table.*

POWER AND THERMAL DATA, TOTAL HYBRID (DRIVER AND RECEIVER)

PARAMETER/CONDITION		SYMBOL	MIN	TYP	MAX	UNIT
Total Supply Current "Standby" mode, or transmitting at less than 1% duty cycle (e.g. 20 μS of transmission every 2 mS or longer interval)		I_{CCS}		40	50	mA
		I_{EES}		30	40	mA
		I_{CCL}		35	45	mA
Total Supply Current transmitting at 1MHz into a 35 ohm load at point A in Figure 4.	DUTY CYCLE					
	25%	I_{CC25}	Note 4	70	80	mA
		I_{EE25}	Note 4	65	75	mA
(I_{CCL} limits do not change with mode of operation or duty cycle)	100%	I_{CC100}	Note 4	175	190	mA
		I_{EE100}	Note 4	165	180	mA
Power Dissipation of most critical (hottest) device in hybrid during continuous transmission (100% duty cycle)	SUPPLY VOLTAGE					
	±12 V	P_{C12}	Note 3	300	400	mW
	±15 V	P_{C15}	Note 3	450	600	mW
Thermal Resistance, junction-to-case, of most critical device		Θ_{JC}		80	100	°C/W
Allowable transmitting duty cycle when case is held to +100°C maximum		Note 5			100	%
Allowable transmitting duty cycle when case is held to +125°C maximum	±12 V supplies	Note 5			80	%
	±15 V supplies	Note 5			55	%

Note 3: *Decreases linearly to zero at zero duty cycle.*
Note 4: *Decreases linearly to applicable "Standby" value at zero duty cycle.*
Note 5: *Based upon operating junction temperature of 160°C for hottest device. For lower operating junction temperatures, reduce maximum duty cycle accordingly.*

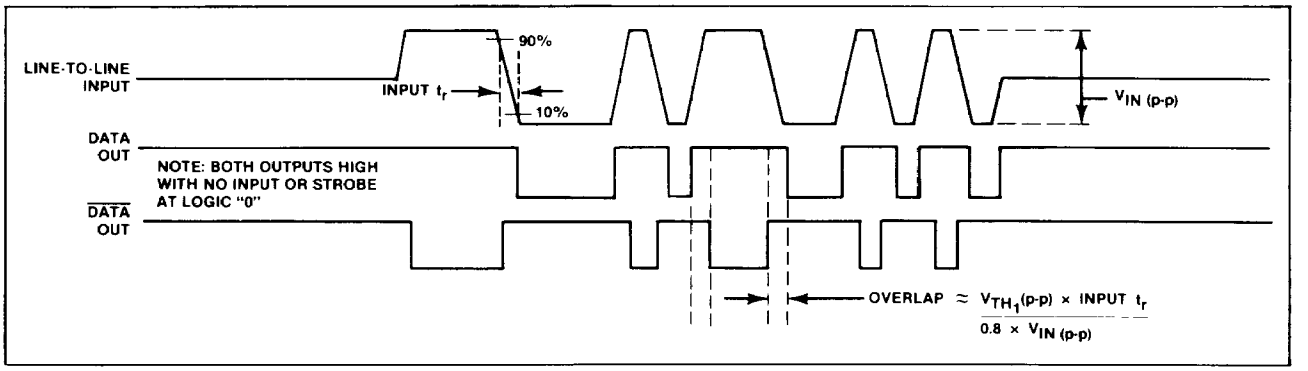


FIGURE 2.
RECEIVER LOGIC WAVEFORMS

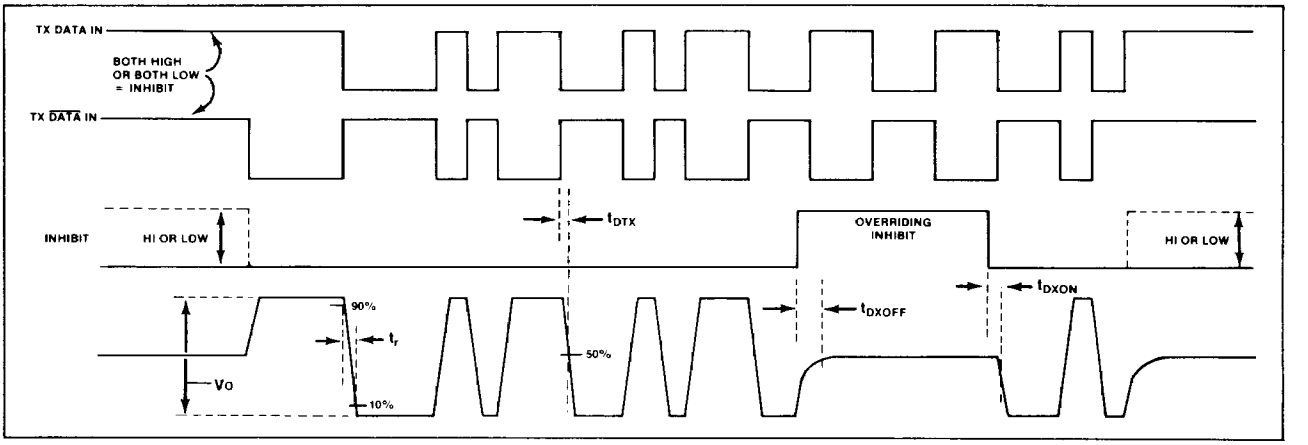


FIGURE 3.
DRIVER LOGIC WAVEFORMS

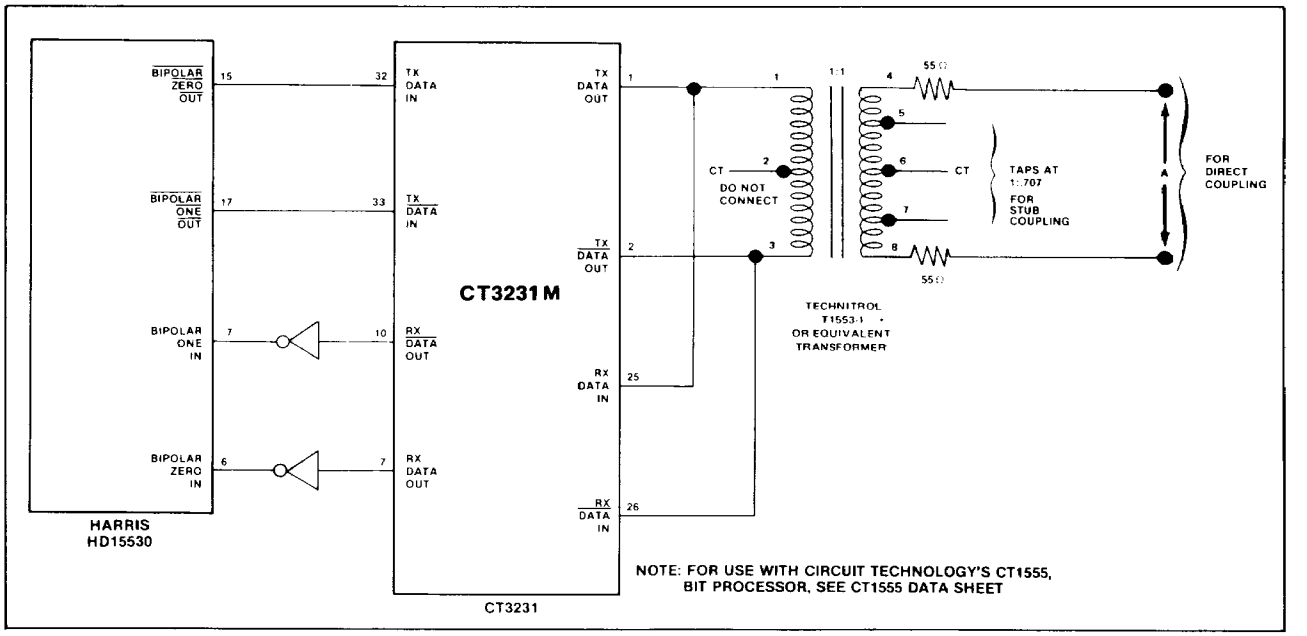
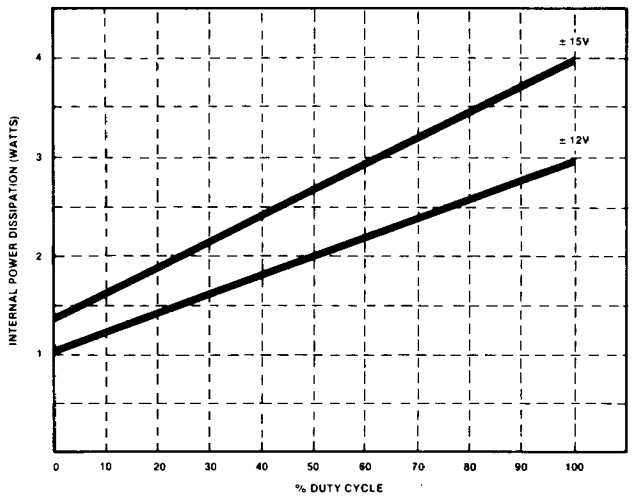


FIGURE 4.
TYPICAL INPUT/OUTPUT CONNECTIONS



$$\% \text{ DUTY CYCLE} = \frac{\text{TRANSMIT TIME}}{\text{TRANSMIT \& RECEIVE TIME}} \times 100$$

NOTE: CASE TEMPERATURE MUST BE HELD TO +100°C MAXIMUM FOR 100% DUTY CYCLE. FOR OPERATION AT CASE TEMPERATURE OF +125°C, SEE "POWER AND THERMAL DATA".

FIGURE 5.
TYPICAL POWER DISSIPATION (TOTAL HYBRID)

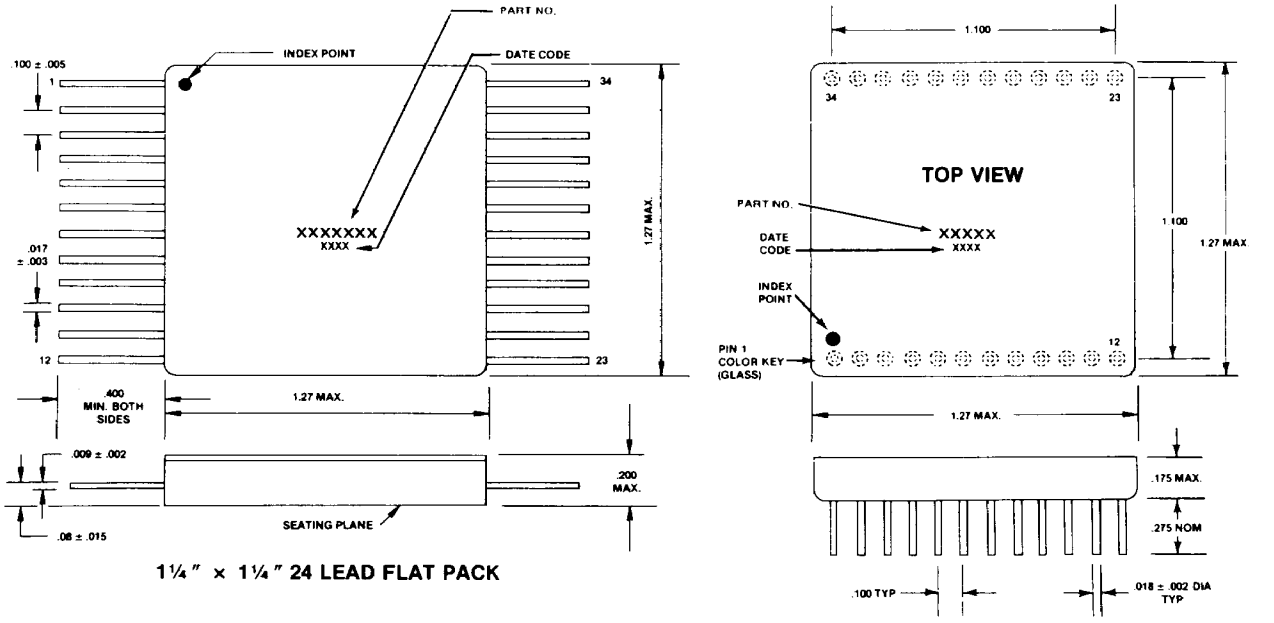


FIGURE 6.
PACKAGE OUTLINE DRAWINGS

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