GigaBlaze Transceiver Cores

CoreWare®

First Gigabit Per Second CMOS Transceiver Cores In The Industry

Overview

LSI Logic's GigaBlaze® cores are the first multi-gigabit per second CMOS transceiver cores in the industry. They provide a full-duplex, point-to-point communications channel for gigabit speed serial interfaces. Protocol independence enables the cores to be used with standard high-speed communications protocols to create a high-speed serial interface. Applications for the cores include storage subsystems, network switches and routers, System Area Network (SAN) and high-speed backplanes.

The GigaBlaze cores are optimally designed for use as a physical layer for high-speed protocols including Fibre Channel, Gigabit Ethernet, and the emerging System Area Network (SAN) standard. Multiple GigaBlaze cores can be integrated into a single ASIC. Combined with other LSI Logic standards-based cores, such as Merlin™ Fibre Channel, the TinyRISC™ and MiniRISC™ processors, and PCI, the GigaBlaze core enables a completely new approach to high-performance, single- chip solution for increased differentiation and reduced chip count, power and cost. The third generation GigaBlaze transceiver is now available in LSI Logic's G11™ process technology, along with the G10 and 500K process technologies.

Description

The GigaBlaze core consists of deserializer and serializer pattern and alignment circuitry. The deserializer receives a serial gigabit speed input encoded data stream and converts it into parallel data. This parallel data acts as an input for any high-speed protocol handler. Likewise, encoded parallel data from the protocol handler can be transmitted at gigabit speeds after being converted into a serial stream by the serializer.

The core transmitter serializes the parallel data with clock information embedded in it. The serialized output is a low-swing differential signal in NRZ format. The receiver recovers data and the embedded clock from the serial data stream, performs byte synchronization and presents parallel data with respect to the recovered clock.

The LSI Logic CoreWare design program provides the complex building blocks, proven design methodology, technology and application support necessary to build a system on a chip, optimized uniquely for the target application. This single-chip approach reduces overall system costs and accelerates time to market.

GigaBlaze G11 Core

The GigaBlaze G11 core is LSI Logic's third generation CMOS serial transceiver core. The GigaBlaze G11 core transmits data up to 2.5 Gbits/sec.

- Serial Transfer Rate: 1.0625, 1.25, 2.125 and 2.5 Gbits/sec
- ASIC Process Technology: G11, 2.5 V, 0.25-micron, cell-based CMOS process
- Parallel Data Interface: Transmitter and receiver set independently for either 10 to 20 bits wide

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GigaBlaze Transceiver Cores

Features

- A gigabit high-speed serial interface CMOS core; can be integrated with other industry-standard cores and user-defined logic for a system-on-a-chip solution
- Supports serial transfer rates of up to 2.5 Gbits/sec
- Multiple cores can be integrated on a single ASIC
- Supports full duplex operation
- Self testability via serial loop back mode
- Available in LSI Logic's leading-edge, CMOS technologies
- Core behavioral models with timing information and simulation verification environment models available with complete test vector sets
- Complete evaluation platforms available
- Worldwide design resource center support

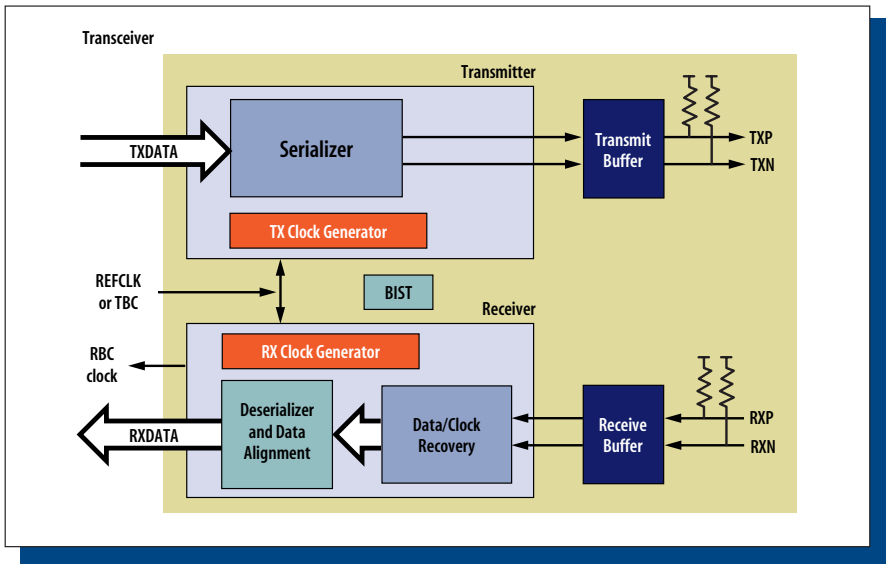

Figure 1. GigaBlaze Block Diagram

GigaBlaze Block Diagram

GigaBlaze technology provides a point-to-point, full-duplex, differential, serial communications link that transfers data at up to 2.5 Gbits/sec. It is a protocol-independent serial interface with a direct interface option to optics, twinax line or a PCB trace. Clock recovery and synchronization are included. As illustrated in Figure 1 above, this CMOS implementation is ideal for applications constrained by power and size, and offers a competitive solution to the GaAs and BiCMOS standard parts available today.

High-Speed Protocols

GigaBlaze technology provides a physical layer for emerging standard, high-speed communications protocols, such as Fibre Channel, Gigabit Ethernet, and the emerging System Area Network (SAN) as well as proprietary board-to-board or box-to-box serial communications.

Serial Data Rates (Gbps)	1.0625	1.25	2.125	2.5	3.125	4.25
GigaBlaze Next Generation						
GigaBlaze G11						
GigaBlaze G10						
GigaBlaze 500K						
Fibre Channel						
GigaBit Ethernet						
System Area Network (SAN)						

*Future Extensions (black)

Figure 2. GigaBlaze Core Specification Support

GigaBlaze Features	500K Core	G10 Core	G11 Core
Manufacturing Process Technology	LC8500K, 3.3-volt, 0.5-micron (drawn) 2-layer metal, cell-based CMOS	G10, 3.3-volt, 0.35-micron (drawn) 3-layer metal, cell-based CMOS	G11, 2.5-volt, 0.25-micron (drawn) 3-layer metal, cell-based CMOS
Parallel Data Interface	Transmitter: 20-bits wide only Receiver: either 10- or 20-bits wide	Transmitter: either 10- or 20-bits wide Receiver: either 10- or 20-bits wide	Transmitter: 20-bits wide only Receiver: either 10- or 20-bits wide
Serial Transfer Rates	1.0625 Gbit/s	1.0625, 1.25 Gbit/s	1.0625, 1.25, 2.125, 2.5 Gbit/s
Termination	External	External	Internal
Bias Generator	Separate hardmacro	Separate hardmacro	Internal to the transceiver core
External Package Pins	13-pins for each core Plus 5 pins for bias generator. Bias generator will support up to 8 cores.	13-pins for each core Plus 5 pins for bias generator. Bias generator will support up to 8 cores.	12 pins for each core

Figure 3. Three Generations of Migrated Transceiver Experience

Benefits

- Reduces cost, chip count, pin count and power consumption; increases reliability, time to market and product differentiation
- Meets the specific high bandwidth requirements of high-performance I/O
- Saves area, reduces noise and enables higher integration
- Facility for simultaneous transmit/receive transfers which improve system performance
- Ensures easy testability, reduces development time
- High-density process maximizes on-chip integration
- AC verification, fast and accurate simulations; reduces test cost, time to market
- Speeds system design
- Design assistance available

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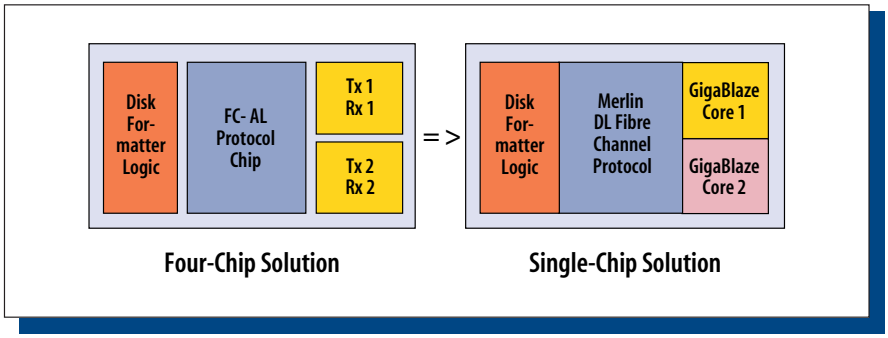

Figure 4. Single-Chip Disk Controller Diagram

Single-Chip Disk Controller

LSI Logic's GigaBlaze technology reduces the number of chips required to implement a disk controller. The standard parts solution contains up to four chips. Using two GigaBlaze cores, the Merlin DL Fibre Channel protocol core and disk formatter logic, this four-chip implementation is reduced to one chip and is illustrated in Figure 4 above.

Gigabit Ethernet

Gigabit Ethernet can drastically improve LAN backbone throughput by providing 10 times the bandwidth of Fast Ethernet. In the example illustrated in Figure 5 below, Gigabit Ethernet improves server access by providing a 1 Gbit/s link from a Fast Ethernet Switch to the server. LSI Logic's GigaBlaze technology can serve as a physical layer for Gigabit Ethernet connections.

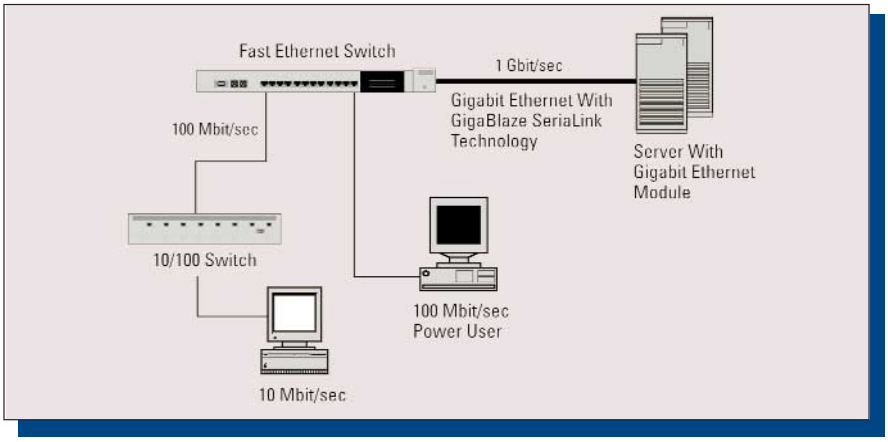

Figure 5. Gigabit Ethernet Diagram

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