SONY

CX20172

Balanced Transformer-less DUAL Amplifier for Audio Use

Description

The CX20172 is a bipolar IC designed as a BTL (balanced transformer-less) amplifier or a DUAL amplifier which can drive an 8Ω load with one dry cell (1.5 V).

Features

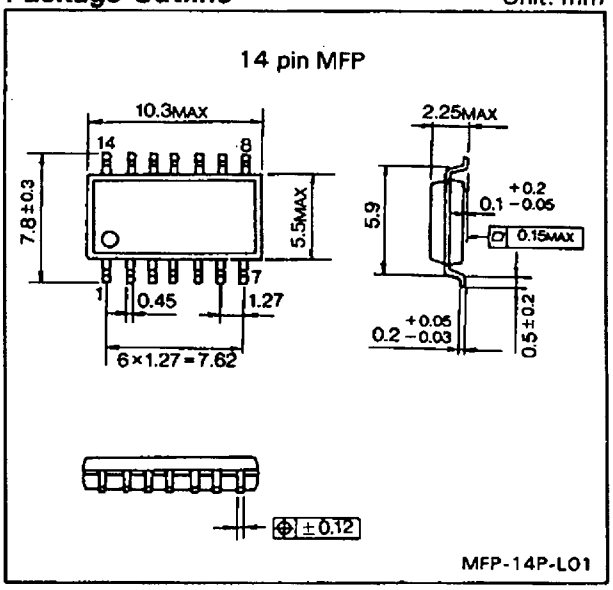
- Operates with one dry cell (operable if Vcc is reduced down to 0.9 V)
- Low power consumption (standard current without signals; 5 mA, 8Ω load, BTL, Vcc=1.25V)
- Large output (BTL: 80 mW/8 Ω, EIAJ; DUAL: 21 mW/CH, 8 Ω load, EIAJ; Vcc = 1.5 V for both BTL and DUAL)
- The mode of either BTL amplifier or DUAL amplifier, as well as their gain setting, is selected by combining the IC with external components.
- Muting and power ON/OFF functions incorporated.

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



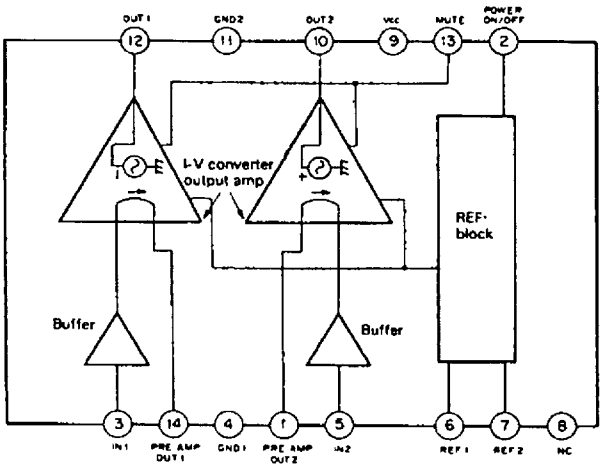
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	4.5	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	560	mW

Recommended Operating Conditions

• Supply voltage	Vcc	0.9 to 2.2	V

Block Diagram



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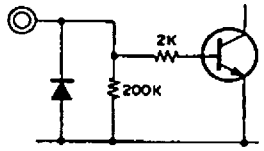
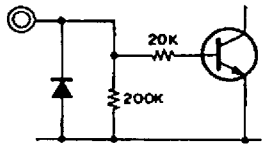
Pin Description

(Ta = 25°C, Supply voltage: 1.25 V)

No.	Symbol	Description	Standard pin voltage (V)
1	Pre Amp out 2	Pin to be connected with a load resistor in the preceding-stage buffer amplifier of CH2. See the Electrical Test Circuit application circuit of BTL mode, and DUAL mode.	0.7
2	Power ON/OFF	ON/OFF switching pin for the whole of the IC. H: (power supply) IC ON L: (ground) IC OFF  (standard internal equivalent circuit)	–
3	IN1	Input pin for CH1. This pin is connected to the ground via a coupling capacitor, the same one as used for the input pin, when the pin is not used as an input pin in the BTL mode. Standard input resistance: 10 kΩ	–
4	GND1	Grounding mainly for the preceding stage	–
5	IN2	Input pin for CH2. This pin is connected to the ground via a coupling capacitor, the same one as used for the input pin, when the pin is not used as an input pin in the BTL mode. Standard input resistance: 10 kΩ	0.7
6	REF1	Output pin for internal reference voltage (high impedance) for phase compensation	0.7
7	REF2	Output pin for internal reference voltage (low impedance)	0.7
8	NC		–
9	Vcc	Power supply pin	–
10	OUT2	Output pin for CH2	0.55 (0.74 during MUTE)
11	GND2	Grounding mainly for the output stage	–
12	OUT1	Output pin for CH1	0.55 (0.74 during MUTE)
13	MUTE	Switch pin to activate the MUTE operation H: (power supply) normal operation L: (ground) MUTE  (standard internal equivalent circuit)	–
14	Pre Amp out 1	Pin to be connected with a load resistor in the preceding stage buffer amplifier of CH1. See the Electrical Test Circuit application circuit of BTL mode, and DUAL mode.	0.7

Electrical Characteristics

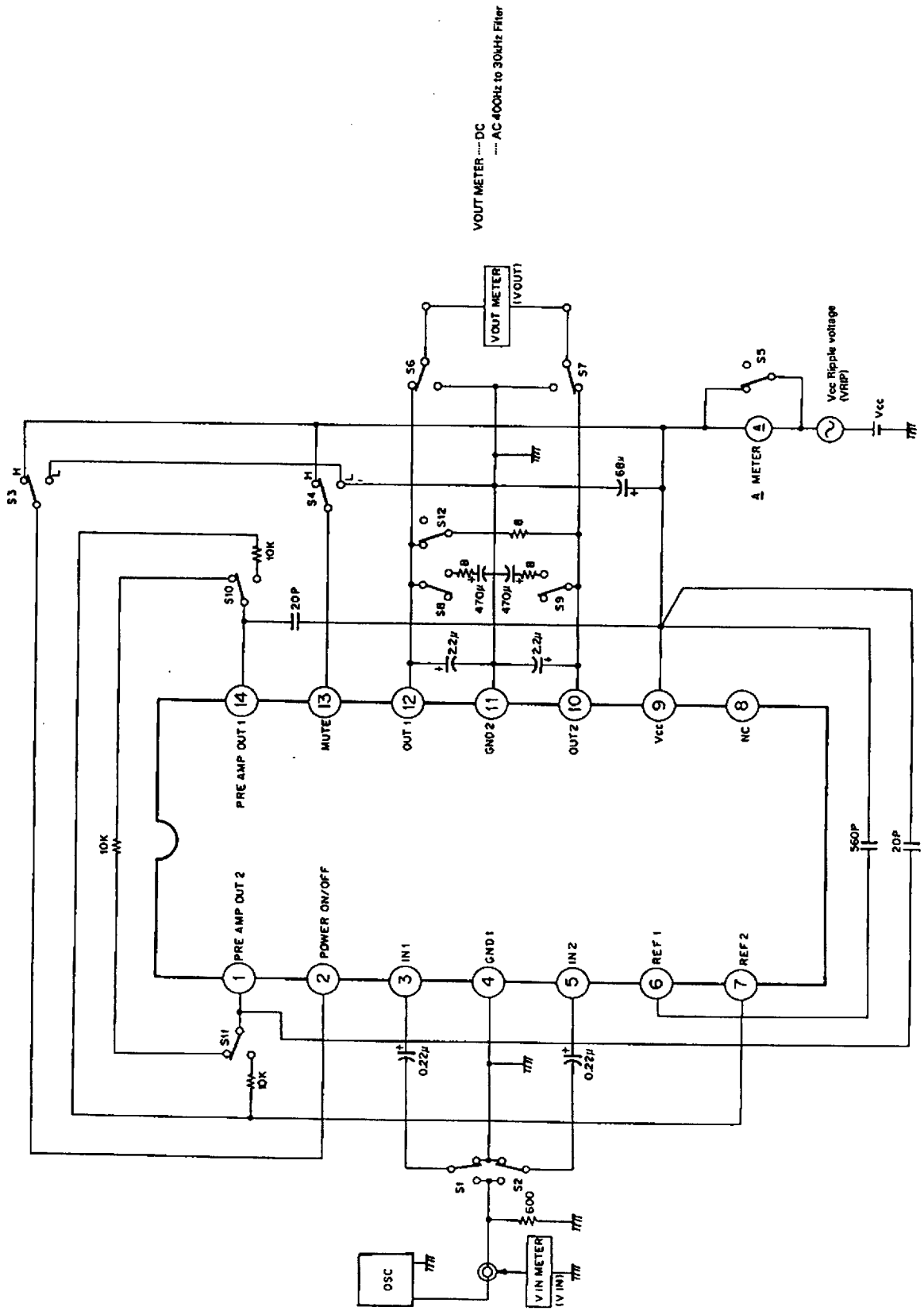
(Ta = 25°C, See the Electrical Characteristics Test Circuit)

No.	Test Item		Symbol	Switches to be set ON	Power Source I/O Conditions: Supply Voltage V_{CC}	Signal Input V_{IN}	Signal Output V_{OUT}	Test Points	Measurement Method and Contents		Min.	Typ.	Max.	Unit
1	Current consumption 1		I_{ON}	S5	1.25(V)			A METER(DC)	Current consumption in BTL with an 8 Ω load and no signal input		2.5	5.0	11.0	mA
2	Output offset voltage		$V\triangle 12$	S7	↓			V_{OUT}(DC)	CH1 DC Output voltage	(CH1 DC output voltage) − (CH2 DC output voltage) is calculated in BTL with an 8 Ω load	−30	0	+30	mV
				S6	↓			V_{OUT}(DC)	CH2 DC Output voltage					
3	Current consumption 2		I_{OFF}	S3, S4, S5	2.0(V)			A METER(DC)	Current consumptions in Power OFF, MUTE			0	10	μA
4	Gain BTL 1		G_{BTL1}	S1	1.25(V)	Adjustment	−20dBm	V_{IN}, V_{OUT}(AC)	Gain for the output of −20 dBm		23.5	25.5	28.0	dB
5	Gain BTL 2		G_{BTL2}	S2	0.9(V)	↓	↓	↓			22.5	24.5	28.0	dB
6	△Gain BTL		$\triangle G_{BTL}$	Arithmetic	—	—	—	—	$\triangle G_{BTL} = G_{BTL1} - G_{BTL2}$			1.0	3.0	dB
7	THD BTL		THD_{BTL}	S1	1.25(V)	Adjustment	−10dBm	V_{OUT}(AC)	THD (BTL) for the output of −10 dBm			1.5	2.5	%
8	EIAJ maximum output BTL		P_{BTLMAX}	S1	1.5(V)	↓	THD10%	V_{OUT}(AC)	BTL output for the output THD of 10%		70	82		mW
9	Ripple output voltage BTL		RIP_{BTL}		1.0(V) +(−30dBm)			V_{RIP}, V_{OUT}(AC)	Check the PTL output by overlaying the ripple voltage with 1 V power supply.			−79	−65	dBm
10	Noise output voltage BTL		N_{BTL}		2.0(V)			V_{OUT}(AC)	Noise output voltage in BTL with an 8 Ω load and no signal input			−80	−75	dBm
11	Output during MUTE		M_{ETL}	S1, S4	1.0(V)	−20dBm		V_{OUT}(AC)	BTL output in the MUTE state				−100	dBm
12	Gain DUAL	CH1	G_{DUAL1}	S1, S7, S8, S9, S10, S11, S12	1.25(V)	Adjustment	−26dBm	V_{IN}, V_{OUT}(AC)	CH1 input CH1 output	Gain for individual outputs of −26 dBm, 8 Ω load	19.0	21.0	24.0	dB
		CH2	G_{DUAL2}	S2, S6, S8, S9, S10, S11, S12	↓	↓	↓	↓	CH2 input CH2 output					
13	Channel balance		$\triangle G_{D12}$	Arithmetic	—	—	—	—	$\triangle G_{D12} = G_{DUAL1} - G_{DUAL2}$		−1.5	0	+1.5	dB
14	THD DUAL	CH1	THD_{D1}	S1, S7, S8, S9, S10, S11, S12	1.25(V)	Adjustment	−16dBm	V_{OUT}(AC)	CH1 input CH1 output	THD for individual outputs of −16 dBm.		0.9	2.5	%
		CH2	THD_{D2}	S2, S6, S8, S9, S10, S11, S12	↓	↓	↓	↓	CH2 input CH2 output					
15	EIAJ maximum output dUAL	CH1	$P_{D1\ MAX}$	S1, S7, S8, S9, S10, S11, S12	1.5(V)	↓	THD10%	↓	CH1 input CH1 output	Output for the individual CH THD's of 10%. 8 Ω load	16	20		mW
		CH2	$P_{D2\ MAX}$	S2, S6, S8, S9, S10, S11, S12	↓	↓	↓	↓	CH2 input CH2 output					
16	Cross talk between DUAL CH'S	CH1 →CH2	C_{TAB}	S1, S6, S8, S9, S10, S11, S12	1.25(V)	Test 12 equivalent to OSC in G_{DUAL1}		V_{IN}, V_{OUT}(AC)	CH1 input CH2 output	The output level at the CH opposite with the input CH		−51	−45	dB
		CH2 →CH1	C_{TBA}	S2, S7, S8, S9, S10, S11, S12	↓	Test 17 equivalent to OSC in G_{DUAL2}		↓	CH2 input CH1 output					

• Both signal input V_{IN} and ripple input V_{RIP} are 1 kHz.

• dBm (600 Ω) 0 dBm: 774.6mVrms
• BPF is set to 400 Hz to 30 kHz for AC measurement.

Electrical Characteristics Test Circuit



Description of Operation

The CX20172 incorporates two buffer amplifiers in the preceding stage and two current input amplifiers in the succeeding stage. Selection between the BTL amplifier and DUAL amplifier is made by altering the method of attaching external components as shown in the Application Circuit.

1. BTL mode (see the BTL mode Application Circuit)
   - Items 1 to 11 in the Electrical Characteristics are the characteristics for the BTL mode.
   - Input through either IN1 or IN2 results in a reverse-phase output at the output side of the input channel and in the same-phase output at the other, to enable BTL driving of the load between OUT1 and OUT2.
   - Ground the unused input pins via a coupling capacitor which is the same one used for the input pin.
   - Gain setting can be altered by changing values of external resistors connected between Pre Amplifier out 1 and 2. Gain decreases as a resistor value between Pin 1 and Pin 14 increases. Reducing a resistor value to increase the gain results in larger output offset and current consumption. I/O characteristics, distortion factor and maximum output change according to resistor values. Specify a set value, therefore, in view of input level, output level, distortion and power consumption.
   - The value of a phase-compensation capacitor can be altered considerably according to patterns on mounting substrate.

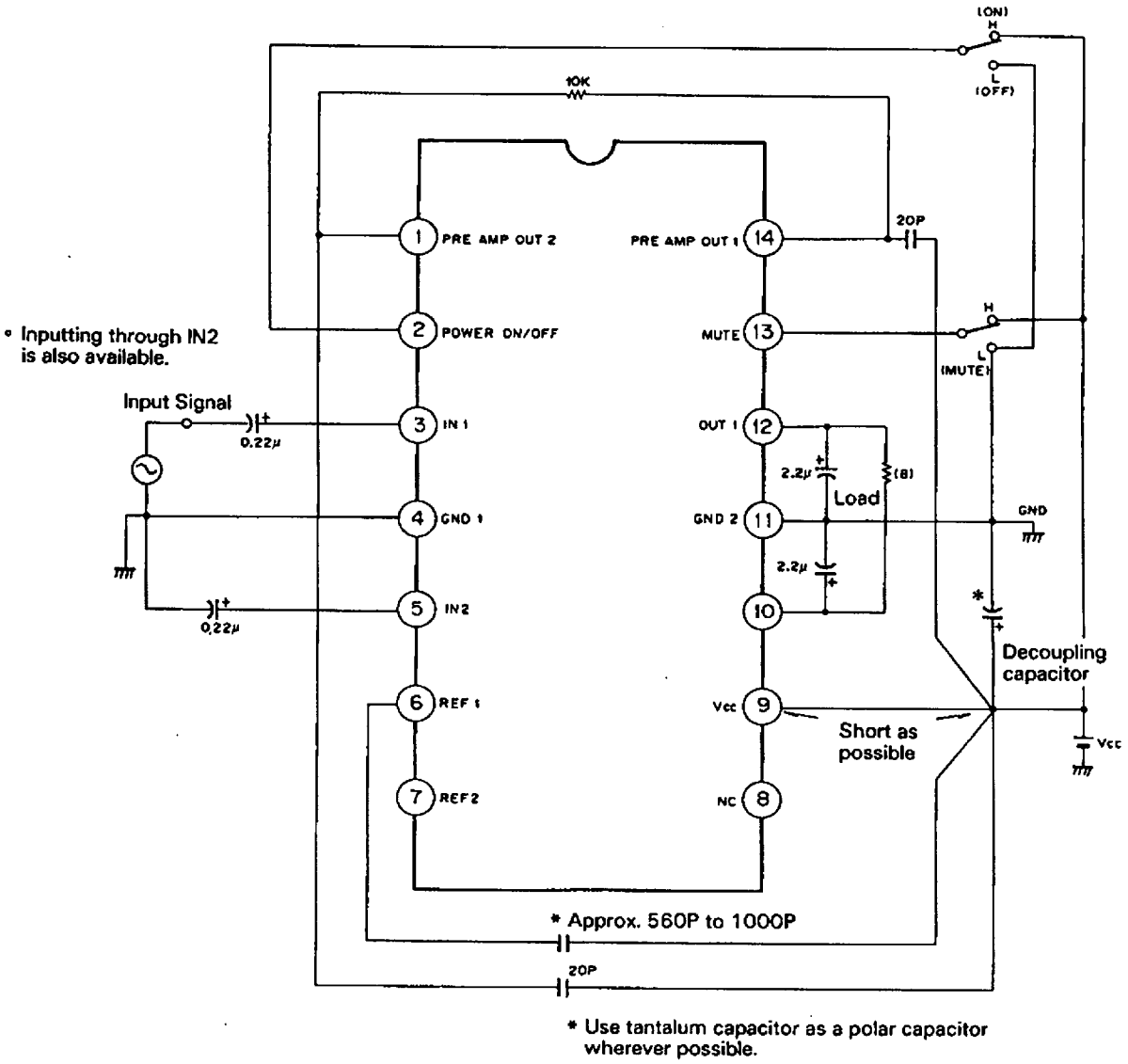
2. Dual mode (see the Dual mode Application Circuit)
   - Items 12 to 16 in the Electrical Characteristics are the characteristics for the Dual mode.
   - Simultaneous input through IN1 and IN2 results in reverse-phase outputs at both output pins to enable DUAL driving.
   - Gain setting can be altered by changing values of external resistors connected between Pre Amplifier out 1 and 2 and REF2, similarly to the BTL mode. Gain decreases as resistor value increases. I/O characteristics, distortion factor and maximum output change according to resistor values. The same consideration as in the BTL mode is, therefore, required. Current consumption has, however, less dependency on the gain than in BTL.
   - The value of a phase-compensation capacitor can be altered considerably according to patterns on mounting substrate.

3. Common functions

3.1 REF block
   - Circuit block to generate reference voltage.
     REF1 (Pin 6) is an output from the block (high impedance). This is reduced in its impedance through the buffer amplifier to generate REF2 (Pin 7).

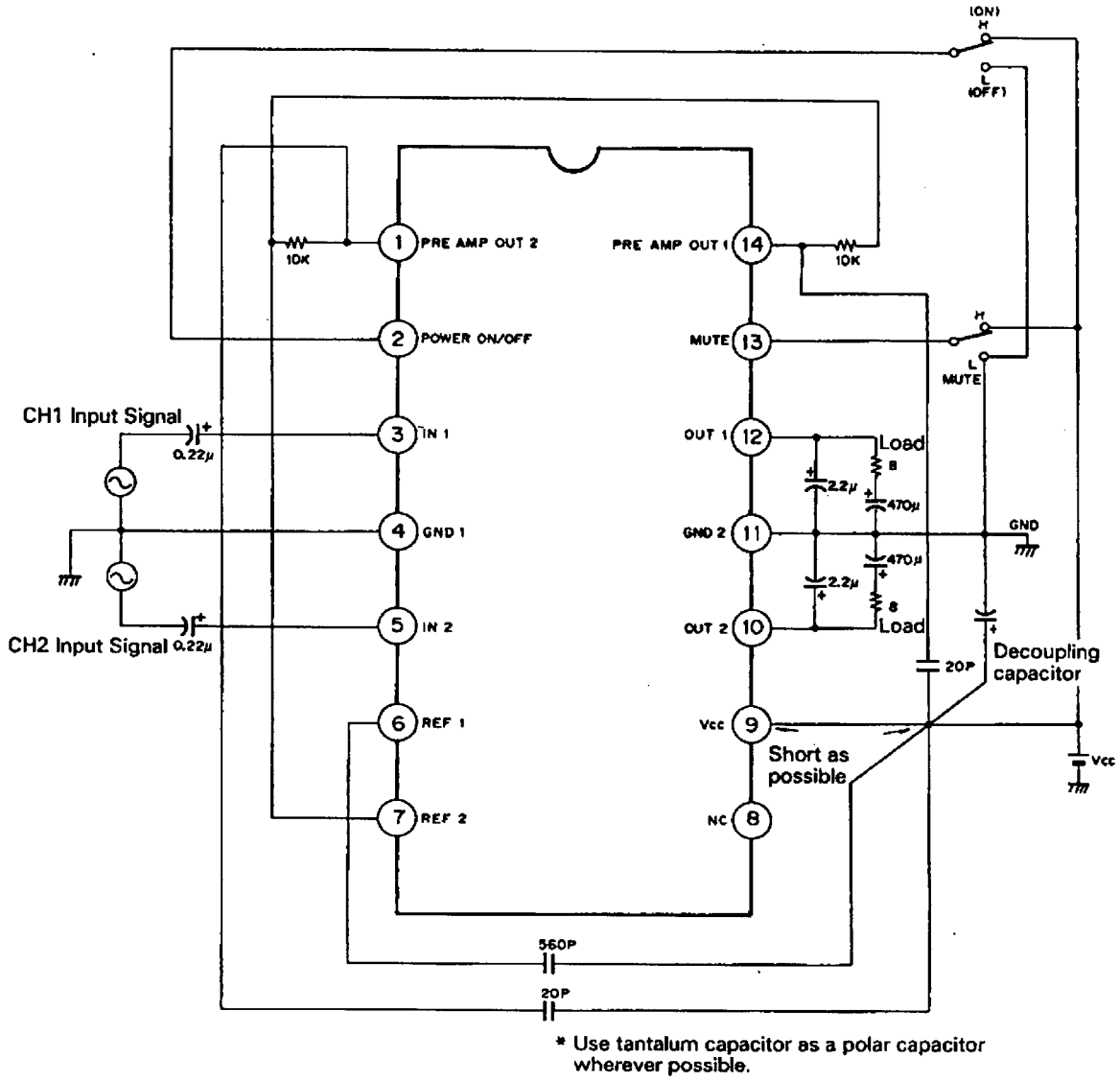
3.2 Mute, Power ON/OFF block
   - Grounding the Mute pin (Pin 13) results in the interrupt of the signal route to generate DC voltage of approx. 700 to 765 mV at both output sides of channel (CH).
   - Grounding the Power ON/OFF pin (Pin 2) results in the OFF state of the REF block and the output is grounded.

BTL Mode Application Circuit



Note) Place a decoupling capacitor between Vcc and GND as close as possible to Vcc and GND2. Assuming this point as the point of power supply or grounding, place (*)-marked components as close as possible.
Values of the decoupling capacitor can be altered according to the pattern layouts.

Dual Mode Application Circuit



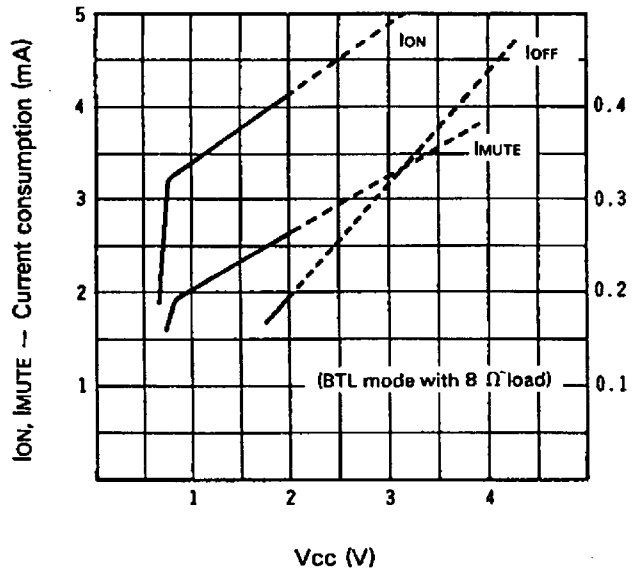
* Use tantalum capacitor as a polar capacitor wherever possible.

Note) Notes for the above are almost same as in BTL.

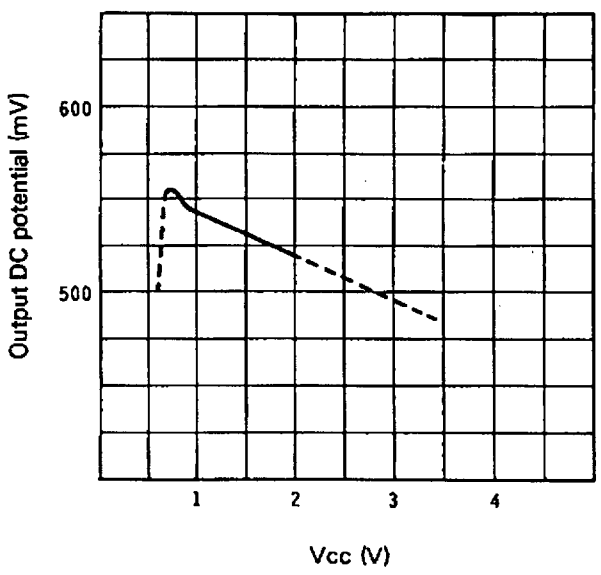
Standard Characteristics

- See "Electrical Characteristics Test Circuit " for the test circuit.
- A resistor between Pin 1 and Pin 14 to determine the gain is of 10 kΩ, unless otherwise specified.
- Measuring temperature is 25°C, unless otherwise specified.

Current consumption I_{ON}, I_{MUTE}, I_{OFF} — Vcc

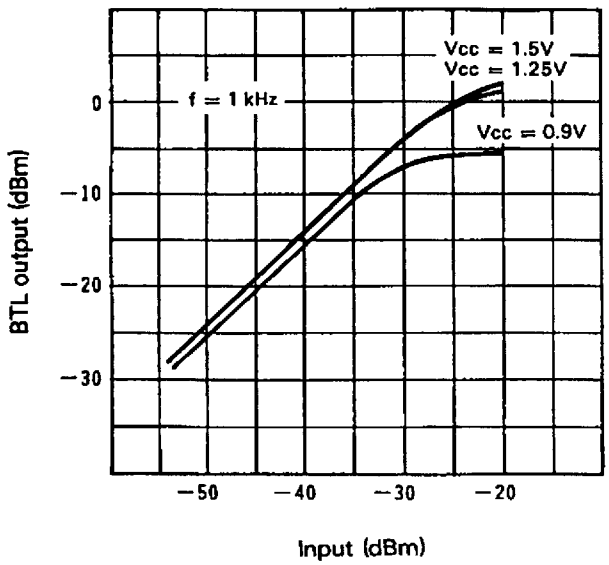


Output DC electric potential — Vcc

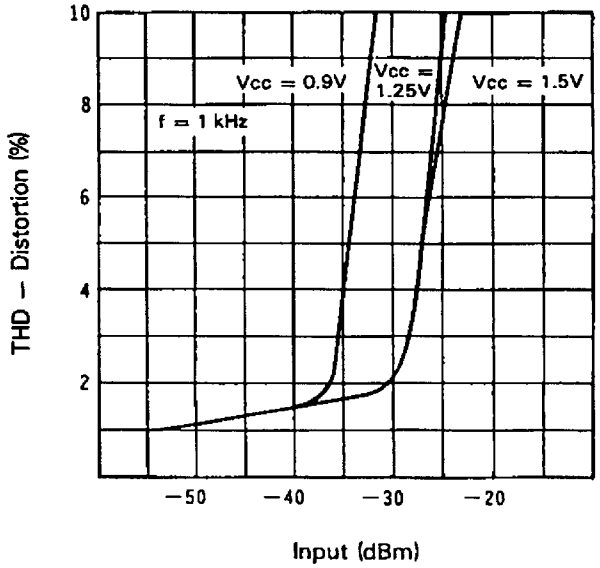


I_{ON} and I_{OFF} are measured conforming to the methods in the measurement 1 and 3.
I_{MUTE} represents the current consumption with S4 and S5 ON.

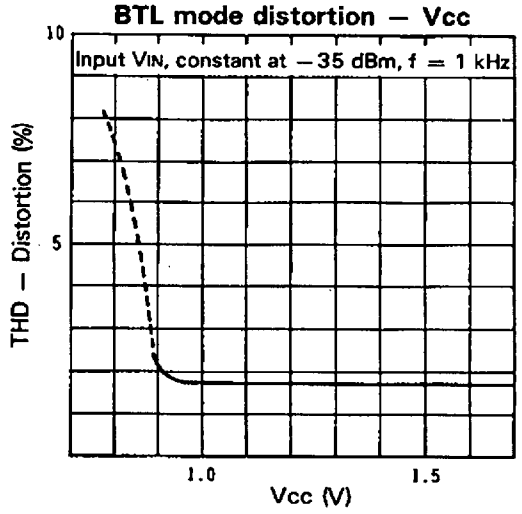
BTL Mode, I/O characteristics (Vcc Parameter)



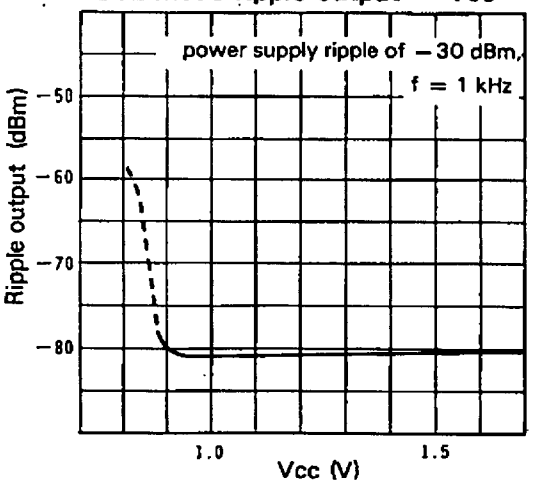
BTL Mode distortion — input level (Vcc Parameter)



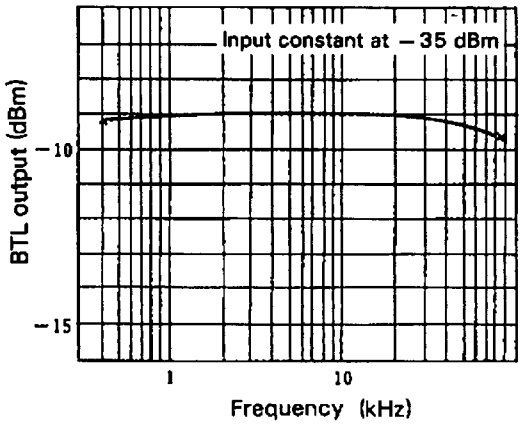
BTL mode distortion — Vcc



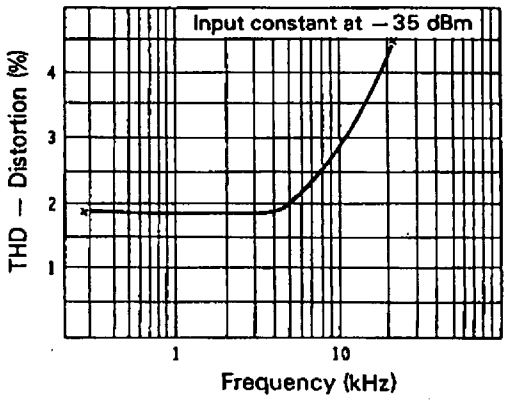
BTL mode ripple output — Vcc



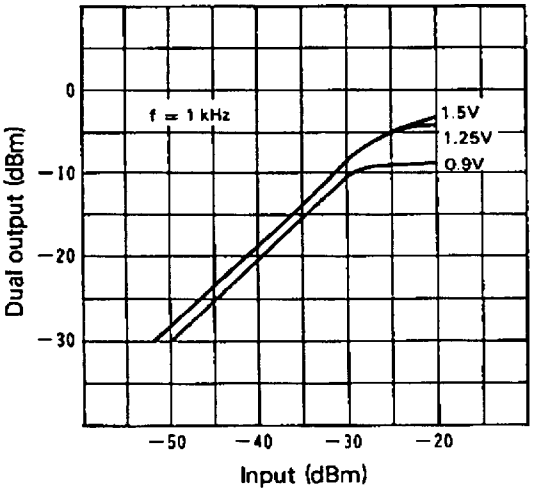
BTL mode output frequency characteristics



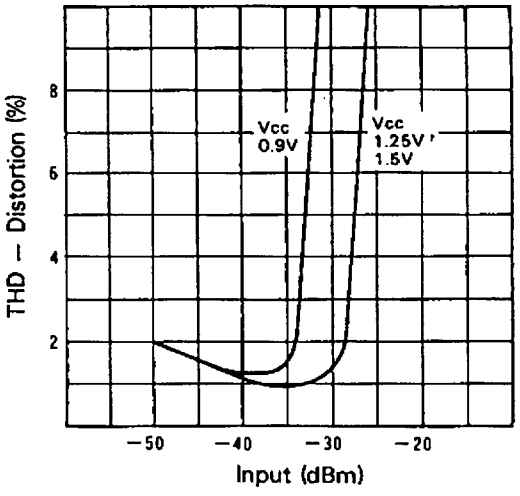
BTL mode distortion frequency characteristics



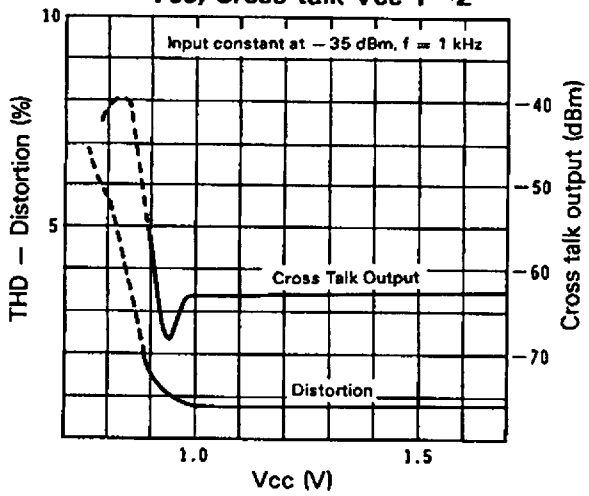
Dual mode I/O characteristics (Vcc Parameter)



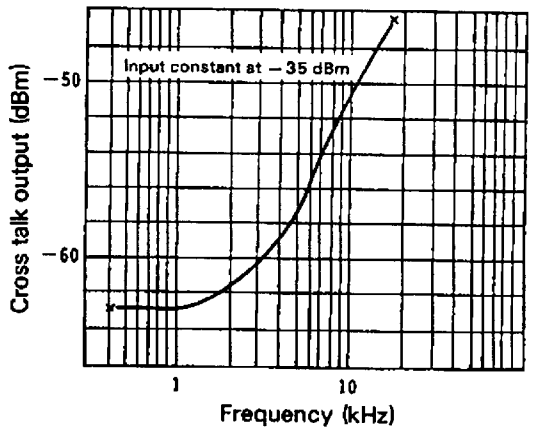
Dual mode distortion — input level (Vcc Parameter)



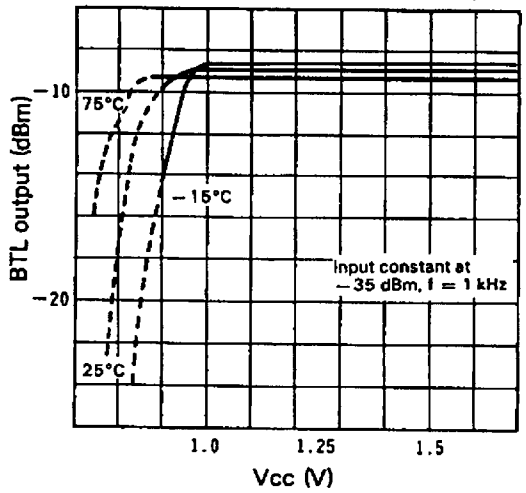
Dual mode distortion — Vcc, Cross talk Vcc 1→2



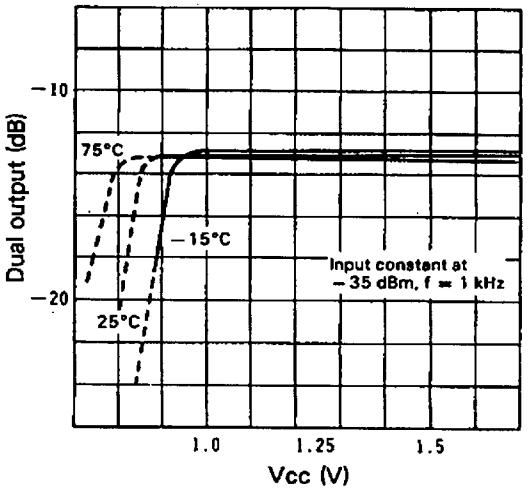
Dual mode cross talk output frequency characteristics



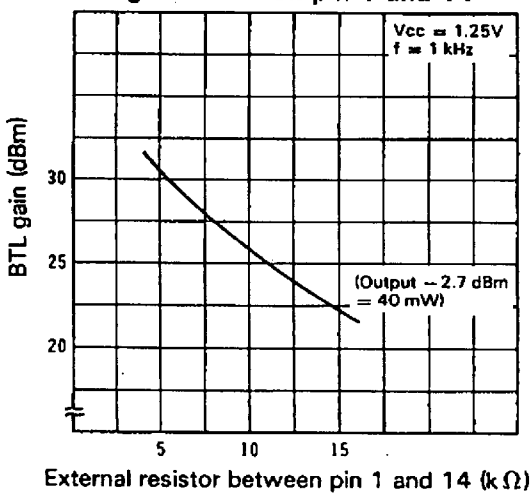
BTL Mode output level — Vcc (Temperature characteristics)



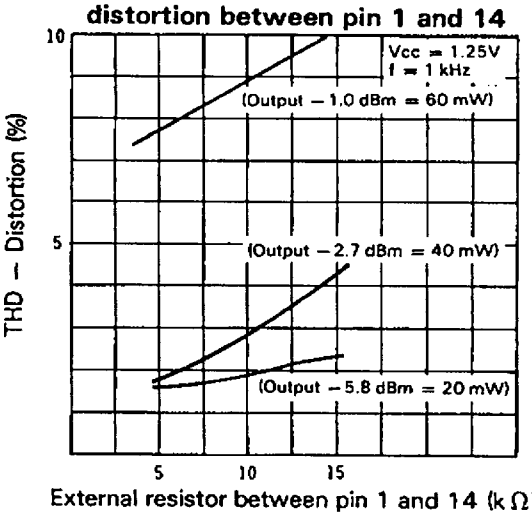
Dual mode output level — Vcc (Temperature characteristics)



BTL mode external resistance — gain between pin 1 and 14



BTL mode external resistance — distortion between pin 1 and 14



BTL mode external resistance — maximum output between pin 1 and 14